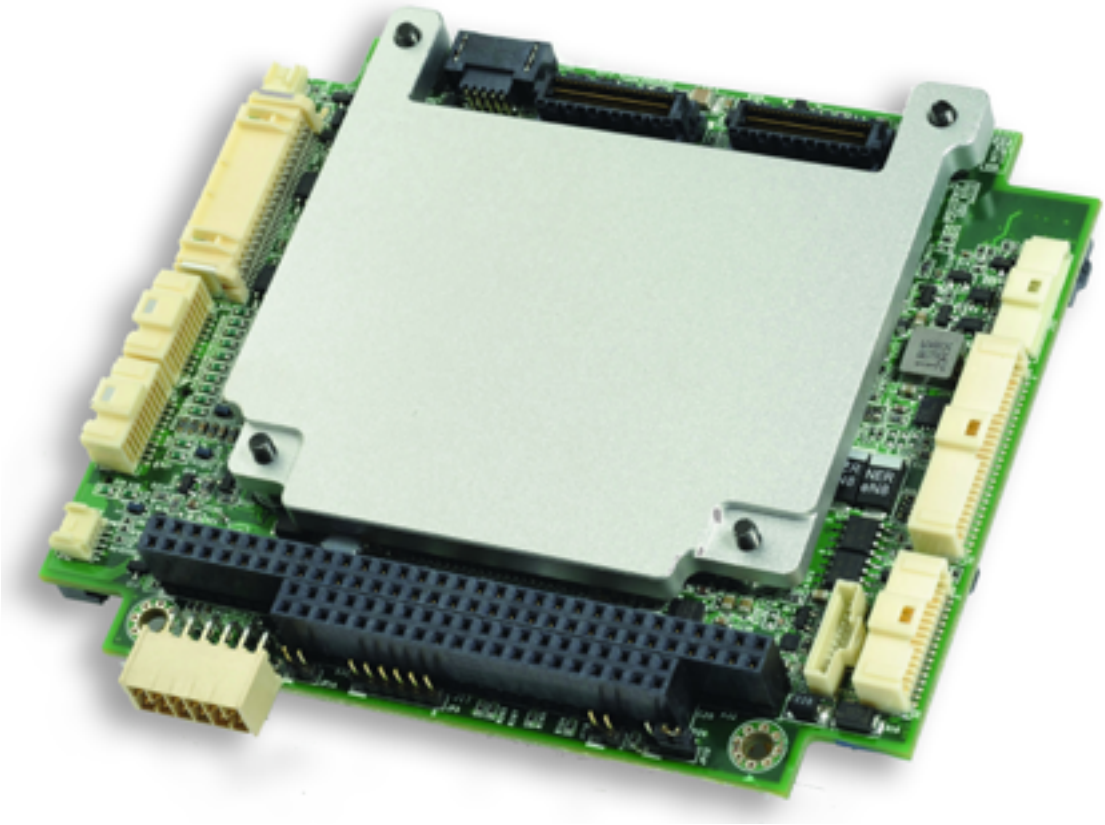
PXM-C388-S

PC/104-compatible 1.66 GHz Intel® ATOM™ -based SBC with Video, Ethernet, and Stackable SUMIT™ PCI Express PC/104 Modules Expansion

PRODUCT MANUAL



WinSystems, Inc.
715 Stadium Drive
Arlington, TX 76011

http://www.winsystems.com

MANUAL REVISION HISTORY

P/N 400-388-000

Revision Date Code	ECO Number
120514	Initial Release
120523	
120806	
120820	
121113	
130206	
130404	
130710	
130724	
140729	14-69

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BEFORE YOU BEGIN

WinSystems offers best practice recommendations for using and handling WinSystems embedded PCs. These methods include valuable advice to provide an optimal user experience and to prevent damage to yourself and/or the product.

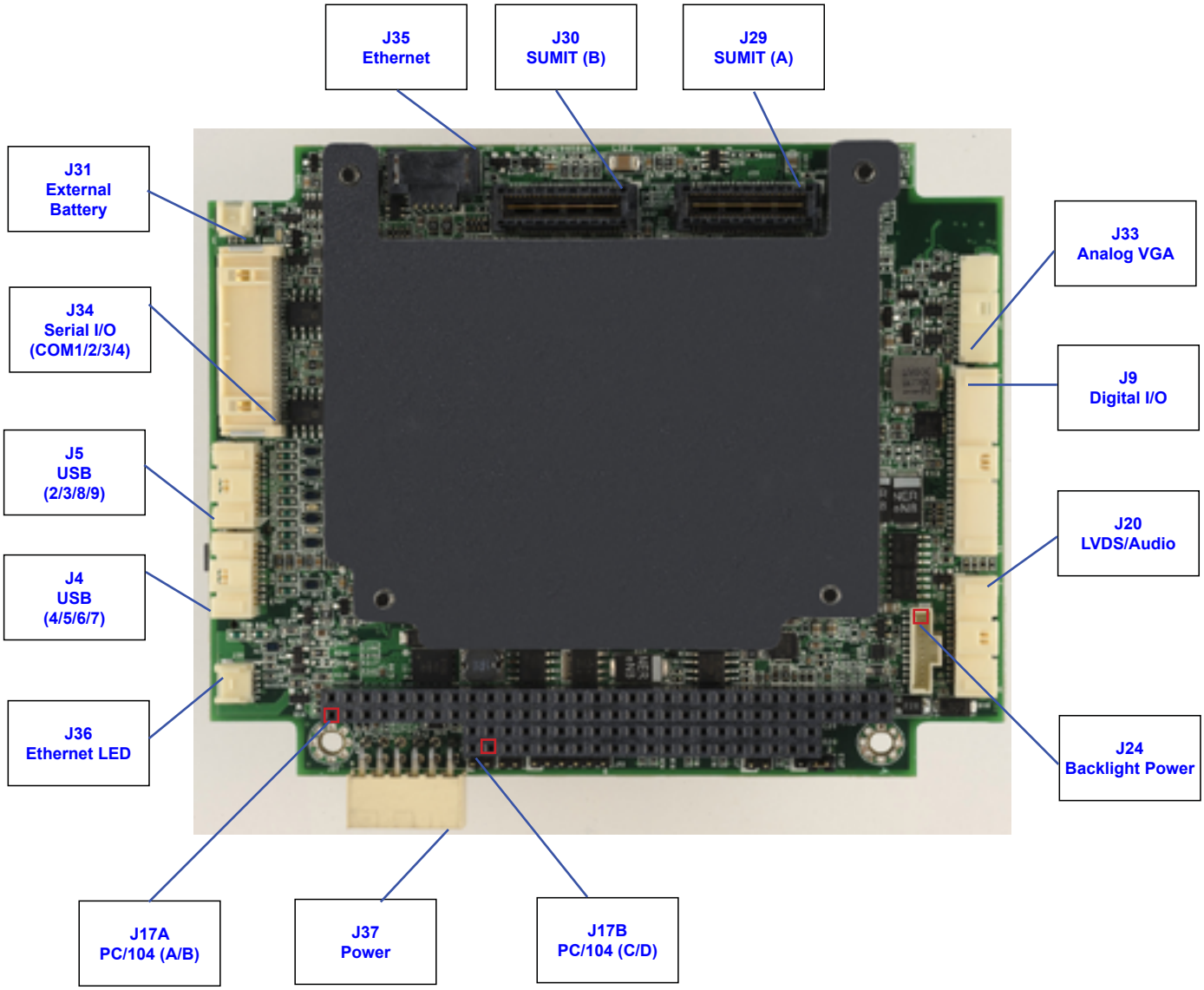
YOU MAY VOID YOUR WARRANTY AND/OR DAMAGE AN EMBEDDED PC BY FAILING TO COMPLY WITH THESE BEST PRACTICES.

Reference Appendix - A for **Best Practices**.

Please review these guidelines carefully and follow them to ensure you are successfully using your embedded PC.
This product ships with a heat sink. Product warranty is void if the heat sink is removed from the product.

For any questions you may have on WinSystems products, contact our Technical Support Group at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

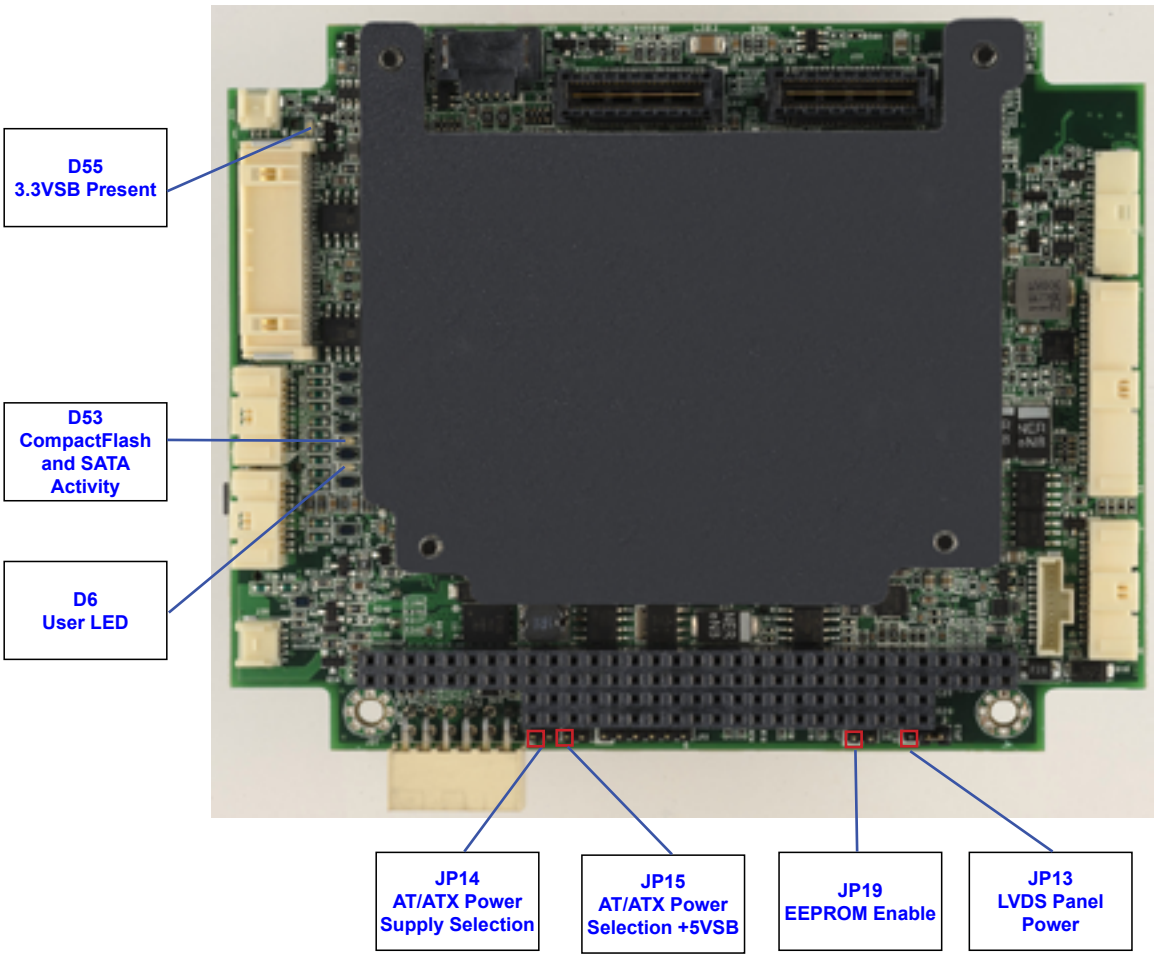
Visual Index - Top View (Connectors)



RESERVED -

NOTE: The reference line to each component part has been drawn to Pin 1, and is also highlighted with a square, where applicable.

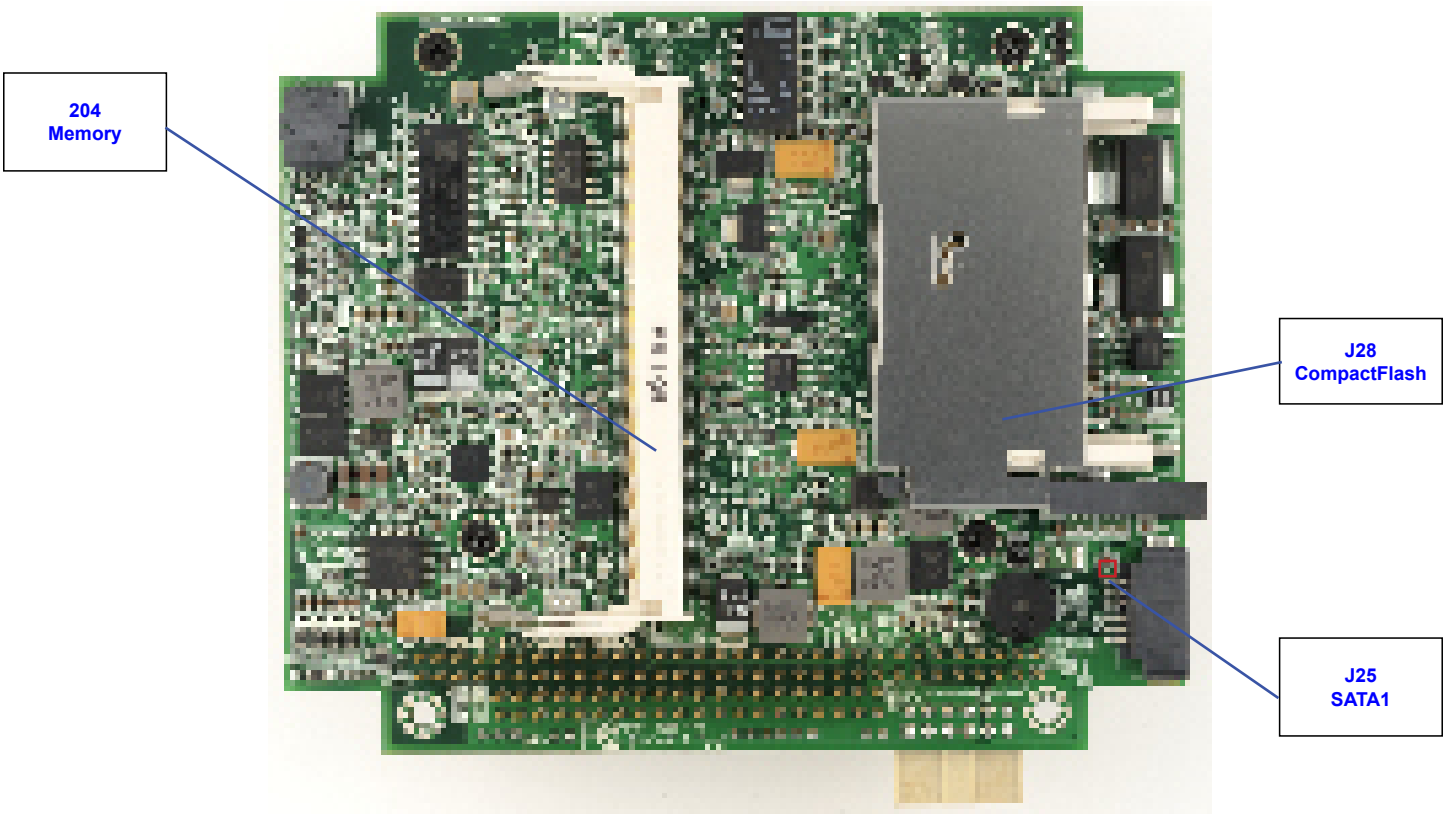
Visual Index - Top View (Jumpers & LEDs)



RESERVED - JP3

NOTE: The reference line to each component part has been drawn to Pin 1, and is also highlighted with a square, where applicable.

Visual Index - Bottom View



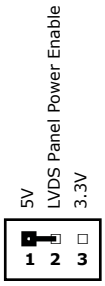
RESERVED -

NOTE: The reference line to each component part has been drawn to Pin 1, and is also highlighted with a square, where applicable.

Jumper Reference

NOTE: Jumper Part# SAMTEC 2SN-BK-G is applicable to all jumpers. These are available in a ten piece kit from WinSystems (Part# KIT-JMP-G-200).

JP13 - LVDS Power



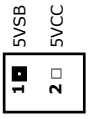
Avoid Simultaneous Jumpering of pins 1-2 and 2-3. Misjumpering panel power causes damage to the board and/or the Flat Panel.

LVDS Enable (default)	1-2
LVDS Disable	2-3

JP14 - Power Selection

JP14

JP15 (Rev. B only)



NOTE: Both jumpers need to be installed for AT mode.

JP19 - EEPROM Enable

JP19

EEPROM Enable	JP19
CMOS EEPROM Enable (default)	1-2
CMOS EEPROM Disable	Open

INTRODUCTION

This manual is intended to provide the necessary information regarding configuration and usage of the PXM-C388 single board computer. WinSystems maintains a Technical Support Group to help answer questions not adequately addressed in this manual. Contact Technical Support at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

FEATURES

CPU
- Intel® ATOM™ N455 single core @ 1.66 GHz

Compatible Operating Systems
- Linux, Windows, and other x86 compatible OS

Memory
- Up to 2 GB of DDR3 SODIMM (Socketed)

BIOS
- Phoenix

Video
- Analog VGA resolution up to SXGA 1400x1050
- LVDS 18-bit support up to 1366x768 or 1280x800
- Simultaneous LVDS and CRT video supported

Ethernet
- Intel® 10/100/1000 Mbps controller (ICH8M)

Storage
- 1 SATA (2.0) channel
- CompactFlash Types I and II memory socket supported

Digital I/O
- 24 GPIO with event sense

Bus Expansion
- PC/104
- SUMIT

Serial I/O
- 4 Serial ports (2 RS-232, 2 RS-232/422/485)

USB
- 8 USB 2.0 ports

Watchdog Timer
- Adjustable from 1 second to 255 minute reset

Audio
- Stereo supported

Power
- 5V required, 2.5A typical

Industrial Operating Temperature
- -40°C to 85°C

Mechanical
- Dimensions: 4.6” x 3.8” (116 mm x 96 mm)
- Weight: 7.2 oz (204g) (for PXM-C388-S1-0-0)

Additional Features
- RoHS compliant
- LED Backlight supported
- Custom splash screen on start-up
- Real-time clock/calendar

System

WinSystems’ PXM-C388 is a SUMIT-ISM Single Board Computer (SBC) with PC/104 expansion that uses Intel’s ATOM N455 single core 1.66 GHz processor paired with the ICH8M controller hub.

The SBC is a full-featured unit with on-board I/O that supports CRT/LVDS simultaneously, Gigabit Ethernet port, eight USB 2.0 ports, two serial RS-232/422/485 COM channels, two serial RS-232 COM channels, 24 digital I/O lines with event sense, HD audio, watchdog timer, and two SUMIT connectors. Plus it has a PC/104 connector for additional I/O expansion.

Memory

The PXM-C388 board supports up to 2 GB DDR3 SODIMM system memory via an on-board socket located at **U9**.

FUNCTIONALITY

The PXM-C388 is well suited for directly upgrading existing PC/104-based designs with Intel's Atom processor family. It blends high-speed serial bus expansion with legacy PC/104 I/O module migration to strike a balance of high-integration computing power for existing cost-effective applications requiring relays, digital I/O and low-to-moderate speed analog I/O.

I/O Port Map

Following is a list of I/O ports used on the PXM-C388-S.

NOTE: The PXM-C388-S uses a PnP BIOS resource allocation. Care must be taken to avoid contention with resources allocated by the BIOS.

HEX Range	Usage
0000h-001Fh	DMA Controller 82C37
0020h-0021h	Interrupt Controller PIC 8259
0024h-0025h	Interrupt Controller
0028h-0029h	Interrupt Controller
002Ch-002Dh	Interrupt Controller
002Eh-002Fh	Forward to Super IO
0030h-0031h	Interrupt Controller
0034h-0035h	Interrupt Controller
0038h-0039h	Interrupt Controller
003Ch-003Dh	Interrupt Controller
0040h-0043h	Timer counter 8254
004Eh-004Fh	Forward to Super IO
0050h-0053h	Timer counter 8254
0060h	Keyboard data port
0061h	NMI controller
0062h	8051 download 4K address counter
0064h	Keyboard status port
0066h	8051 download 8-bit data port
0070h-0077h	RTC Controller
0080h-0091h	DMA Controller
0092h	Reset Generator
0093h-009Fh	DMA Controller
00A0h-00A1h	Interrupt Controller PIC 8259
00A4h-00A5h	Interrupt Controller
00A8h-00A9h	Interrupt Controller
0ACh-00ADh	Interrupt Controller
00B0h-00B1h	Interrupt Controller
00B2h-00B3h	Power Management
00B4h-00B5h	Interrupt Controller
00B8h-00B9h	Interrupt Controller
00C0h-00DFh	DMA Controller 82C37
00F0h	FERR#/IGNNE/Interrupt Controller
0140h-01FFh	Reserved *
0170h-0177h	IDE1 Controller
0180h-01FFh	Reserved
0298h-029Bh	Reserved for Super I/O Configuration
029C	Interrupt Status Register
029D	Status LED Register

HEX Range	Usage
029E-029F	Watchdog Timer Control
02E8h-02EFh	COM4 (Default)
02F8h-02FFh	COM2 (Default)
0340h-03E7h	Reserved *
0376h	IDE1 Controller
0378h-037Bh	Reserved
03E8h-03EFh	COM3 (Default)
03F0h-03F5h	Reserved
03F6h	IDE0 Controller
03F8h-03FFh	COM1 (Default)

This product utilizes a LPC to ISA Bridge to address the PC/104 bus. The majority of legacy PC/104 modules are I/O mapped and function as expected. However, neither DMA nor memory mapped PC/104 modules are supported with this product. The PC/104-*Plus* PCI signals are completely supported.

*** The ICH8M limits the LPC (ISA) decode ranges to four windows, two of which can be adjusted in the BIOS. For example, the 0300-033Fh range can be changed to 0600-06FFh so the full 256 bytes are available for PC/104 modules. Resources addressed internally may still exist in these ranges so please check the I/O map for availability.**

The advanced watchdog timer is the only on-board device affected by adjusting LPC (ISA) decode range. It will not be available if the 0564-0568h decode range is disabled.

The default is for the PC/104 decode ranges are shown below. Please contact an Applications Engineer if you have questions regarding the decode ranges.

0100-013Fh 64 Bytes (Fixed)

0200-02FFh 256 Bytes (Fixed)

0300-033Fh 64 Bytes (BIOS Selectable)

0500-05FFh 256 Bytes (BIOS Selectable)

Interrupt Map

Hardware Interrupts (IRQs) are supported for both PC/104 (ISA), PCI and PCIe devices. The user must reserve IRQs in the BIOS CMOS configuration for use by legacy devices. The PCIe/PnP BIOS will use unreserved IRQs when allocating resources during the boot process. The table below lists IRQ resources as used by the PXM-C388-S.

IRQ0	18.2 Hz heartbeat
IRQ1	Keyboard
IRQ2	Chained to Slave controller (IRQ9)
IRQ3	COM2 *
IRQ4	COM1 *
IRQ5	COM3 *
IRQ6	COM4 *
IRQ7	LPT *
IRQ8	Real Time Clock
IRQ9	FREE **
IRQ10	Digital I/O
IRQ11	PCI Interrupts
IRQ12	Mouse
IRQ13	Floating point processor
IRQ14	IDE
IRQ15	IDE

*	These IRQ references are default settings that can be changed by the user in the CMOS Settings utility. Reference the Super I/O Control section under Intel.
**	IRQ9 is commonly used by ACPI when enabled and may be unavailable (depending on operating system) for other uses.
***	IRQ15 is currently unavailable under the Windows operating systems.
Some IRQs can be freed for other uses if the hardware features they are assigned to are not being used. To free an interrupt, use the CMOS setup screens to disable any unused board features or their IRQ assignments.	

Interrupt Status Register - 29CH

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	N/A	N/A	N/A	COM4	COM3	COM2	COM1

Note: A **1** will be read for the device(s) with an interrupt pending.

WinSystems does not provide software support for implementing the Interrupt Status Register to share interrupts. Some operating systems, such as Windows XP and Linux, have support for sharing serial port interrupts and examples are available. The user will need to implement the appropriate software to share interrupts for the other devices.

Watchdog Timer

The PXM-C388 features an advanced watchdog timer which can be used to guard against software lockups. Two interfaces are provided to the watchdog timer. The Advanced interface is the most flexible and recommended for new designs. The other interface option is provided for software compatibility with older WinSystems single board computers.

Advanced

The watchdog timer can be enabled in the BIOS Settings by entering a value for Watchdog Timeout on the Intel → Super I/O Control screen. Any non-zero value represents the number of minutes prior to reset during system boot. Once the operating system is loaded, the watchdog can be disabled or reconfigured in the application software.

NOTE: It is recommended that a long timeout be used if the watchdog is enabled when trying to boot any operating system.

The watchdog can be enabled, disabled or reset by writing the appropriate values to the configuration registers located at I/O addresses 565h and 566h. The watchdog is enabled by writing a timeout value other than zero to the I/O address 566h and disabled by writing **00h** to this I/O address. The watchdog timer is serviced by writing the desired timeout value to I/O port 566h. If the watchdog has not been serviced within the allotted time, the circuit resets the CPU.

The timeout value can be set from 1 second to 255 minutes. If port 565h bit 7 equals **0**, the timeout value written into I/O address 566h is in minutes. The timeout value written to address 566h is in seconds if port 565 bit 7 equals **1**.

Watchdog Timer Examples

Port Address	Port Bit 7 Value	Port Address	Value	Reset Interval
565H	x	566H	00h	DISABLED
565H	1	566H	03h	3 SECONDS
565H	1	566H	1Eh	30 SECONDS
565H	0	566H	04h	4 MINUTES
565H	0	566H	05h	5 MINUTES

Software watchdog timer PET = PORT 566H, write the timeout value.

Real-Time Clock/Calendar

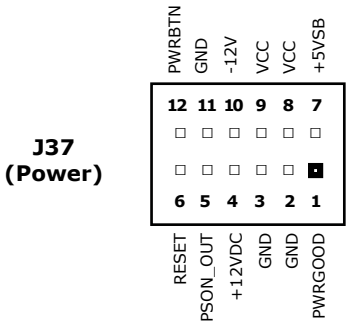
A real-time clock is used as the AT-compatible clock/calendar. It supports a number of features including periodic and alarm interrupt capabilities. In addition to the time and date keeping functions, the system configuration is kept in CMOS RAM contained within the clock section. A battery must be enabled for the real-time clock to retain time and date during a power down.

POWER

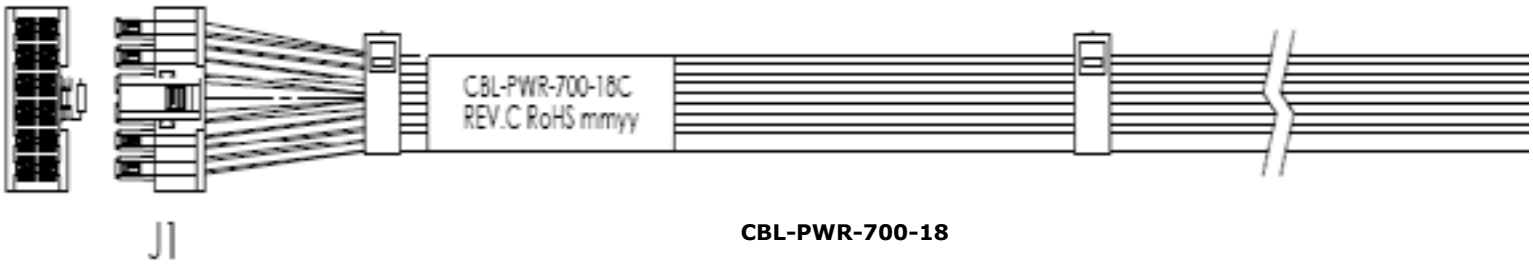
J37 - Power

Visual Index

PCB Connector: SAMTEC IPL1-105-01-L-D-RA-K (J37)
Mating Connector: SAMTEC IPD1-06-D-K (Housing)
SAMTEC CC79L-2024-01L or CC79R-2024-01L (Crimp)



Power is applied to the PXM-C388 via the connector at **J37**. WinSystems offers the cable CBL-PWR-700-18 to simplify this connection. See the list of Cables in this manual for additional cables for other power supplies.



CBL-PWR-700-18

JP14 - Power Supply Selection

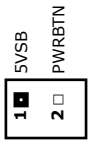
Visual Index

The PXM-C388 supports either AT (standard power supply) or ATX type power supplies. Zero load supplies are recommended. An AT power supply is a simple on/off supply with no interaction with the single board computer. Most embedded systems use this type of power supply and it is the default setting. **JP14** should always be jumpered with an AT style power supply and **+5V should be connected to both VCC and +5VSB** (jumper **JP15** on Rev. B and later).

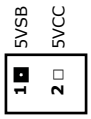
ATX type power supplies function with a “soft” on/off power button and a +5 VSB (standby). If an ATX compatible power supply is connected, **JP14** and **JP15** should be open and a power button (momentary contact) connected between pin 12 (power button) and pin 11 (ground) of **J37**. The +5 VSB signal provides the standby voltage to the PXM-C388 but does not power any other features of the board. When the power button is pressed, the PXM-C388 pulls PSON (Power Supply On) low and the power supply turns on all voltages to the single board computer. When the power button is pressed again, the BIOS signals the event so ACPI-compliant operating systems can be shutdown before the power is turned off. In ATX mode, if the power button is held for 4 seconds, the power supply is forced off, regardless of ACPI.

It is possible to use an ATX power supply without a power button. Simply jumper **JP14** and it will boot when the supply is turned on.

JP14



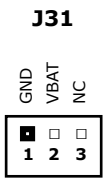
JP15 (Rev. B and later)



J31 - External Battery

Visual Index

PCB Connector: **MOLEX 501953-0307 (J31)**



(For external battery. Provides battery backup to RTC and BIOS CMOS.)

WARNING: BAT-LTC-E-36-16-2 or BAT-LTC-E-36-27-2 must be connected at J31. Improper installation of the battery could result in explosive failure. Please be careful to note correct connection at location J31.

An optional external battery, connected at **J31**, supplies the PXM-C388 board with standby power for the real-time clock and CMOS setup RAM. An extended temperature lithium battery is available from WinSystems, part number BAT-LTC-E-36-16-2 or BAT-LTC-E-36-27-2.

A power supervisory circuit contains the voltage sensing circuit and an internal power switch to route the battery or standby voltage to the circuits selected for backup. The battery automatically switches ON when the VCC of the systems drops below the battery voltage and back OFF again when VCC returns to normal.

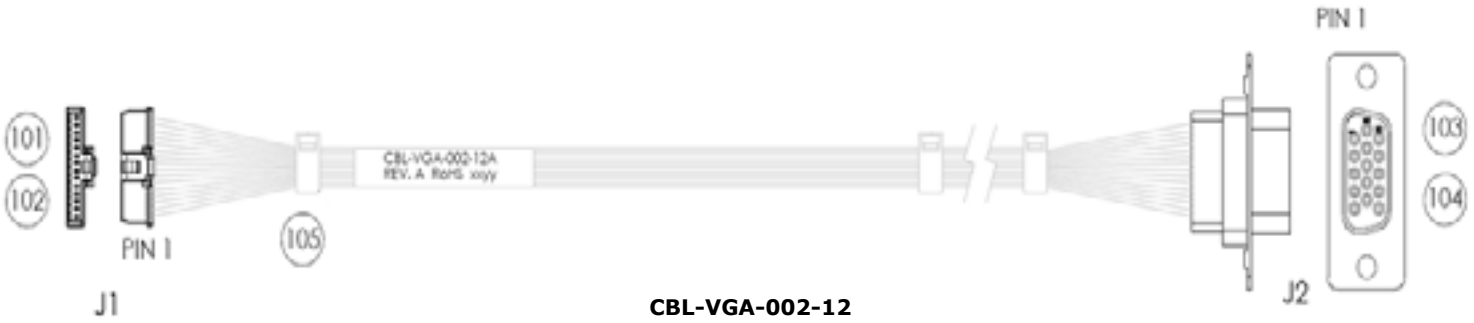
J33 - ANALOG VGA

Visual Index

PCB Connector: **MOLEX 501568-1407 (J33)**
Mating Connector: **MOLEX 501330-1400 (Housing)**
MOLEX 501334-0000 (Crimp)

J33

RED	1
GND	2
GREEN	3
GND	4
BLUE	5
GND	6
HSYNC	7
GND	8
VSYNC	9
GND	10
DDCDATA	11
N/C	12
DDCCLK	13
VCC	14



CBL-VGA-002-12

The PXM-C388-S has an integrated display controller that interfaces to both Analog VGA and flat panel displays. The video output mode is selected in the CMOS setup. Simultaneous flat panel and Analog VGA mode is also supported. The Analog VGA connector is located at **J33**. WinSystems offers the cable CBL-VGA-002-12 to simplify the connection. The LVDS interface connector is located at **J20** to interface to flat panels. A backlight power connectors is located at **J24.** Panel power option selection is made at **JP13**.

Contact your WinSystems' Applications Engineer for information about available cable kits and supported panels.
This manual does not attempt to provide any information about how to connect to specific LCDs.

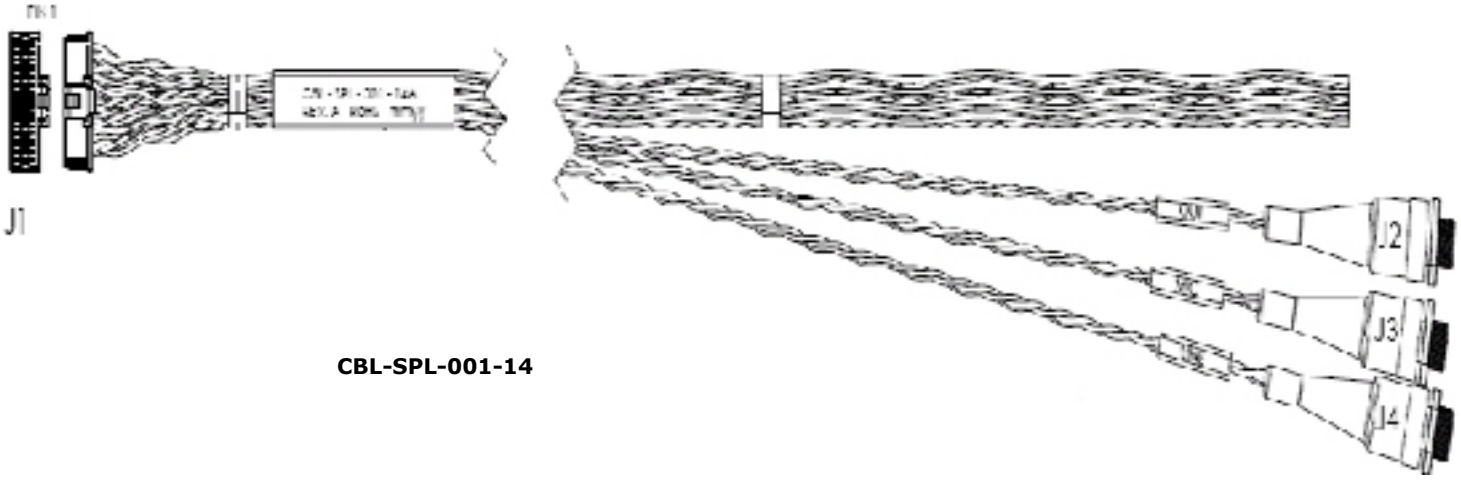
J20 - LVDS

PCB Connector: MOLEX 501571-4007 (J20)
Mating Connector: MOLEX 501189-3010 (Housing)
MOLEX 501193-2000 (Crimp)

J20

SWVDD (LVDS)	1	2	GND (LVDS)
D0- (LVDS)	3	4	D0+ (LVDS)
D1- (LVDS)	5	6	D1+ (LVDS)
SWVDD (LVDS)	7	8	GND (LVDS)
D2- (LVDS)	9	10	D2+ (LVDS)
NC (LVDS)	11	12	NC (LVDS)
SWVDD (LVDS)	13	14	GND (LVDS)
CLK-(LVDS)	15	16	CLK+ (LVDS)
DDC_CLK (LVDS)	17	18	GND (LVDS)
DDC_DATA (LVDS)	19	20	GND (LVDS)
GND (LVDS)	21	22	ANALOG_GND (AUDIO)
OUT_R (AUDIO)	23	24	MIC_R (AUDIO)
OUT-L (AUDIO)	25	26	MIC_L (AUDIO)
ANALOG_GND (AUDIO)	27	28	ANALOG_GND (AUDIO)
LINE_R (AUDIO)	29	30	LINE_L (AUDIO)

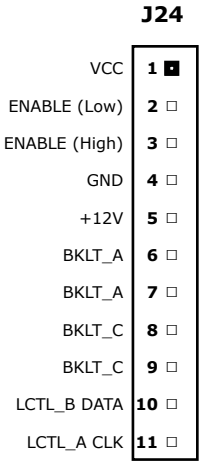
LVDS connection is provided at **J20**. WinSystems provides cable CBL-SPL-001-14 to adapt to this connector. The native resolution of the LCD Panel is configured in the BIOS.



CBL-SPL-001-14

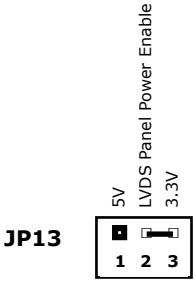
J24 - Backlight Power

PCB Connector: MOLEX 501131-1107 (J24)
Mating Connector: MOLEX 501330-1100 (Housing)
MOLEX 501334-0000 (Crimp)



HAZARD WARNING: LCD panels can require a high voltage for the panel backlight. This high-frequency voltage can exceed 1000 volts and can present a shock hazard. Care should be taken when wiring and handling the inverter output. To avoid the danger of shock and to avoid the panel, make all connection changes with the power removed.

JP13 - LVDS Power



Panel power option selection is made at **JP13**. **JP13** sets the voltage supply on V_{DD} of the LVDS connector **J20** to either +3.3V (default) or +5V.

J20 - Audio

Visual Index

PCB Connector: **MOLEX 501571-4007 (J20)**
Mating Connector: **MOLEX 501189-4010 (Housing)**
MOLEX 501193-2000 (Crimp)

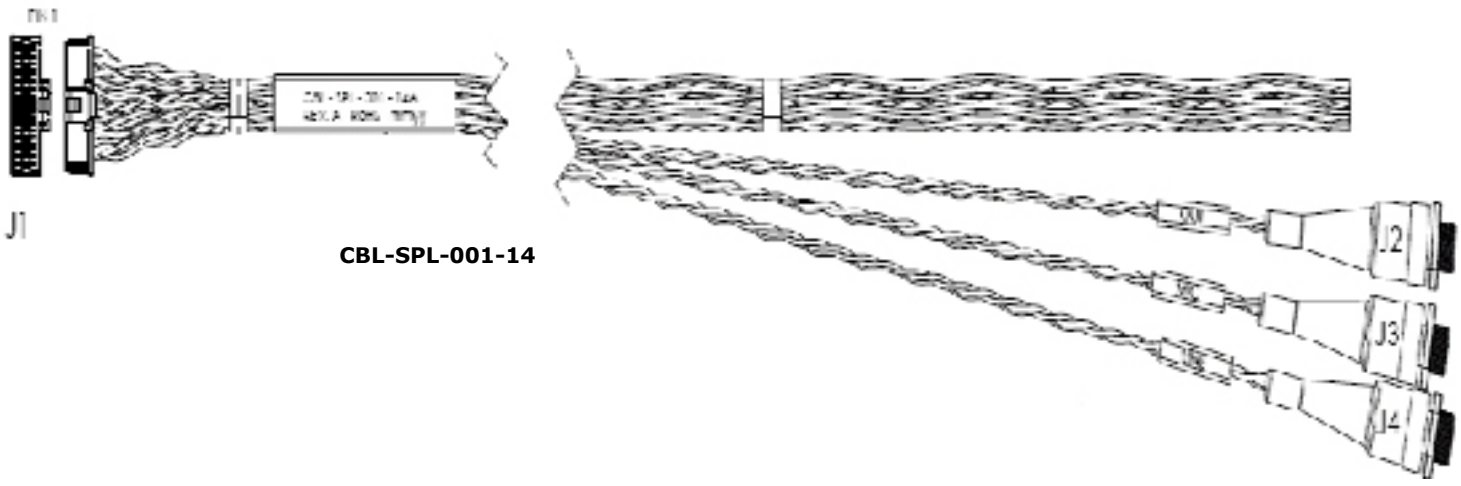
J20

SWVDD (LVDS)	1	2	GND (LVDS)
D0- (LVDS)	3	4	D0+ (LVDS)
D1- (LVDS)	5	6	D1+ (LVDS)
SWVDD (LVDS)	7	8	GND (LVDS)
D2- (LVDS)	9	10	D2+ (LVDS)
NC (LVDS)	11	12	NC (LVDS)
SWVDD (LVDS)	13	14	GND (LVDS)
CLK-(LVDS)	15	16	CLK+ (LVDS)
DDC_CLK (LVDS)	17	18	GND (LVDS)
DDC_DATA (LVDS)	19	20	GND (LVDS)
GND (LVDS)	21	22	ANALOG_GND (AUDIO)
OUT_R (AUDIO)	23	24	MIC_R (AUDIO)
OUT-L (AUDIO)	25	26	MIC_L (AUDIO)
ANALOG_GND (AUDIO)	27	28	ANALOG_GND (AUDIO)
LINE_R (AUDIO)	29	30	LINE_L (AUDIO)

Audio External Connection

The Intel HD Audio controller is included with a Realtek ALC886 codec.

Audio connection is provided at **J20**. WinSystems provides cable CBL-SPL-001-14 to adapt to this connector.



CBL-SPL-001-14

BZ1 - Speaker

Speaker

An on-board speaker, **BZ1**, is available for sound generation.

Beep Codes

Reference the chart Appendix-B section of this manual for the appropriate beep codes.

J34 - COM1, COM2, COM3, COM4

Visual Index

PCB Connector: MOLEX 502046-4070 (J34)
Mating Connector: MOLEX 503110-4000 (Housing)
MOLEX 501930-1100 (Crimp)

J34

GND	40	39	GND
RI (COM4)	38	37	DTR (COM4)
CTS (COM4)	36	35	TXD (COM4)
RTS (COM4)	34	33	RXD (COM4)
DSR (COM4)	32	31	DCD (COM4)
GND	30	29	GND
RI (COM3)	28	27	DTR (COM3)
CTS (COM3)	26	25	TXD (COM3)
RTS (COM3)	24	23	RXD (COM3)
DSR (COM3)	22	21	DCD (COM3)
GND	20	19	GND
RI (COM2)	18	17	DTR (COM2)
CTS (COM2)	16	15	TXD (COM2)
RTS (COM2)	14	13	RXD (COM2)
DSR (COM2)	12	11	DCD (COM2)
GND	10	9	GND
RI (COM1)	8	7	DTR (COM1)
CTS (COM1)	6	5	TXD (COM1)
RTS (COM1)	4	3	RXD (COM1)
DSR (COM1)	2	1	DCD (COM1)

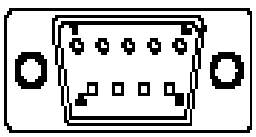
Four independent, asynchronous serial channels are on-board. Interface is provided at connector **J34**. WinSystems offers the cable CBL-SER4-002-12 to simplify the connection.

All serial ports are configured as Data Terminal Equipment (DTE). Both the send and receive registers of each port have a 16-byte FIFO. All serial ports have 16C550-compatible UARTs. The RS-232 transceivers have charge pumps to generate the plus and minus voltages so the PXM-C388 only requires +5V to operate.

Each port is setup to provide internal diagnostics such as loopback and echo mode on the data stream. An independent, software programmable baud rate generator is selectable from 50 through 115.2 kbps. Individual modem handshake control signals are supported for all ports.

RS-232 interface levels are supported on all four serial ports which can be enabled in the BIOS. COM1 and COM2 also have RS-422/RS-485 support.

COM1, COM2, COM3, COM4 [DB9 Male]



Pin	RS-232	RS-422	RS-485
1	DCD	N/A	N/A
2	RX	TX+	TX/RX+
3	TX	TX-	TX/RX-
4	DTR	N/A	N/A
5	GND	GND	GND
6	DSR	RX+	N/A
7	RTS	RX-	N/A
8	CTR	N/A	N/A
9	RI	N/A	N/A

COM1 and COM2 Configuration Options in BIOS

1. RS-232 Mode
2. RS-422 Mode with RTS transmitter enable
3. RS-422 Mode with auto transmitter enable
4. RS-485 Mode with RTS transmitter enable
5. RS-485 Mode with RTS transmitter enable and echo back
6. RS-485 Mode with auto transmitter enable
7. RS-485 Mode with auto transmitter enable and echo back

Mode(s)	Configuration Note
2, 4, 5	Require the RTS bit (MCR Bit 1) to be set in order to transmit.
3, 6, 7	Require TX/RX(300) termination on one node.
4	Requires the RTS (MCR Bit 1) be de-asserted in order to receive.

J4, J5 - USB

Visual Index

PCB Connector: MOLEX 501571-2007 (J4, J5)
Mating Connector: MOLEX 501189-2010 (Housing)
MOLEX 501193-2000 (Crimp)

J5
USB (2/3/8/9)

USBPWR8	1	2		USBPWR9
D8-	3	4		D9-
D8+	5	6		D9+
GND	7	8		GND
GND	9	10		GND
GND	11	12		GND
USBPWR2	13	14		USBPWR3
D2-	15	16		D3-
D2+	17	18		D3+
GND	19	20		GND

J4
USB (4/5/6/7)

USBPWR4	1	2		USBPWR5
D4-	3	4		D5-
D4+	5	6		D5+
GND	7	8		GND
GND	9	10		GND
GND	11	12		GND
USBPWR6	13	14		USBPWR7
D6-	15	16		D7-
D6+	17	18		D7+
GND	19	20		GND

CBL-USB4-002-12 with ADP-I0-USB-002

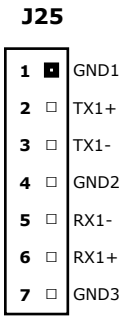
Up to two USB cables may be attached to the PXM-C388 via the connectors for a total of eight USB 2.0 ports. These are terminated to 20-pin connector at **J4** and **J5**. An adapter cable CBL-USB4-002-12 is available from WinSystems for connection along with ADP-IO-USB-002. Two additional USB channels are routed to the SUMIT-A bus connector.

SERIAL ATA

J25 - SATA

Visual Index

PCB Connector: **MOLEX 47080-4001 (J25)**



The PXM-C388 supports one SATA interface located at **J25**.

COMPACTFLASH

J28 - CompactFlash

Visual Index

When using a CompactFlash device, the device is set to Master. The PXM-C388 supports solid state CompactFlash storage devices for applications where the environment is too harsh for mechanical hard disks.

The CompactFlash socket at **J28** supports modules with TrueIDE support. WinSystems offers industrial grade CompactFlash modules that provide high performance and extended temperature operation (-40ºC to +85ºC).

STATUS LED

D53 - CompactFlash and SATA Activity

Visual Index

A status activity LED is located at **D53** on the PXM-C388.

D55 - 3.3 VSB Present

Visual Index

An 3VSB Present LED is located at **D55** on the PXM-C388.

D6 - User LED

Visual Index

A user LED is populated on the board at **D6** which can be used for any application specific purpose. The LED can be turned on in software applications by writing a **1** to I/O port 29DH. The LED can be turned off by writing a **0** to 29DH.

J35 - Gigabit Ethernet

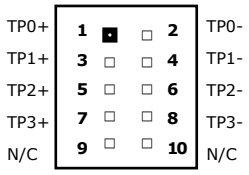
Visual Index

PCB Connector: SAMTEC TFM-105-02-L-DH (J35)
Mating Connector: SAMTEC ISDF-05-D-M (Housing)
SAMTEC CC03L-2830-01-G or CC03R-2830-01-G (Crimp)

Gigabit Ethernet Controllers

The PXM-C388 is equipped with an Intel Gigabit Ethernet controller, using the controller inside the ICH8M. This provides a standard IEEE 802.3 Ethernet interface for 1000/100/10BASE-T networks. The RJ-45 connection for the Ethernet port is available at **J35**.

J35



CBL-ENET1-302-12

J36 - Ethernet LED

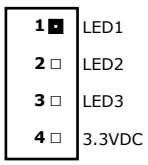
Visual Index

PCB Connector: MOLEX 501953-0307 (J36)
Mating Connector: MOLEX 501939-0400 (Housing)
MOLEX 501334 (Crimp)

Ethernet LED

On-board Ethernet activity signals are provided at **J36**. These activity signals are also available off-board for enclosures or other applications that have remote mounting requirements. See the pin definition below.

J36



J36
(Gigabit Ethernet Controller)

Pin	LED	Signal
1	**LED1**	ACTIVITY
2	**LED2**	SPEED1000
3	**LED3**	SPEED100
4	-	+3V

CBL-LED3-000-14

J9 - GPIO

Visual Index

PCB Connector: MOLEX 501571-5007
Mating Connector: MOLEX 501189-5010 (Housing)
MOLEX 501193-2000 (Crimp)

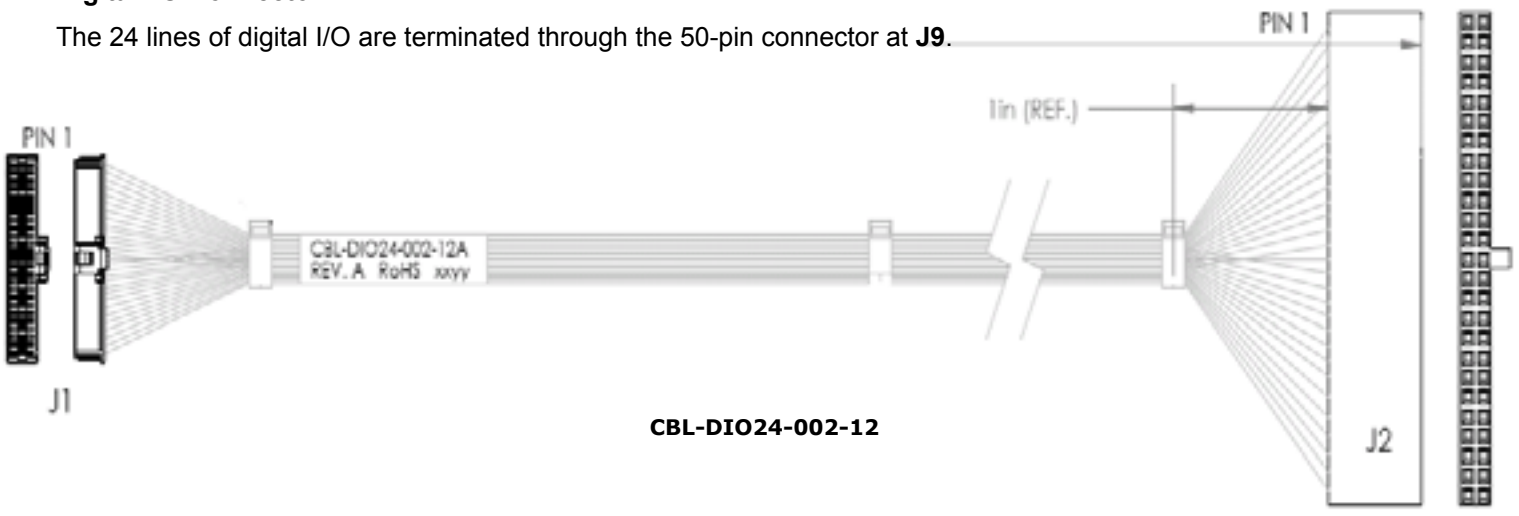
J9
(Ports 0/1/2)

Port 2 Bit 7	1	2	GND
Port 2 Bit 6	3	4	GND
Port 2 Bit 5	5	6	GND
Port 2 Bit 4	7	8	GND
Port 2 Bit 3	9	10	GND
Port 2 Bit 2	11	12	GND
Port 2 Bit 1	13	14	GND
Port 2 Bit 0	15	16	GND
Port 1 Bit 7	17	18	GND
Port 1 Bit 6	19	20	GND
Port 1 Bit 5	21	22	GND
Port 1 Bit 4	23	24	GND
Port 1 Bit 3	25	26	GND
Port 1 Bit 2	27	28	GND
Port 1 Bit 1	29	30	GND
Port 1 Bit 0	31	32	GND
Port 0 Bit 7	33	34	GND
Port 0 Bit 6	35	36	GND
Port 0 Bit 5	37	38	GND
Port 0 Bit 4	39	40	GND
Port 0 Bit 3	41	42	GND
Port 0 Bit 2	43	44	GND
Port 0 Bit 1	45	46	GND
Port 0 Bit 0	47	48	GND
+5V	49	50	GND

The PXM-C388 has 24 open collector digital I/O bits with a default base address of 120H. Each bit is configured as an open collector with a 10K pullup. Each bit is able to sink up to 8 mA. The first 24 lines are capable of fully latched event sensing with polarity being software programmable.

Digital I/O Connector

The 24 lines of digital I/O are terminated through the 50-pin connector at **J9**.



CBL-DIO24-002-12

Register Definitions (WS16C48)

The PXM-C388 uses the WinSystems exclusive ASIC device, the WS16C48. This device provides 48 lines of digital I/O. There are 16 unique registers within the WS16C48. The following table summarizes the registers, and the text that follows provides details on each of the internal registers.

I/O Address Offset	Page 0	Page 1	Page 2	Page 3
00H	Port 0 I/O	Port 0 I/O	Port 0 I/O	Port 0 I/O
01H	Port 1 I/O	Port 1 I/O	Port 1 I/O	Port 1 I/O
02H	Port 2 I/O	Port 2 I/O	Port 2 I/O	Port 2 I/O
03H	Port 3 I/O	Port 3 I/O	Port 3 I/O	Port 3 I/O
04H	Port 4 I/O	Port 4 I/O	Port 4 I/O	Port 4 I/O
05H	Port 5 I/O	Port 5 I/O	Port 5 I/O	Port 5 I/O
06H	Int_Pending	Int_Pending	Int_Pending	Int_Pending
07H	Page/Lock	Page/Lock	Page/Lock	Page/Lock
08H	Reserved	Pol_0	Enab_0	Int_ID0
09H	Reserved	Pol_1	Enab_1	Int_ID1
0AH	Reserved	Pol_2	Enab_2	Int_ID2

Register Details

Port 0 through 5 I/O

Each I/O bit in each of the six ports can be individually programmed for input or output. Writing a **0** to a bit position causes the corresponding output pin to go to a high-impedance state (pulled high by external 10 KΩ resistors). This allows it to be used as an input. When used in the input mode, a read reflects the inverted state of the I/O pin, such that a high on the pin will read as a **0** in the register. Writing a **1** to a bit position causes that output pin to sink current (up to 12 mA), effectively pulling it low.

INT_PENDING

This read-only register reflects the combined state of the INT_ID0 through INT_ID2 registers. When any of the lower three bits are set, it indicates that an interrupt is pending on the I/O port corresponding to the bit position(s) that are set. Reading this register allows an Interrupt Service Routine to quickly determine if any interrupts are pending and which I/O port has a pending interrupt.

PAGE/LOCK

This register serves two purposes. The upper two bits select the register page in use as shown here:

D7	D6	Page
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

Bits 5-0 allow for locking the I/O ports. A **1** written to the I/O port position will prohibit further writes to the corresponding I/O port.

POL0 - POL2

These registers are accessible when Page 1 is selected. They allow interrupt polarity selection on a port–by–port and bit-by-bit basis. Writing a **1** to a bit position selects the rising edge detection interrupts while writing a **0** to a bit position selects falling edge detection interrupts.

ENAB0 - ENAB2

These registers are accessible when Page 2 is selected. They allow for port-by-port and bit-by-bit enabling of the edge detection interrupts. When set to a **1**, the edge detection interrupt is enabled for the corresponding port and bit. When cleared to **0**, the bit's edge detection interrupt is disabled. Note that this register can be used to individually clear a pending interrupt by disabling and re-enabling the pending interrupt.

INT_ID0 – INT_ID2

These registers are accessible when Page 3 is selected. They are used to identify currently pending edge interrupts. A bit when read as a **1** indicates that an edge of the polarity programmed into the corresponding polarity register has been recognized. Note that a write to this register (value ignored) clears ALL of the pending interrupts in this register.

J17A, J17B - PC/104

Visual Index

PCB Connector: **TEKA PC232-A-1BD-M (J17A)**
TEKA PC220-A-1BD-M (J17B)

The PC/104 bus is electrically equivalent to the 16-bit ISA bus. Standard PC/104 I/O cards can be populated on PXM-C388's connectors, located at **J17A** and **J17B**. The interface does not support hot swap capability. The PC/104 bus connector pin definitions are provided below for reference. Refer to the PC/104 Bus Specification for specific signal and mechanical specifications.

J17B (C/D)

GND	**D0**	**C0**	GND
MEMCS16#	**D1**	**C1**	SBHE#
IOCS16#	**D2**	**C2**	LA23
IRQ10	**D3**	**C3**	LA22
IRQ11	**D4**	**C4**	LA21
IRQ12	**D5**	**C5**	LA20
IRQ15	**D6**	**C6**	LA19
IRQ14	**D7**	**C7**	LA18
DACK0#	**D8**	**C8**	LA17
DRQ0	**D9**	**C9**	MEMR#
DACK5#	**D10**	**C10**	MEMW#
DRQ5	**D11**	**C11**	SD8
DACK6#	**D12**	**C12**	SB9
DRQ6	**D13**	**C13**	SD10
DACK7#	**D14**	**C14**	SD11
DRQ7	**D15**	**C15**	SD12
+5V	**D16**	**C16**	SD13
MASTER#	**D17**	**C17**	SD14
GND	**D18**	**C18**	SD15
GND	**D19**	**C19**	KEY

J17A (A/B)

IOCHK#	**A1**	**B1**	GND
SD7	**A2**	**B2**	RESET
SD6	**A3**	**B3**	+5V
SD5	**A4**	**B4**	IRQ
SD4	**A5**	**B5**	-5V
SD3	**A6**	**B6**	DRQ2
SD2	**A7**	**B7**	-12V
SD1	**A8**	**B8**	SRDY#
SD0	**A9**	**B9**	+12V
IOCHRDY	**A10**	**B10**	KEY
AEN	**A11**	**B11**	SMEMW#
SA19	**A12**	**B12**	SMEMR#
SA18	**A13**	**B13**	IOW#
SA17	**A14**	**B14**	IOR#
SA16	**A15**	**B15**	DACK3#
SA15	**A16**	**B16**	DRQ3
SA14	**A17**	**B17**	DACK1#
SA13	**A18**	**B18**	DRQ1
SA12	**A19**	**B19**	REFRESH#
SA11	**A20**	**B20**	BCLK
SA10	**A21**	**B21**	IRQ7
SA9	**A22**	**B22**	IRQ6
SA8	**A23**	**B23**	IRQ5
SA7	**A24**	**B24**	IRQ4
SA6	**A25**	**B25**	IRQ3
SA5	**A26**	**B26**	DACK2#
SA4	**A27**	**B27**	TC
SA3	**A28**	**B28**	BALE
SA2	**A29**	**B29**	+5V
SA1	**A30**	**B30**	OSC
SA0	**A31**	**B31**	GND
GND	**A32**	**B32**	GND

= Active Low Signal

NOTES:

1. Rows C and D are not required on 8-bit modules.
2. B10 and C19 are key locations. WinSystems uses key pins as connections to GND.
3. Signal timing and function are as specified in ISA specification.
4. Signal source/sink current differ from ISA values.

J29, J30 - SUMIT

Visual Index

PCB Connector: **SAMTEC ASP-129637-01**

J29

5V	1	2		12V
3.3V_1	3	4		SMB_DATA
3.3V_2	5	6		SMB_CLK
EXPCD_REQ#	7	8		SMB_ALERT
EXPCD_PRSNT#	9	10		SPI_DO
USB_OC#0/1	11	12		SPI_DI
USB_OC#0/1	13	14		SPI_CLK
5V_2	15	16		SPI_CS0
USB3+	17	18		SPI_CS1
USB3-	19	20		RESERVED_5
5V_3	21	22		LPC_DRQ
USB2+	23	24		LPC_AD0
USB2-	25	26		LPC_AD1
5V_4	27	28		LPC_AD2
USB1+	29	30		LPC_AD3
USB1-	31	32		LPC_FRAME#
5V_5	33	34		SERIRQ#
USB0+	35	36		LPC_PRSNT#/GND
USB0-	37	38		CLK_33MHz
GND_1	39	40		GND_3
A_PETp0	41	42		A_PERp0
A_PETn0	43	44		A_PERn0
GND_2	45	46		APRSNT
PERST#	47	48		A_CLKp
WAKE#	49	50		A_CLKn
5V_6	51	52		GND_4

J30

5V	1	2		GND
B_PETp0	3	4		B_PERp0
B_PETn0	5	6		B_PERn0
GND	7	8		BPRST#/GND
C_CLKp	9	10		B_CLKp
C_CLKn	11	12		B_CLKn
CPRSNT#/GND	13	14		GND
C_PETp0	15	16		C_PERp0
C_PETn0	17	18		C_PERn0
GND_2	19	20		GND
C_PETp1	21	22		C_PERp1
C_PETn1	23	24		C_PERn1
GND	25	26		GND
C_PETp2	27	28		C_PERp2
C_PETn2	29	30		C_PERn2
GND_3	31	32		GND
C_PETp3	33	34		C_PERp3
C_PETn3	35	36		C_PERn3
GND_4	37	38		GND
PERST#	39	40		WAKE#
RESERVED	41	42		RESERVED
5V_2	43	44		RESERVED
RV_3	45	46		3.3V
5V_4	47	48		3.3V_2
5V_5	49	50		3.3V_3
5V_6	51	52		5V_7

The PXM-C388 has a SUMIT-A connector which allows for multiple I/O modules to be stacked on top of a host module. SUMIT-A is located at **J29**. A second SUMIT-B connector, located at **J30**. Their pinouts for **J29** and **J30** are listed above. Refer to the SUMIT Specification for more information on the SUMIT Interface.

BIOS SUPPLEMENTAL

General Information

The PXM-C388 includes BIOS from Phoenix Technologies to assure full compatibility with PC operating systems and software. The basic system configuration is stored in battery backed CMOS RAM within the clock/calendar. As an alternative, the CMOS configuration may be stored in EEPROM for operation without a battery. For more information of CMOS configuration, see the BIOS Settings Storage Options section of this manual. Access to this setup information is via the Setup Utility in the BIOS.

Entering Setup

To enter setup, power up the computer and press **F2** when either the splash screen is displayed or when the **Press F2 for Setup** message is displayed. It may take a few seconds before the main setup menu screen is displayed.

Navigation of the Menus

Use the **Up** and **Down** arrow keys to move among the selections and press **Enter** when a selection is highlighted to enter a sub-menu or to see a list of choices. Following are images of each menu screen in the default configuration along with a brief description of each option where applicable. Available options are listed in reference tables. Menu values shown in **bold** typeface are factory defaults.

BIOS Splash Screen

Custom BIOS Splash Screens can be accommodated for OEM customers. Please contact one of our Application Engineers for details.

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Main Menu	
System Time:	**09:40:34**
System Date:	**04/09/2010**
>IDE Primary Master	**None**
>IDE Primary Slave	**None**
>SATA Port 1	**None**
>SATA Port 2	**None**
System Memory:	633 KB
Extended Memory:	2085888 KB
Ethernet MAC Address 1:	xx:xx:xx:xx:xx:xx
Ethernet MAC Address 2:	xx:xx:xx:xx:xx:xx
CPU Temperature:	50 °C/132 °F
Ambient Temperature:	40 °C/104 °F

Each available option is listed in detail in the following sections.

Navigation to the screens is located at the top of each screen's layout.

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Depending on the Primary Master **Type**, various Primary Master options will be available. See the following screens.

Main Menu > **IDE Primary Master/Slave [None]**	
Type:	**Auto**
Multi-Sector Transfers:	**Disabled**
LBA Mode Control:	**Disabled**
32 Bit I/O:	**Disabled**
Options: Disabled Enabled	
Transfer Mode:	**FPIO 4 / DMA 2**
Ultra DMA Mode:	**Disabled | (Mode 2 for IDE Primary Slave only)**
SMART Monitoring	**Disabled**

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Depending on the Primary Master **Type**, various Primary Master options will be available. See the following screens.

Main Menu > **SATA Port 1 / SATA Port 2**	
Type:	**Auto**
Multi-Sector Transfers:	**Disabled**
LBA Mode Control:	**Disabled**
32 Bit I/O:	**Disabled**
Options: Disabled Enabled	
Transfer Mode:	**Standard**
Ultra DMA Mode:	**Disabled**
SMART Monitoring	**Disabled**

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Advanced	
Installed O/S:	**Win95**
Options: Other Win95 Win98 WinMe Win2000	
Reset Configuration Data:	**No**
Options: No Yes	
Large Disk Access Mode:	**DOS**
Options: Other DOS	
Summary screen:	**Disabled**
Options: Disabled Enabled	
Boot-time Diagnostic Screen:	**Enabled**
Options: Disabled Enabled	
QuickBoot Mode:	**Enabled**
Options: Disabled Enabled	
Extended Memory Testing:	**None**
Options: Normal Just zero it None	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel
> CPU Control Sub-Menu
> Video (Intel IGD) Control Sub-Menu
> ICH Control Sub-Menu
> Super I/O Control Sub-Menu
> ACPI Control Sub-Menu

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > CPU Control Sub-Menu	
Hyperthreading:	**Enabled**
Options: Disabled Enabled	
Processor Power Management:	**Enabled**
Options: Disabled GV3 Only C-States Only Enabled	
Timestamp Counter Updates	**Enabled**
Options: Disabled Enabled	
> CPU Thermal Control Sub-Menu	
Set Max Ext CPUID = 3	**Disabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > CPU Control Sub-Menu > **CPU Thermal Control Sub-Menu**	
Thermal Control Circuit:	**Disabled**
Options: Disabled TM1 TM2 TM1 and TM2	
DTS Enable:	**Disabled**
Options: Disabled Enabled	
Active Trip Point:	**55 C**
Options: Disabled 55 C 63 C 71 C 79 C 87 C 95 C 103 C 111 C 119 C	
Passive Cooling Trip Point:	**95 C**
Options: Disabled 55 C 63 C 71 C 79 C 87 C 95 C 103 C 111 C 119 C	
Passive TC1 Value:	**1**
Passive TC2 Value:	**5**
Options: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	
More CPU Thermal Control Sub-Menu options are continued on the next page.	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > CPU Control Sub-Menu > CPU Thermal Control Sub-Menu (continued)

Passive TSP Value:	**10**
Options: 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150	
Critical Trip Point:	**POR**
Options: POR 15 C 23 C 31 C 39 C 47 C 55 C 63 C 71 C 79 C 87 C 95 C 103 C 111 C 119 C 127 C	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > **Video (Intel IGD) Control Sub-Menu**	
IGD - VBIOS Boot Type:	**CRT**
Options: VBT Default CRT LFP CRT+LFP	
> IGD - LCD Control Sub-Menu	
DVMT 4.0 Mode:	**Auto**
Options: Fixed DVMT Auto	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > Video (Intel IGD) Control Sub-Menu > **IGD - LCD Control Sub-Menu**	
IGD - LCD Panel Type:	**3: 1024x768 LVDS**
Options: 1: 640x480 LVDS 2: 800x600 LVDS 3: 1024x768 LVDS 4: 1280x1024 LVDS 5: 1400x1050LVDS1 6: 1400x1050 LVDS2 7: 1600x1200 LVDS 8: 1280x768 LVDS 9: 1680x1050 LVDS 10: 1920x1200 LVDS 11: Reserved 12: Reserved 13: Reserved 14: 1280X800 LVDS 15: 1280X600 LVDS 16: Reserved	
IGD - Panel Scaling:	**Auto**
Options: Auto Force Scaling Off	
GMCH BLC Control:	**GMBus**
Options: Disabled PWM GMBus	
BIA Control	**Disabled**
Options: Automatic Disabled Level 1 Level 2 Level 3 Level 4 Level 5	
Spread Spectrum Clock Chip:	**Off**
Options: Off Hardware Software	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > **ICH Control Sub-Menu**	
> Integrated Device Control Sub-Menu	
Serial IRQ Quiet Mode:	**Enabled**
Options: Disabled Enabled	
Pop Up Mode Enable:	**Enabled**
Options: Disabled Enabled	
Pop Down Mode Enable:	**Enabled**
Options: Disabled Enabled	
LPC Decode Range 1 Base Address:	**300h**
LPC Decode Range 1 Size:	**128 Bytes**
Options: 128 Bytes 64 Bytes 32 Bytes 16 Bytes 8 Bytes 4 Bytes	
LPC Decode Range 2 Base Address:	**500h**
LPC Decode Range 2 Size:	**256 Bytes**
Options: 256 Bytes 128 Bytes 64 Bytes 32 Bytes 16 Bytes 8 Bytes 4 Bytes	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > ICH Control Sub-Menu > **Integrated Device Control Sub-Menu**	
> PCI Express Control Sub-Menu	
> ICH USB Control Sub-Menu	
Azalia - Device 27, Function 0:	**Auto**
Options: Disabled Auto	
AHCI Configuration:	**Disabled**
Options: Disabled Enabled	
Disable Vacant Ports:	**Disabled**
Options: Disabled Enabled	
On-board LAN:	**Enabled**
Options: Disabled Enabled	
PXE OPROM:	**Disabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > ICH Control Sub-Menu > Integrated Device Control Sub-Menu > **PCI Express Control Sub-Menu**	
PCI Express - Root Port 1:	**Enabled**
Options: Disabled Enabled Auto	
PCI Express - Root Port 2:	**Auto**
Options: Disabled Enabled Auto	
Root Port ASPM Support:	**Auto**
Options: Disabled Auto	
ASPM Latency Checking:	**Auto**
Options: Disabled Auto	
> PCI/PNP ISA IRQ Resource Exclusion	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > ICH Control Sub-Menu > Integrated Device Control Sub-Menu > PCI Express Control Sub-Menu

PCI/PNP ISA IRQResource Exclusion

IRQ 3:	**Available**
Options: Available Reserved	
IRQ 4:	**Available**
Options: Available Reserved	
IRQ 5:	**Available**
Options: Available Reserved	
IRQ 7:	**Available**
Options: Available Reserved	
IRQ 9:	**Available**
Options: Available Reserved	
IRQ 10:	**Available**
Options: Available Reserved	
IRQ 11:	**Available**
Options: Available Reserved	
IRQ 15:	**Available**
Options: Available Reserved	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > ICH Control Sub-Menu > Integrated Device Control Sub-Menu > **ICH USB Control Sub-Menu**	
USB Dev #29	**Fun #0,1,2,7**
Options: Disabled Fun #0 Fun #0,1 Fun #0,1,2 Fun #0,1,2,7	
USB Dev #26	**Fun #0,1,7**
Options: Disabled Fun #0,7 Fun #0,1,7	
Overcurrent Detection	**Enabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > Super I/O Control Sub-Menu

Serial port 1:	**Enabled**
Speed:	**Low**
Base I/O address:	**3F8**
Interrupt:	**IRQ 4**
Interface:	**RS232**

Options:

Port x:	**Speed:**	**Base I/O address:**	**Interrupt:**	**Interface:**
Disabled	Low	3F8	Disabled	RS232
Enabled	High	2F8	IRQ 3	RS422 RTS
		3E8	IRQ 4	RS422 Auto
		2E8	IRQ 5	RS485 RTS
			IRQ 6	RS485 RTS w/Echo
			IRQ 7	RS485 Auto
			IRQ 9	RS485 Auto w/Echo

Serial port 2:	**Enabled**
Speed:	**Low**
Base I/O address:	**2F8**
Interrupt:	**IRQ 3**
Interface:	**RS232**

Options:

Port x:	**Speed:**	**Base I/O address:**	**Interrupt:**	**Interface:**
Disabled	Low	3F8	Disabled	RS232
Enabled	High	2F8	IRQ 3	RS422 RTS
		3E8	IRQ 4	RS422 Auto
		2E8	IRQ 5	RS485 RTS
			IRQ 6	RS485 RTS w/Echo
			IRQ 7	RS485 Auto
			IRQ 9	RS485 Auto w/Echo

Serial port 3:	**Enabled**
Speed:	**Low**
Base I/O address:	**3E8**
Interrupt:	**IRQ 5**
Interface:	**RS232**

Options:

Port x:	**Speed:**	**Base I/O address:**	**Interrupt:**	**Interface:**
Disabled	Low	3F8	Disabled	RS232
Enabled	High	2F8	IRQ 3	RS422 RTS
		3E8	IRQ 4	RS422 Auto
		2E8	IRQ 5	RS485 RTS
			IRQ 6	RS485 RTS w/Echo
			IRQ 7	RS485 Auto
				RS485 Auto w/Echo

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > Super I/O Control Sub-Menu (continued)

Serial port 4:		**Enabled**		
Speed:		**Low**		
Base I/O address:		**2E8**		
Interrupt:		**IRQ 6**		
Interface:		**RS232**		
Options:				
Port x: Disabled Enabled	**Speed:** Low High	**Base I/O address:** 3F8 2F8 3E8 2E8	**Interrupt:** Disabled IRQ 3 IRQ 4 IRQ 5 IRQ 6 IRQ 7	**Interface:** RS232 RS422 RTS RS422 Auto RS485 RTS RS485 RTS w/Echo RS485 Auto RS485 Auto w/Echo
Parallel port:		**Enabled**		
Base I/O address:		**378**		
Interrupt:		**IRQ 7**		
Options:				
Port x: Disabled Enabled		**Base I/O address:** 378 278	**Interrupt:** Disabled IRQ 3 IRQ 4 IRQ 5 IRQ 6 IRQ 7 IRQ 9 IRQ 10	
Digital I/O port:		**Enabled**		
DIO port address:		**120**		
DIO IRQ:		**IRQ 10**		
Options:				
Digital I/O port: Disabled Enabled	**DIO port address:** 120 130 140	**DIO IRQ:** Disabled IRQ 3 IRQ 4 IRQ 5 IRQ 6 IRQ 7 IRQ 9 IRQ 10		
Watchdog:		**0**		
Options: {Enter any value between 0-255 for seconds.}				
SIO Firmware:		Rev 0003		

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > **ACPI Control Sub-Menu**	
Passive Cooling Trip Point:	**55 C**
Options: Disabled 55 C 63 C 71 C 79 C 87 C 95 C 103 C 111 C 119 C	
Passive Cooling Trip Point:	**95 C**
Options: Disabled 55 C 63 C 71 C 79 C 87 C 95 C 103 C 111 C 119 C	
Passive TC1 Value:	**1**
Passive TC2 Value:	**5**
Options: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	
Passive TSP Value:	**10**
Options: 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > **ACPI Control Sub-Menu** (continued)	
Critical Trip Point:	**POR**
Options: POR 15 C 23 C 31 C 39 C 47 C 55 C 63 C 71 C 79 C 87 C 95 C 103 C 111 C 119 C 127 C	
FACP - RTC S4 Flag Value:	**Enabled**
Options: Disabled Enabled	
FACP - PM Timer Flag Value:	**Enabled**
Options: Disabled Enabled	
HPET Support:	**Disabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Security	
Supervisor Password Is:	Clear
User Password Is:	Clear
Set Supervisor Password:	**Enter**
Set User Password:	Enter
Virus check reminder:	**Disabled**
Options: Disabled Daily Weekly Monthly	
Password on boot:	Disabled
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Boot

Boot priority order:

1:
2:
3:
4:
5:
6:
7:
8:

Options:

Excluded from boot order:

Options:
All IDE HDD
All USB Floppy
All USB Key
All USB HDD
All USB CDROM
All USB ZIP
All USB LS120
All PCI SCSI
All PCI BEV
Legacy Network Card
Bootable Add-in Cards

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Exit
Exit Saving Changes
Exit Saving Changes to CMOS and EEPROM
Exit Discarding Changes
Load Setup Defaults
Discard Changes
Save Changes

BIOS SETTINGS STORAGE OPTIONS

CMOS Storage Locations

The PXM-C388's BIOS configuration is stored in three (3) locations:

(1) CMOS RAM (nonvolatile if battery backed)

(2) EEPROM (nonvolatile storage for user defaults)

(3) FLASH PROM (nonvolatile storage for factory defaults)

Saving the CMOS Configuration

The Real-Time Clock and the CMOS RAM settings can be maintained by an optional battery when the board is powered off. A battery is always required to maintain time and date functions when the board is powered off.

The EEPROM feature allows the user to save CMOS configuration settings to nonvolatile storage that does not require a battery. This feature can be enabled/disabled using **JP19**. When enabled, the user's CMOS settings can be saved to EEPROM from the BIOS utility's Main Menu. If the board is powered off with no battery, the user's CMOS settings will be restored from EEPROM but time and date information will be lost and returned to default values.

JP19 - EEPROM Enable

EEPROM Enable	JP19
CMOS EEPROM Enable (default)	1-2
CMOS EEPROM Disable	Open

At system boot, the BIOS first performs a checksum validation on the contents of the CMOS RAM. Invalid checksums usually occur due to a low or disabled battery. If the checksum is valid, the system boots using values stored in CMOS RAM. If a checksum error occurs, the BIOS attempts to load CMOS values from the EEPROM.

After a checksum validation, the BIOS configuration is loaded from the EEPROM and the boot process continues. If the EEPROM is disabled or the contents of the EEPROM fail the checksum validation, the system loads the factory default settings from the FLASH PROM and continues the boot sequence.

For applications where the battery is present, CMOS settings should be saved to both the CMOS RAM and to the EEPROM so the system can continue to function without user interaction.

Resetting CMOS to EEPROM defaults

If a battery is present, you can reset the CMOS RAM to the values stored in EEPROM by turning the system off and removing the external battery. Replace the battery and reboot. When power is applied to the board, the system will boot with the CMOS settings that were stored in EEPROM.

Resetting CMOS to EEPROM to Factory Defaults

The PXM-C388 can normally be returned to the factory default BIOS configuration by selecting option Load Setup Defaults on the BIOS Exit menu.

If you have saved EEPROM values that prevent you from accessing BIOS menus, the board can be reset to factory defaults as follows:

1) Turn the system off.
2) Remove the jumpers from **JP19**.
3) Turn the system on and enter the BIOS Main Menu using the **F2** key.
4) Select Load Defaults from the Exit menu.
5) Install the jumpers to **JP19**.
6) Save the restored defaults to CMOS and EEPROM.

Updating the BIOS FLASH PROM

The most recent PXM-C388 BIOS is available on the WinSystems website. However, it is highly recommended that an Applications Engineer be consulted prior to any BIOS FLASH PROM update. If the BIOS PROM is updated, the steps described above must be followed to reset the CMOS and EEPROM to the newly loaded factory defaults and to clear the data from the previous BIOS version.

CABLES

Part Number	Description
Additional Cables	
CBL-BKLT-000-14	Backlight 1x11 1-mm., Unterminated Pico-Clasp
CBL-DIO24-001-12	DIO 2x25, 1-mm. to 2x25 1-mm., 12-in.
CBL-DIO24-002-12	DIO Cable 2x25, 1-mm. to 2x25 .1 CNTRS, 12-in.
CBL-ENET1-302-12	ENET 2X5 1.27-mm. to RJ-45 Jack,12-in.
CBL-LED3-000-14	LED, Ethernet 1x4, 1-mm. Unterminated, 14-in.
CBL-LED3-001-12	LED, Ethernet 1x4, 1-mm. to 1x4 1-mm.
CBL-PWR-114-18	PCM-DC to PXM Power Cable
CBL-PWR-602-18	Auxiliary Power and Reset
CBL-PWR-700-18	Power ATX, 18-in. Unterminated
CBL-PWR-803-18	C388 to SDK Power Cable
CBL-PWR-903-18	ATX to SDK Power Cable
CBL-SATA-701-20	SATA, Latching, Mirror, Straight 20-in. long
CBL-SER4-000-14	Serial Cable 2x20, 1.25-mm. to Unterminated, 14-in.
CBL-SER4-001-12	Serial Cable 2x20, 1.25-mm. to 2x20 1.25-mm., 12-in.
CBL-SER4-002-12	Serial Cable 2x20, 1.25-mm. to 4EA DB9, 12-in.
CBL-SPL-001-14	LVDS Unterminated and Audio,PICO
CBL-USB4-000-14	4x USB ports - Unterminated
CBL-USB4-001-12	4x USB ports with 2x 15 pins with clasp
CBL-USB4-002-12	4x USB ports with two, 8-pin, 2-mm. clasps
CBL-VGA-002-12	Video 1x14 1-mm. to DB15, 12-in.
External Batteries	
BAT-LTC-E-36-16-2	External 3.6V, 1650 mAH battery with plug-in connector
BAT-LTC-E-36-27-2	External 3.6V, 2700 mAH battery with plug-in connector

SOFTWARE DRIVERS

Software Drivers	
Windows 7	PXMC388Windows7.zip
Windows XP SP3	PXMC388WindowsXP_SP3.zip
Linux Drivers - Kernel 2.6.18+ - WS16C48 Digital I/O	uio48io_kernel_2.6.18.zip
Linux Drivers - Kernel 2.6.36	uio48io_kernel_2.6.36.zip

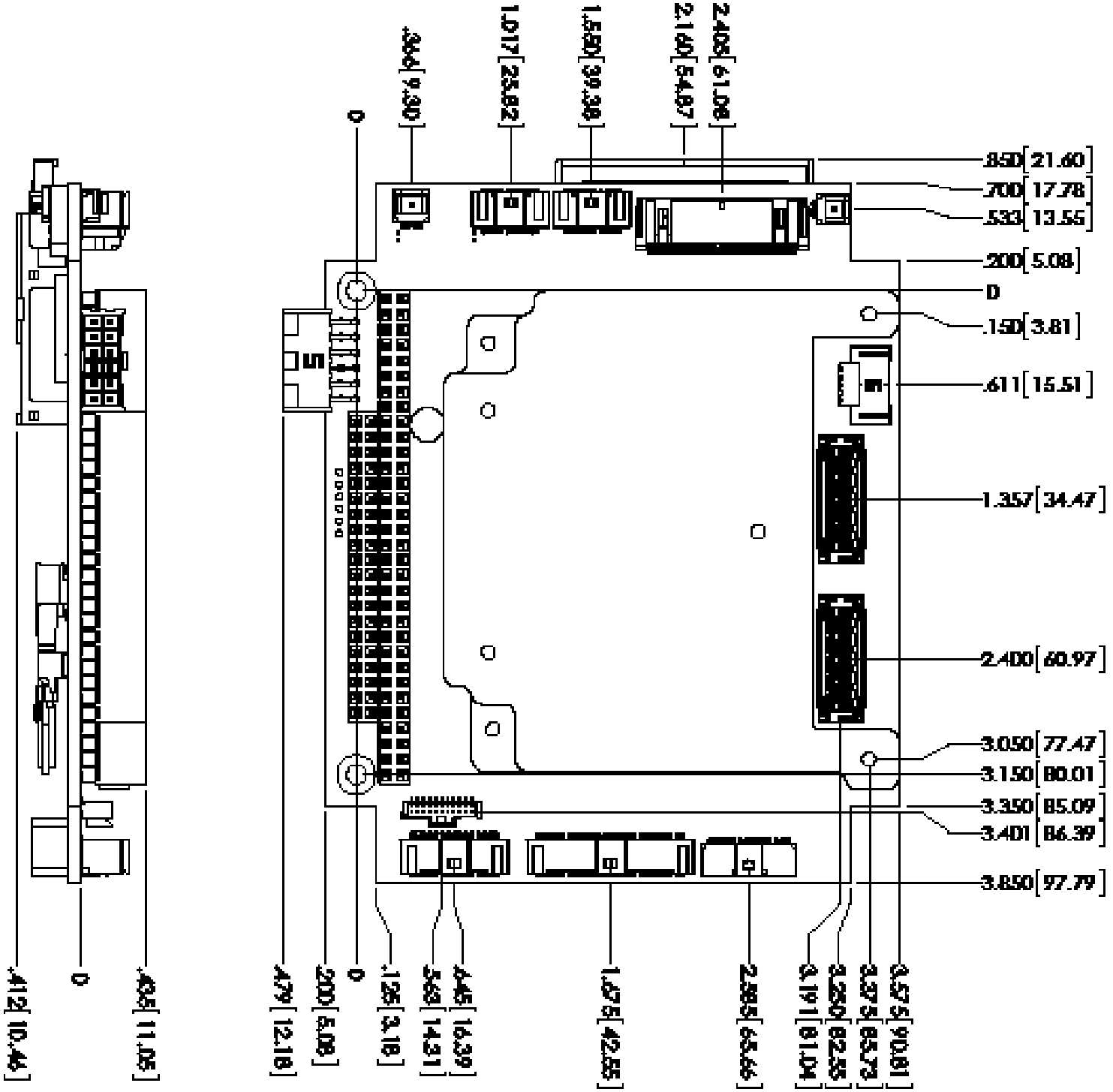
SPECIFICATIONS

Electrical		
VCC	±5V ±5% required, 2.5A typical	
	MODELS **PXM-C388-S1-0-0(-ST)** **PXM-C388-S1-0-1(-ST)**	
Power	Typical	2.5A
	Maximum	2.94A
	Standby (S3)	268 mA
MTBF	296,525 hours Bellcore TR-332, Issue 6 at 55 degress C	
Mechanical		
Dimensions	4.6 x 3.8 inches (116 x 96 mm)	
Weight	7.2 oz (204 g) (for PXM-C388-S1-0-0)	
Environmental		
Operating Temperature	-40°C to 85°C *	
Random Vibration	MIL-STD-202G, Method 214A, Condition D .1g/Hz (11.95g rms), 20 minutes per axis, 3 axis	
Mechanical Shock	MIL-STD-202G, Method 213B, Condition A 50g half-sine, 11 ms duration per axis, 3 axis	

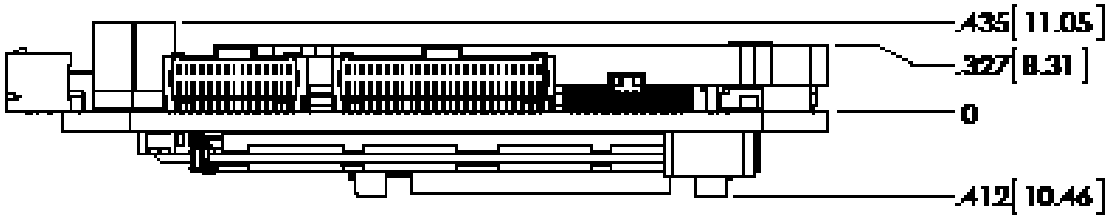
* - Thermal profiles can also vary greatly depending on the operating system and applications being used. WinSystems uses the Intel TAT (Thermal Analysis Tool) for testing with Intel processors. This program heavily loads the system and creates a worst case scenario for the single board computer. Specific real world applications will rarely tax the system as heavily and may allow for extending the fanless operational range. WinSystems conducts temperature verification with PassMark Burn-InTest to provide a more realistic real world example. The PassMark Burn-InTest is performed with all internal tests operating at 50% duty cycle.

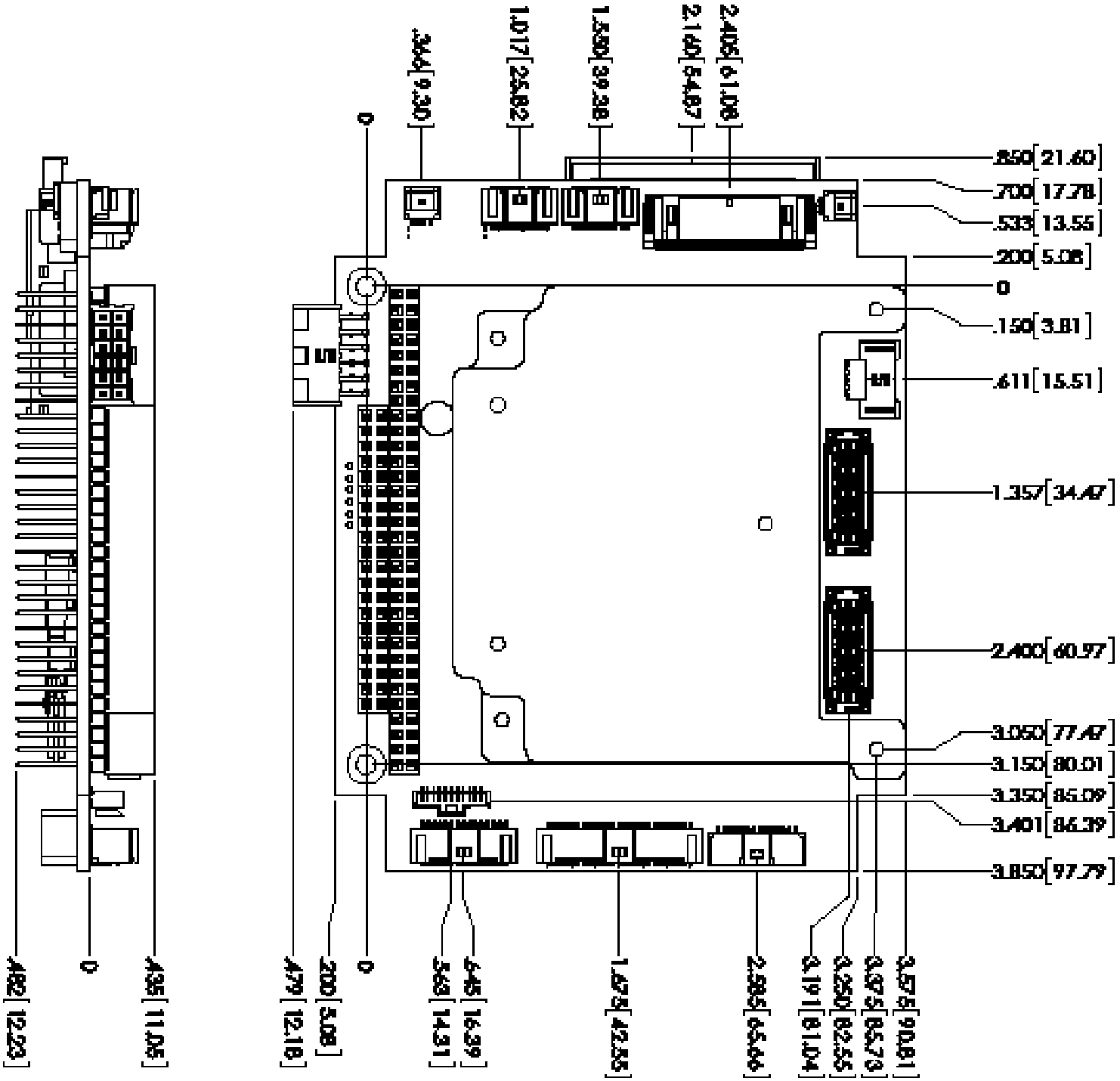
Thermal Qualification Testing						
SBC	**Test Application**	**Air Flow (linear ft/min)**	**Low Temp (Celsius)**	**High Temp (Celsius)**	**CPU Freq. (GHz)**	**CPU Throttling**
PXM-C388-S1-0-1(-ST)	PassMark BurnInTest	160	-40	85	1.66	No
PXM-C388-S1-0-1(-ST)	Intel TAT	160	-40	80	1.66	No
PXM-C388-S1-0-1(-ST)	PassMark BurnInTest	0	-40	63	1.66	No
PXM-C388-S1-0-1(-ST)	Intel TAT	0	-40	60	1.66	No
PXM-C388-S1-0-0(-ST)	PassMark BurnInTest	160	-40	71	1.66	No
PXM-C388-S1-0-0(-ST)	Intel TAT	160	-40	66	1.66	No
PXM-C388-S1-0-0(-ST)	PassMark BurnInTest	0	-40	51	1.66	No
PXM-C388-S1-0-0(-ST)	Intel TAT	0	-40	46	1.66	No

MECHANICAL DRAWING



PXM-C388-S1-0-0





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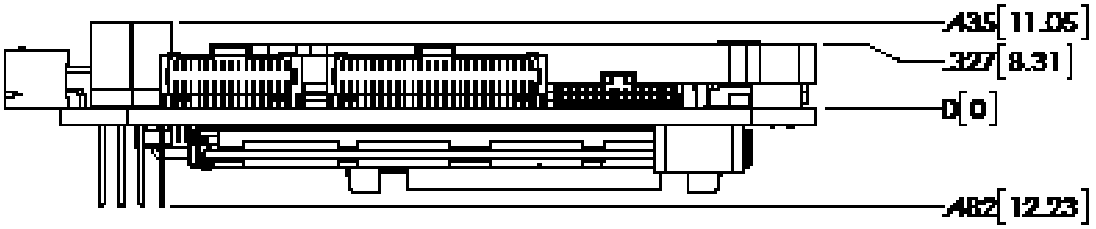

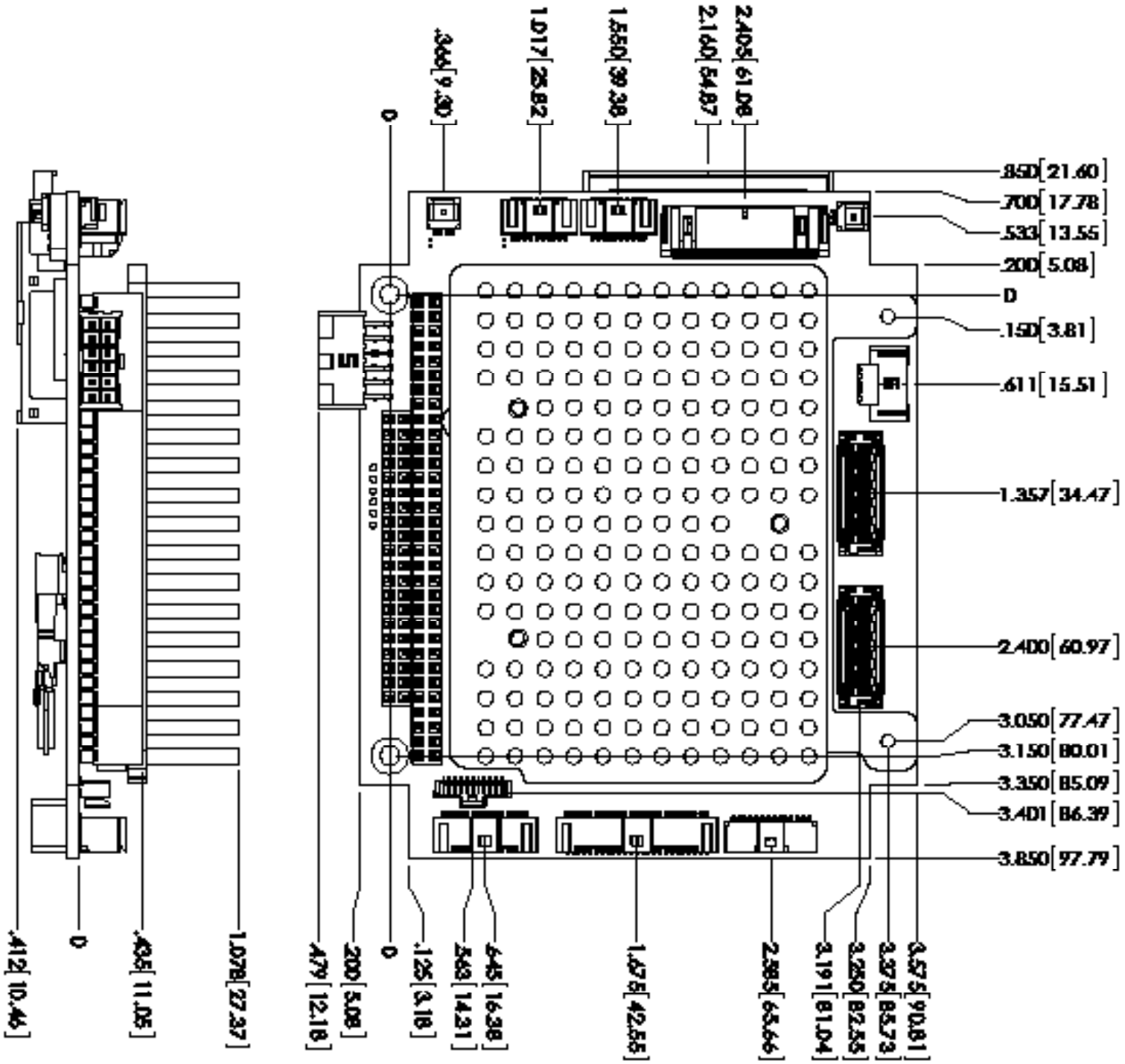

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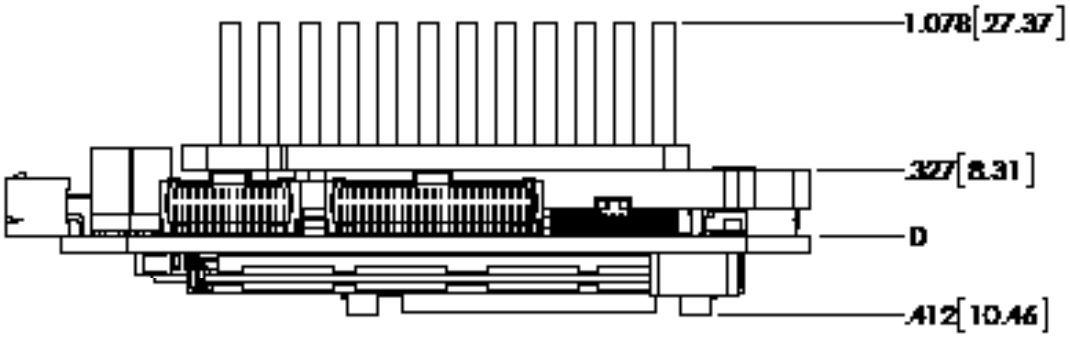
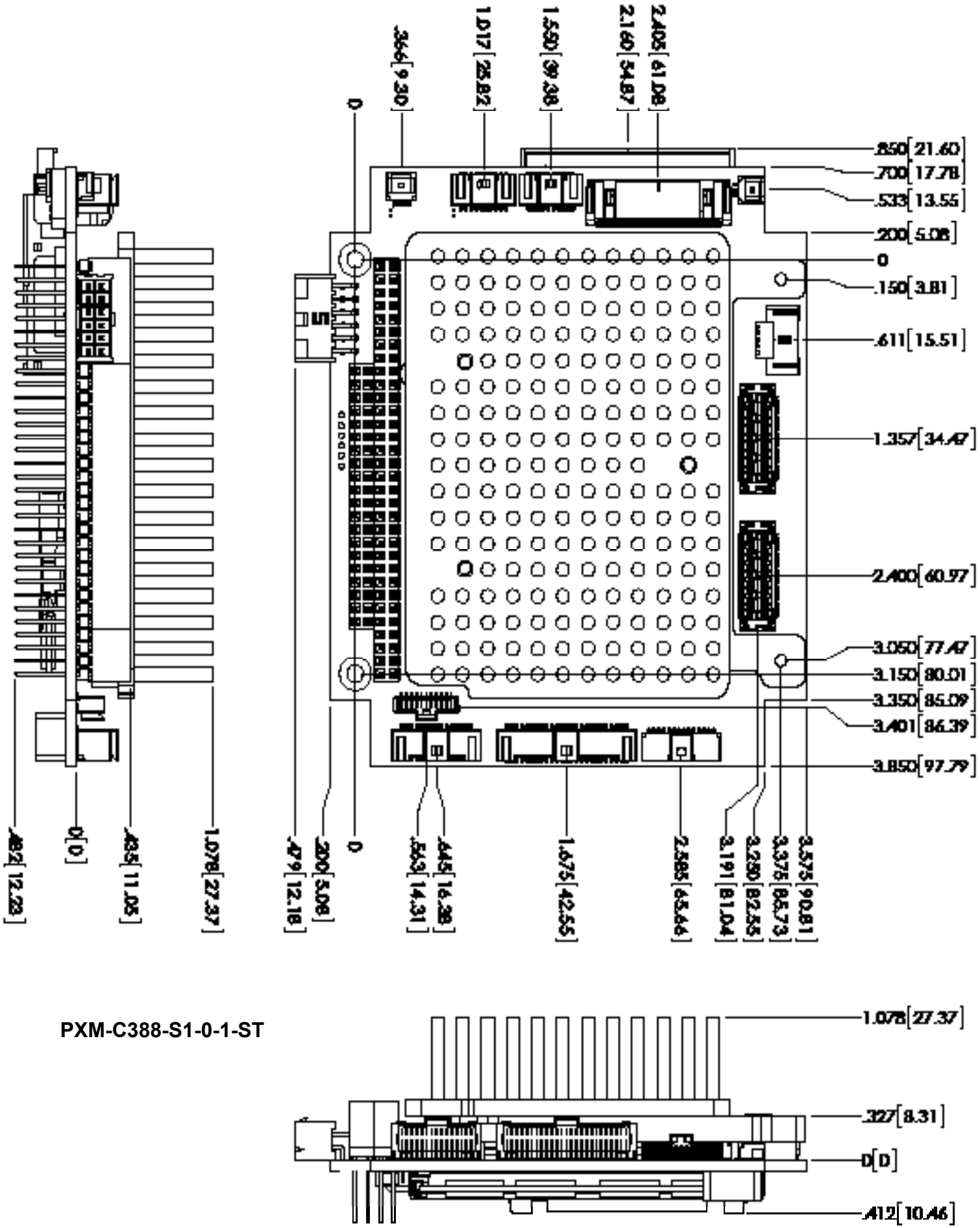




PXM-C388-S1-0-1-ST

APPENDIX - A

BEST PRACTICES

POWER SUPPLY

The power supply and how it is connected to the Single Board Computer (SBC) is very important.

Avoid Electrostatic Discharge (ESD)
Only handle the SBC and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

Power Supply Budget
Evaluate your power supply budget. It is usually good practice to budget 2X the typical power requirement for all of your devices.

Zero-Load Power Supply
Use a zero-load power supply whenever possible. A zero-load power supply does not require a minimum power load to regulate. If a zero-load power supply is not appropriate for your application, then verify that the single board computer's typical load is not lower than the power supply's minimum load. If the single board computer does not draw enough power to meet the power supply's minimum load, then the power supply will not regulate properly and can cause damage to the SBC.

Use Proper Power Connections (Voltage)
When verifying the voltage, you should always measure it at the power connector on the SBC. Measuring at the power supply does not account for voltage drop through the wire and connectors.

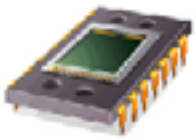
The single board computer requires +5V (±5%) to operate. Verify the power connections. Incorrect voltages can cause catastrophic damage.

Populate all of the +5V and ground connections. Most single board computers will have multiple power and ground pins, and all of them should be populated. The more copper connecting the power supply to the single board computer the better.

Adjusting Voltage
If you have a power supply that will allow you to adjust the voltage, it is a good idea to set the voltage at the power connector of the SBC to 5.1V. The SBC can tolerate up to 5.25V, so setting your power supply to provide 5.1V is safe and allows for a small amount of voltage drop that will occur over time as the power supply ages and the connector contacts oxidize.

Power Harness
Minimize the length of the power harness. This will reduce the amount of voltage drop between the power supply and the single board computer.

Gauge Wire
Use the largest gauge wire that you can. Most connector manufacturers have a maximum gauge wire they recommend for their pins. Try going one size larger; it usually works and the extra copper will help your system perform properly over time.



Contact Points
WinSystems' boards mostly use connectors with gold finish contacts. Gold finish contacts are used exclusively on high speed connections. Power and lower speed peripheral connectors may use a tin finish as an alternative contact surface. It is critical that the contact material in the mating connectors is matched properly (gold to gold and tin to tin). Contact areas made with dissimilar metals can cause oxidation/corrosion resulting in unreliable connections.

Pin Contacts
Often the pin contacts used in cabling are not given enough attention. The ideal choice for a pin contact would include a design similar to Molex's or Trifurcons' design, which provides three distinct points to maximize the contact area and improve connection integrity in high shock and vibration applications.

POWER DOWN

Make sure the system is **completely off/powered down** before connecting anything.

Power Supply OFF
The power supply should always be off before it is connected to the single board computer.

I/O Connections OFF
I/O Connections should also be off before connecting them to the single board computer or any I/O cards. Connecting hot signals can cause damage whether the single board computer is powered or not.

MOUNTING AND PROTECTING THE SINGLE BOARD COMPUTER

Do Not Bend or Flex the SBC
Never bend or flex the single board computer. Bending or flexing can cause irreparable damage. Single board computers are especially sensitive to flexing or bending around Ball-Grid-Array (BGA) devices. BGA devices are extremely rigid by design and flexing or bending the single board computer can cause the BGA to tear away from the printed circuit board.

Mounting Holes
The mounting holes are plated on the top, bottom and through the barrel of the hole and are connected to the single board computer's ground plane. Traces are often routed in the inner layers right below, above or around the mounting holes.

Never use a drill or any other tool in an attempt to make the holes larger.

Never use screws with oversized heads. The head could come in contact with nearby components causing a short or physical damage.

Never use self-tapping screws; they will compromise the walls of the mounting hole.

Never use oversized screws that cut into the walls of the mounting holes.

Always use all of the mounting holes. By using all of the mounting holes you will provide the support the single board computer needs to prevent bending or flexing.

Plug or Unplug Connectors Only on Fully Mounted Boards
Never plug or unplug connectors on a board that is not fully mounted. Many of the connectors fit rather tightly and the force needed to plug or unplug them could cause the single board computer to be flexed.

Avoid cutting of the SBC
Never use star washers or any fastening hardware that will cut into the single board computer.

Avoid Overtightening of Mounting Hardware
Causing the area around the mounting holes to compress could damage interlayer traces around the mouting holes.

Use Appropriate Tools
Always use tools that are appropriate for working with small hardware. Large tools can damage components around the mounting holes.

Placing the SBC on Mounting Standoffs
Be careful when placing the single board computer on the mounting standoffs. Sliding the board around until the standoffs are visible from the top can cause component damage on the bottom of the single board computer.

Avoid Conductive Surfaces
Never allow the single board computer to be placed on a conductive surface. Almost all single board computers use a battery to backup the clock-calendar and CMOS memory. A conductive surface such as a metal bench can short the battery causing premature failure.

ADDING PC/104 BOARDS TO YOUR STACK

Be careful when adding PC/104 boards to your stack.

Never allow the power to be turned on when a PC/104 board has been improperly plugged onto the stack. It is possible to misalign the PC/104 card and leave a row of pins on the end or down the long side hanging out of the connector. If power is applied with these pins misaligned, it will cause the I/O board to be damaged beyond repair.

CONFORMAL COATING

Applying conformal coating to a WinSystems product will not in itself void the product warranty, if it is properly removed prior to return. Coating may change thermal characteristics and impedes our ability to test, diagnose, and repair products. Any coated product sent to WinSystems for repair will be returned at customer expense and no service will be performed.

OPERATIONS / PRODUCT MANUALS

Every single board computer has an Operations manual or Product manual.

Manual Updates
Operations/Product manuals are updated often. Periodicially check the WinSystems website (http://www.winsystems.com) for revisions.

Check Pinouts
Always check the pinout and connector locations in the manual before plugging in a cable. Many single board computers will have identical headers for different functions and plugging a cable into the wrong header can have disastrous results.

Contact an Applications Engineer with questions
If a diagram or chart in a manual does not seem to match your board, or if you have additional questions, contact your Applications Engineer.

APPENDIX - B

POST CODES

If the system hangs before the BIOS can process the error, the value displayed at the I/O port I/O address 80h is the last test that performed. In this case, the screen does not display an error code.

The following is a list of the checkpoint codes written at the start of each test and their corresponding audio beep codes issued for terminal errors.

Code	Beeps	Location	Description
01h			IPMI initialization
02h			Verify real mode
03h			Disable non-maskable interrupt (NMI)
04h			Get CPU type
06h			Hardware initialization
07h			Chipset BIOS deshadow
08h			Chipset initialization
09h			Set IN POST flag
0Ah			CPU initialization
0Bh			CPU cache on
0Ch			Cache initialization
0Eh			I/O initialization
0Fh			FDISK initialization
10h			Power management initialization
11h			Register initialization
12h			Restore CR0
13h			PCI bus master reset
14h			8742 initialization (keyboard/embedded controller)
16h	1-2-2-3	Checksum BIOS ROM	
17h			Pre-size RAM (initialize cache before memory auto size)
18h			Timer initialization (8254 CTC)
1Ah			DMA initialization (8237 DMAC)
1Ch			Reset PIC (8259 PIC)
20h	1-3-1-1	Test DRAM refresh	
22h	1-3-1-3		Test 8742 Keyboard Controller
24h			Set huge ES (segment register to 4 GB)
26h			Enable A20
28h			Auto size DRAM
29h			POST memory manager (PMM) initialization
2Ah			Zero base (clear 512 KB base RAM)
2Bh			Enhanced CMOS initialization
2Ch	1-3-4-1	Address test (RAM failure on address line **xxxx***)	
2Eh	1-3-4-3	Base RAM Low (RAM failure on data bits **xxxx*** of low byte)	
2Fh			Pre-sys shadow (Enable cache before system BIOS shadow)
30h			Base RAM High (RAM failure on data bits **xxxx*** of high byte)
32h			Compute speed (test CPU bus-clock frequency)
33h			Post Dispatch Manager (PDM) initialization
34h			CMOS test
35h			Register re-initialization
36h			Check shutdown (perform warm restart)

Code	Beeps	Location	Description
37h			Chipset re-initialization
38h			System shadow (shadow BIOS ROM)
39h			Cache re-initialization
3Ah			Cache auto-size
3Bh			Debug server initialization
3Ch			Advanced chipset initialization
3Dh			Advanced register configuration
3Eh			Read hardware
3Fh			RomPilot memory initialization
40h			Speed
41h			RomPilot initialization
42h			Interrupt vectors initialization
44h			Set BIOS interrupt
45h			Device initialization
46h	2-1-2-3	Check ROM copyright	
48h			Config (Check video configuration against CMOS)
49h			PCI initialization
4Ah			Video initialization (Initialize all video adapters)
4Bh			QuietBoot start
4Ch			Video shadow (Shadow video BIOS)
4Eh			Copyright display
4Fh			MultiBoot-XP initialization
50h			CPU type display
51h			EISA initialization
52h			Keyboard test
54h			Set key click (if enabled)
55h			USB initialization
56h			Enabled keyboard
57h			1394 Firewire initialization
58h	2-2-3-1	HOT (Test for unexpected interrupts)	
59h			POST display service (PDS) initialization
5Ah			Display prompt **Press F2 to enter SETUP**
5Bh			CPU cache off
5Ch			Test RAM between 512 KB to 640 KB
60h			Test extended memory
62h			Test extended memory address
64h			Jumper to UserPatch1
66h			Configure advanced cache registers
67h			Initialize Multi Processor APIC
68h			Cache configuration (enable internal and external caches)
69h			PM setup System Management Mode (SMM)
6Ah			Display external L2 cache size
6Bh			Load custom defaults (optional)
6Ch			Display shadow-area messages
70h			Display error messages
72h			Check for configuration errors

Code	Beeps	Location	Description
74h			RTC test
76h			Keyboard test
7Ah			Key lock
7Ch			Hardware interrupts
7Dh			Intelligent System Monitoring (ISM) initialization
7Eh			Coprocessor initialization (if present)
80h			I/O initialization (before)
81h			Late device initialization
82h			RS-232 initialization
83h			FDISK config IDE
84h			LPT initialization
85h			PCI PCC initialization (PC-compatible PnP ISA devices)
86h			I/O initialization (after)
87h			Motherboard Configurable Devices (MCD) initialization
88h			BIOS data-area initialization (BDA)
89h			Enable Non-Maskable Interrupt (NMI)
8Ah			Extended BIOS Extended Data Area (EBDA)
8Bh			Mouse initialization
8Ch			Floppy initialization
8Fh			FDISK fast pre-initialization
90h			FDISK initialization
91h			FDISK fast initialization
92h			Jump to UserPatch2
93h			Build MPTABLE for multi-processor boards
95h			CDROM initialization
96h			Clear huge ES
97h			MultiProcessor table fix-up
98h	1-2		Option ROM scan
99h			FDISK check SMART
9Ah			Miscellaneous shadow (shadow option ROMs)
9Bh			PM CPU speed
9Ch			Power Management (PM) setup
9Dh			Intialize security engine
9Eh			IRQS
9Fh			FDISK fast initialization #2
A0h			Time of day - set
A2h			Keylock test
A4h			Key rate initialization (typematic rate)
A8h			Erase F2 prompt
AAh			Scan for F2 keystroke
ACh			Setup check
AEh			Clear bootflag
B0h			Error check
B1h			RomPilot unload
B2h			POST done - prepare to boot operating system
B4h	1		One beep (before boot)

Code	Beeps	Location	Description
B5h			Terminate QuietBoot
B6h			Check password
B7h			ACPI initialization
B8h			System initialization
B9h			Prepare to boot
BAh			DMI - SMBIOS initialization
BBh			BCV (Boot Connection Vectors) initialization
BCh			Parity - clear parity checkers
BDh			MultiBoot-XP boot menu display
BEh			Clear screen
BFh			Check reminders (virus and backup)
C0h			INT19 - boot
C1h			POST Error Manager (PEM) - Initialization
C2h			POST Error Manager (PEM) - Logging initialization
C3h			POST Error Manager (PEM) - Initialize error display function
C4h			POST Error Manager (PEM) - Initialize system error handler
C5h			PNP'ed dual CMOS
C6h			Initialize note dock
C7h			Initialize note dock late
C8h			Force check
C9h			Extended checksum

Embedded Extensions	
Code	**Description**
CAh	TP_SERIAL_KEY - Redirect INT15h to serial keyboard
CBh	TP_ROMRAM - Redirect INT13h to Memory Technologies Devices Such as ROM, RAM, PCMCIA, and serial disk
CCh	TP_SERIAL_VID - Redirect INT10h to enable remote serial video
CDh	TP_PCMATA - Re-map I/O and memory for PCMCIA
CEh	TP_PEN_INIT - Initialize digitizer and display message
CFh	TP_XBDA_FAIL - Extended BIOS Data Area (XBDA) failure

More Post Codes	
Code	**Description**
D1h	TP_BIOS_STACK_INIT
D3h	TP_SETUP_WAD
D4h	TP_CPU_GET_STRING
D5h	TP_SWITCH_POST_TABLES
D6h	TP_PCCARD_INIT
D7h	TP_FIRSTWARE_CHECK
D8h	TP_ASF_INIT
D9H	TP_IPMI_INIT_LATE
DAh	TP_PCIE_INIT
DBh	TP_SROM_TEST
DCh	TP_UPD_ERROR
DDh	TP_REMOTE_FLASH
DEh	TP_UNDI_INIT
DFh	TP_UNDI_SHUTDOWN
E0h	TP_EFI_NV_INIT
E1h	TP_PERIODIC_TIMER

Boot Block	
Code	**Description**
80h	TP_BB_CS_INIT - Chipset Init
81h	TP_BB_BRIDGE_INIT - Bridge Init
82h	TP_BB_CPU_UNIT - CPU Init
83h	TP_BB_TIMER_INIT - System timer Init
84h	TP_BB_IO_INIT - System I/O Init
85h	TP_BB_FORCE - Check force recovery boot
86h	TP_BB_CHKSUM - Check BIOS Checksum
87H	TP_BB_GOTOBIOS - Go to BIOS
88h	TP_BB_MP_INIT - Init Multi Processor
89h	TP_BB_SET_HUGE - Set Huge Seg
8Ah	TP_BB_OEM_INIT - OEM Special Init
8Bh	TP_BB_HW_INIT - Init PIC and DMA
8Ch	TP_BB_MEM_TYPE - Init Memory Type
8Dh	TP_BB_MEM_SIZE - Init Memory Size
8Eh	TP_BB_SHADOW - Shadow Boot Block
8Fh	TP_BB_SMM_INIT - Init SMM
90h	TP_BB_RAMTEST - System Memory Test
91h	TP_BB_VECS_INIT - Init Interrupt Vectors
92h	TP_BB_RTC_INIT - Init RTC
93h	TP_BB_VIDEO_INIT - Init Video
94h	TP_BB_OUT_INIT - Init Beeper
95h	TP_BB_BOOT_INIT - Init Boot
96h	TP_BB_CLEAR_HUGE - Clear Huge Seg
97h	TP_BB_BOOT_OS - Boot to OS
98h	TP_BB_USB_INIT - Intialize the USB Controller
99h	TP_BB_SECUR_INIT - Init Security

***** If the BIOS detects error 2C, 2E, or 30 (base 512 KB RAM error), it displays an additional word-bitmap (**xxxx**) indicating the address line or bits that failed.

For example, “2C 0002” means address line 1 (bit one set) has failed. “2E 1020” means data bits 12 and 5 (bits 12 and 5 set) have failed in the lower 16 bits. Note that error 30 cannot occur on 386SX systems because they have a 16 rather than 32-bit bus. The BIOS also sends the bitmap to the port-80h LED display. It first displays the checkpoint code, followed by a delay, the high-order byte, another delay, and then the low-order byte of the error. It repeats this sequence continuously.

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