PCM-SDIO

PC/104 Quad Serial and 48-line Digital I/O

PRODUCT MANUAL

WinSystems, Inc.
715 Stadium Drive
Arlington, TX 76011

http://www.winsystems.com

MANUAL REVISION HISTORY

P/N 400-0387-000

Revision Date Code	ECO Number
120411	Initial Release
120713	ECO 12-79
130403	

TABLE OF CONTENTS

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BEFORE YOU BEGIN

WinSystems offers best practice recommendations for using and handling WinSystems embedded PCs. These methods include valuable advice to provide an optimal user experience and to prevent damage to yourself and/or the product.

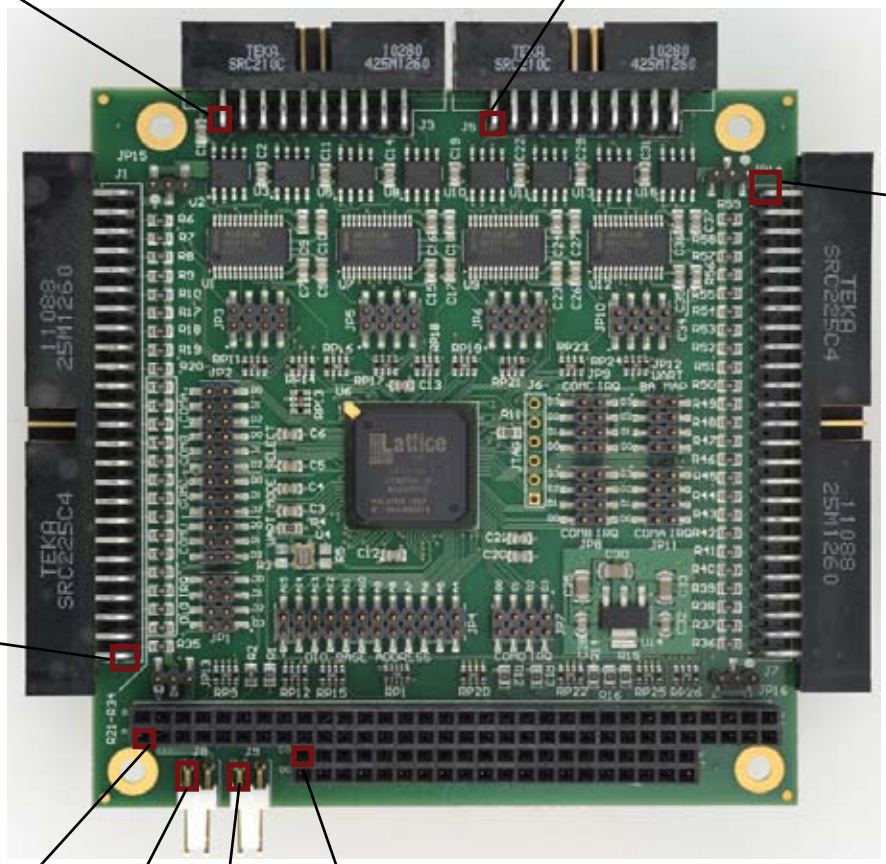
YOU MAY VOID YOUR WARRANTY AND/OR DAMAGE AN EMBEDDED PC BY FAILING TO COMPLY WITH THESE BEST PRACTICES.

Reference **Appendix - A** for **Best Practices**.

Please review these guidelines carefully and follow them to ensure you are successfully using your embedded PC.

For any questions you may have on WinSystems products, contact our Technical Support Group at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

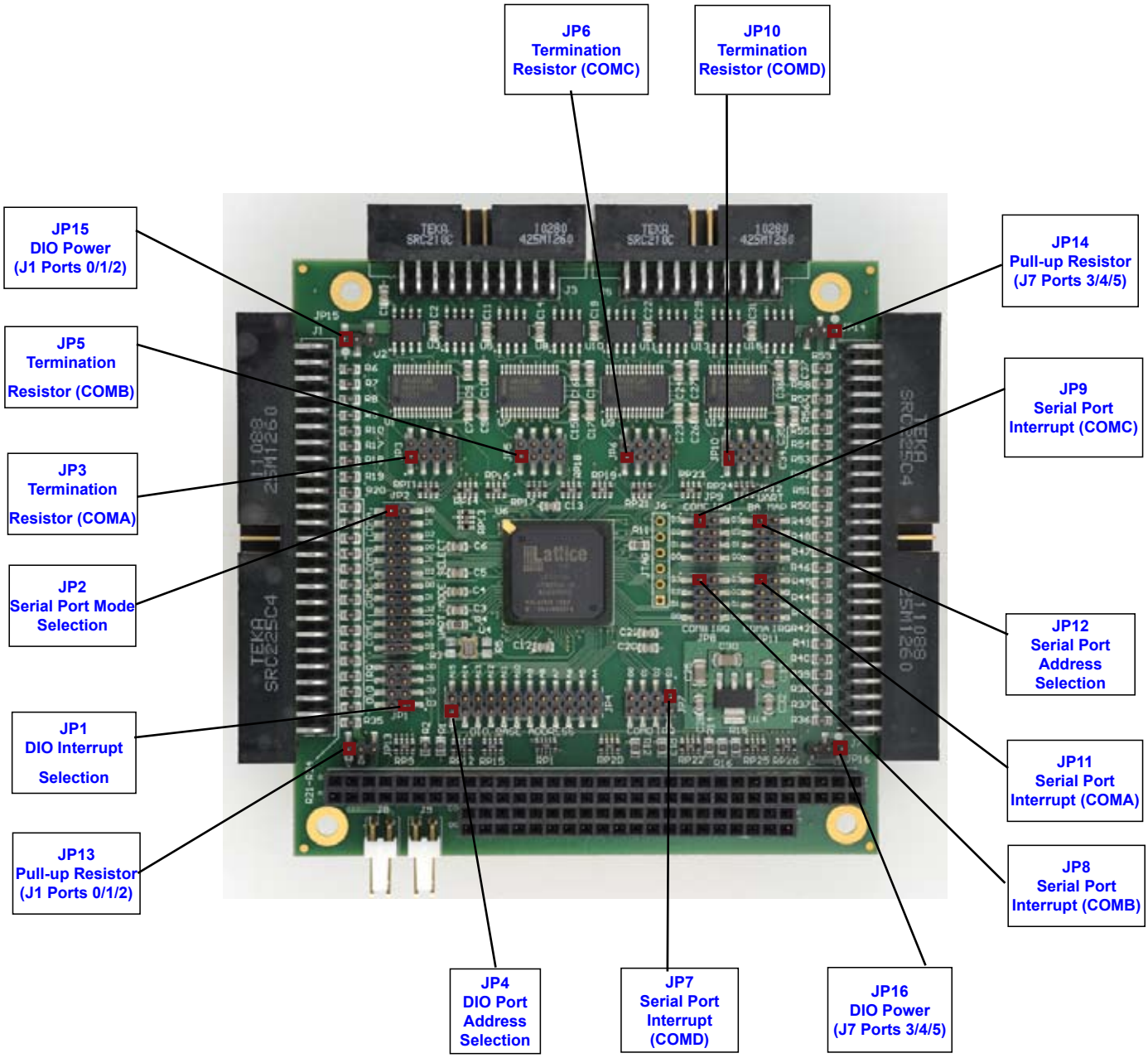
Visual Index - Top View (Connectors)



RESERVED - J6

NOTE: The reference line to each component part has been drawn to Pin 1, and is also highlighted with a square, where applicable.

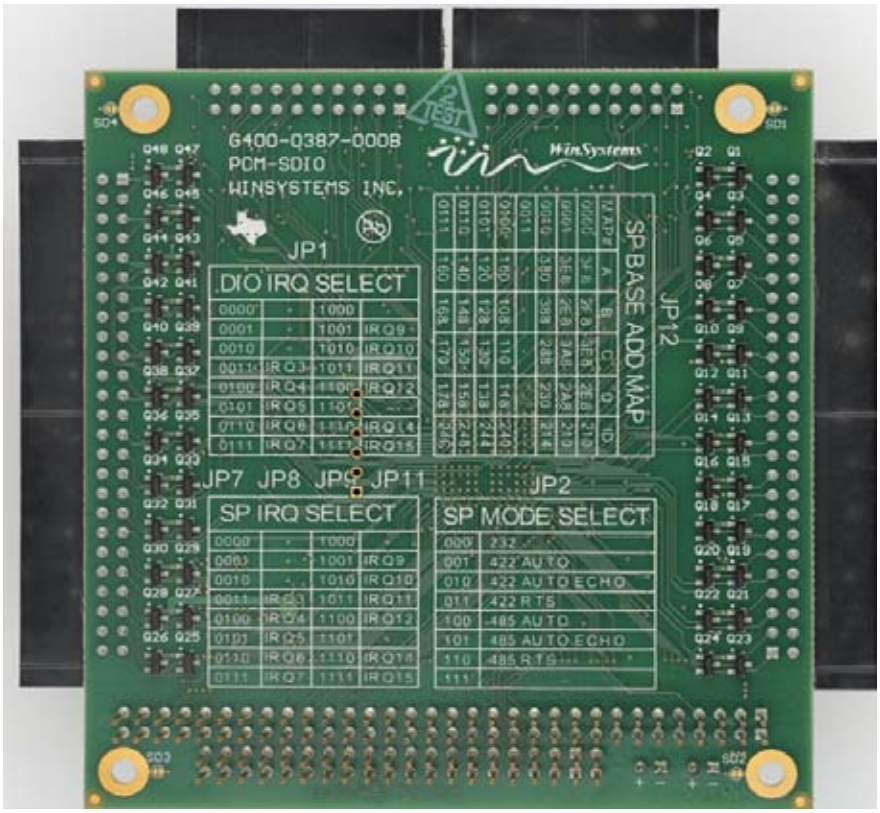
Visual Index - Top View (Jumpers)



RESERVED - J6

NOTE: The reference line to each component part has been drawn to Pin 1, and is also highlighted with a square, where applicable.

Visual Index - Bottom View



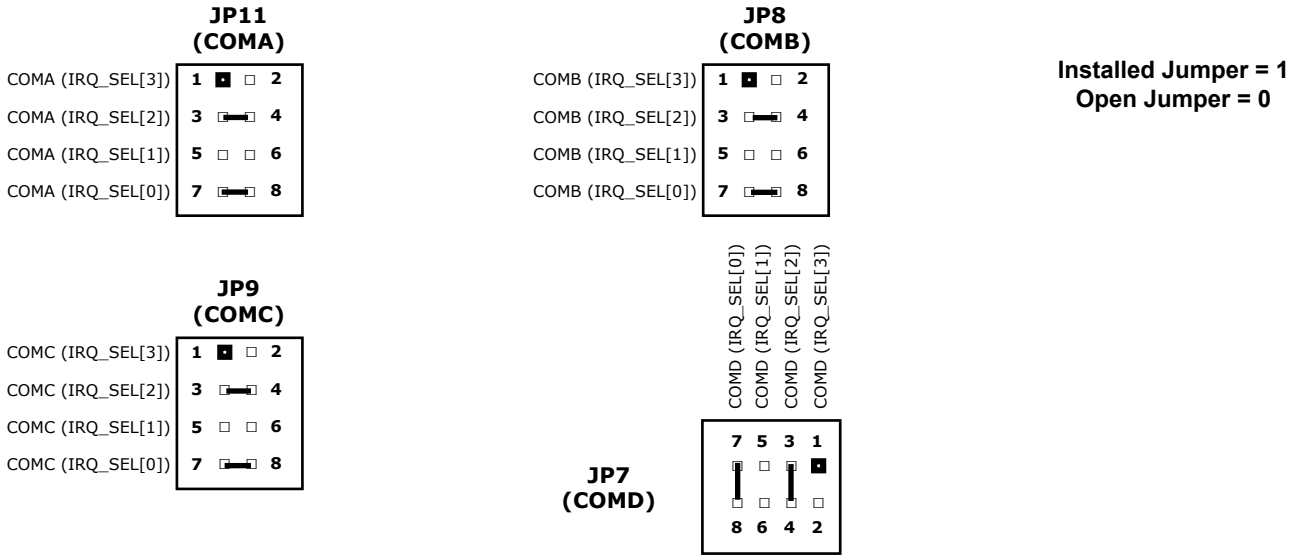
RESERVED - J6

NOTE: The reference line to each component part has been drawn to Pin 1, and is also highlighted with a square, where applicable.

Jumper Reference

NOTE: Jumper Part# SAMTEC 2SN-BK-G is applicable to all jumpers. These are available in a ten piece kit from WinSystems (Part# KIT-JMP-G-200).

JP11 - COMA, JP8 - COMB, JP9 - COMC, JP7 - COMD (Serial Port Interrupts)

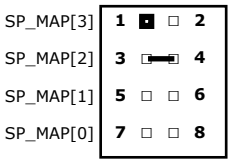


*The jumper references above represents **IRQ5** shared for each port.

JP7, JP8, JP9, J11 Serial Port IRQ Selection	
Binary	**IRQ**
0000	Not Used
0001	Not Used
0010	Not Used
0011	IRQ3
0100	IRQ4
0101	IRQ5
0110	IRQ6
0111	IRQ7
1000	Not Used
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	Not Used
1110	IRQ14
1111	IRQ15

JP12 - Serial Port Base Address

JP12



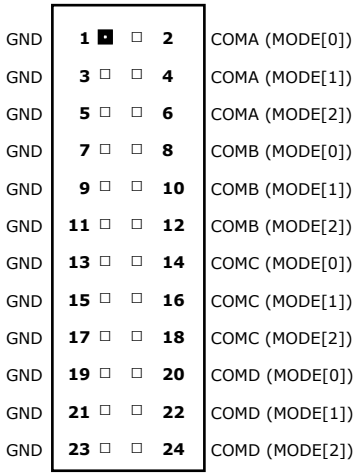
*The jumper reference above represents **Map 0100**.

JP12 Serial Port Base Address Selection					
Map#	**A**	**B**	**C**	**D**	**Interrupt Status Register**
0000	3F8	2F8	3E8	2E8	220
0001	3E8	2E8	3A8	2A8	220
0010	380	388	288	230	224
0011	RESERVED				
0100	100	108	110	118	240
0101	120	128	130	138	244
0110	140	148	150	158	248
0111	160	168	170	178	24C

Installed Jumper = 1
Open Jumper = 0

JP2 - Serial Port Operation Mode

JP2

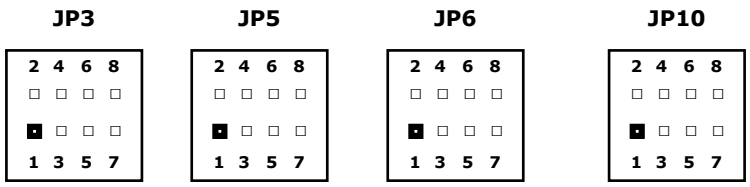


Installed Jumper = 1
Open Jumper = 0

JP2 Serial Port Mode Selection	
Binary	**Mode**
0000	RS-232 Mode
0001	RS-422 Mode with RTS transmitter enable
0010	RS-422 Mode with auto transmitter enable
0011	RS-485 Mode with transmitter enable
0100	RS-485 Mode with transmitter enable and echo back
0101	RS-485 Mode with auto transmitter enable
0110	RS-485 Mode with auto transmitter enable and echo back
0111	Reserved

Jumper Reference (cont'd)

JP3 - COMA, JP5 - COMB, JP6 - COMC, JP10 - COMD (Termination Resistors)



RS-422 Termination and Biasing Resistors		
TX (100): Places a 100Ω Resistor across the TX+/TX- pair		7-8
RX (100): Places a 100Ω Resistor across the RX+/RX- pair		1-2
TX/RX(300):	Places a 100Ω Resistor from +5V to TX+	5-6
	Places a 100Ω Resistor between TX+ and TX-	7-8
	Places a 100Ω Resistor from Ground to TX-	3-4

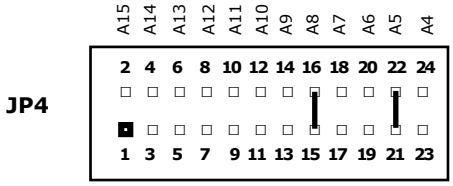
Revision B PCB products require a wire-wrap jumper from 2-3.

Revision B PCB products require a wire-wrap jumper from 1-4.

RS-485 Termination and Biasing Resistors		
TX/RX (100): Places a 100Ω Resistor across the TX/RX+/TX/RX- pair		7-8
TX/RX(300):	Places a 100Ω Resistor from +5V to TX/RX+	5-6
	Places a 100Ω Resistor between TX/RX+ and TX/RX-	7-8
	Places a 100Ω Resistor from Ground to TX/RX-	3-4

Revision B PCB products require a wire-wrap jumper from 1-4.

JP4 - DIO Base Address

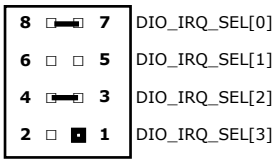


Installed Jumper = Binary 1
Open Jumper = 0

*The jumper reference above represents **120H**.

JP1 - DIO Interrupts

JP1

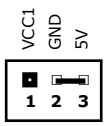


*The jumper reference above represents **IRQ5**.

JP1 DIO IRQ Selection	
Binary	**IRQ**
0000	Not Used
0001	Not Used
0010	Not Used
0011	IRQ3
0100	IRQ4
0101	IRQ5
0110	IRQ6
0111	IRQ7
1000	Not Used
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	Not Used
1110	IRQ14
1111	IRQ15

JP13 - Pull-up Resistor (for J1)

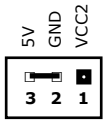
JP13



Pull-up Resistor source for +5V (default)	2-3
No Pull-up Resistor	OPEN
Pull-up Resistor source for VCC1 provided at **J8**	1-2

JP14 - Pull-up Resistor (for J7)

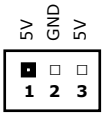
JP14



Pull-up Resistor source for +5V (default)	2-3
No Pull-up Resistor	OPEN
Pull-up Resistor source for VCC2 provided at **J9**	1-2

JP15 - Digital I/O VCC (for J1)

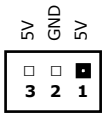
JP15



+5V is provided at pin 49 of **J1**	1-2
No Power at Pin 49 of **J1** (default)	OPEN

JP16 - Digital I/O VCC (for J7)

JP16



+5V is provided at pin 49 of **J7**	1-2
No Power at Pin 49 of **J7** (default)	OPEN

INTRODUCTION

This manual is intended to provide the necessary information regarding configuration and usage of the PCM-SDIO PC/104 expansion board. WinSystems maintains a Technical Support Group to help answer questions not adequately addressed in this manual. Contact Technical Support at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

FEATURES

Digital I/O

- 48 Bidirectional lines (WS16C48)
- 12 mA sink current
- 5 mA source current
- 30V I/O tolerance

Serial I/O

- 4 UART serial ports (16550)
- Jumper selectable RS-232/422/485 port types
- 115.2 kbps Baud Rate maximum
- Jumper selectable RS-422/485 termination resistors
- Jumper selectable Interrupts
- Jumper selectable Base address

Bus Expansion

- PC/104

Industrial Operating Temperature

- -40°C to 85°C

Mechanical

- PC/104-compliant
- 3.60” x 3.80” (90 mm x 96 mm)
- Weight: 3.2 oz (90.7 g)

Additional Features

- RoHS compliant

Product Description

The PCM-SDIO is a PC/104-compatible expansion card which provides 48 lines of digital I/O (DIO) and utilizes 4 serial channels based on the 16550 type UART. Each UART has a maximum baud rate capacity of 115.2 kbps and is configurable for RS-232/RS-422/RS-485 operation modes. The 48-bit DIO interface contains 2 ports, each composed of three 8-bit registers. Each bit is individually configurable as input or output. Input signal levels as high as 30 VDC are allowed for the DIO interface.

The PCM-SDIO allows for programmable logic device (PLD) implementation of the 4 serial channels and 48 lines of digital I/O. The DIO and UART peripherals are I/O mapped and relocation in the 16-bit ISA I/O address space is accomplished via on-board jumper selection.

SERIAL

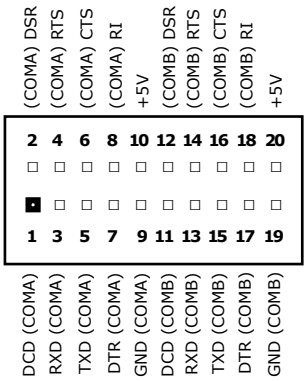
All ports are configured as Data Terminal Equipment (DTE). Both the send and receive registers of each port have a 16-byte FIFO. All serial ports have 16C550-compatible UARTs. The RS-232 has a charge pump to generate the plus and minus voltages so the PCM-SDIO only requires +5V to operate. An independent, software programmable baud rate generator is selectable from 50 through 115.2 kbps. Individual modem handshake control signals are supported for all ports.

J3 - COMA/COMB, J5 - COMC/COMD

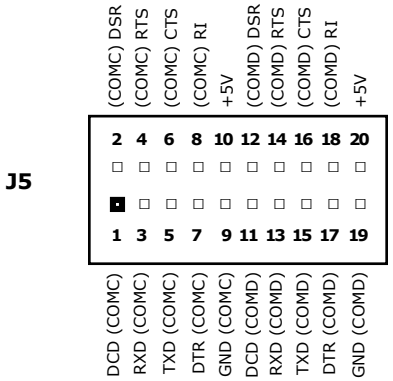
Visual Index

PCB Connector: **TEKA SRC210C425M126-0 (J3, J5)**
Mating Connector: **ITW-PANCON 050-020-455A**

J3



J5



JP12 - Serial Port Base Address Map

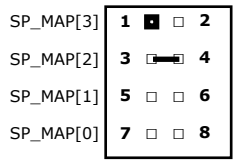
JP12 is used to select the serial port base addresses. Each of the 4 serial ports is mapped to a unique binary code base address. The INTID register represents an alternate single register which is useful when sharing system interrupts between ports. Instead of querying each individual port, the INTID register can be used by an application developer to determine the source of an interrupt. Below is the Serial Port Base Address Map.

JP12 Serial Port Base Address Selection					
Map#	**A**	**B**	**C**	**D**	**Interrupt Status Register**
0000	3F8	2F8	3E8	2E8	220
0001	3E8	2E8	3A8	2A8	220
0010	380	388	288	230	224
0011	RESERVED				
0100	100	108	110	118	240
0101	120	128	130	138	244
0110	140	148	150	158	248
0111	160	168	170	178	24C

Installed Jumper = 1
Open Jumper = 0

Serial Port Address Selection (JP12)

JP12



*The jumper reference above represents **Map 0100**.

Serial Port Interrupt Status Register

The PCM-SDIO has a fast on-board interrupt identification register mapped to an I/O port dependent on the map selected. (See the Serial Port Base Address Map for more information.) This read-only register is used with shared interrupts for quick identification of the UART channel(s) requiring service. The register's bit definitions are listed below.

Interrupt Status Register

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	UART D	UART C	UART B	UART A

WinSystems does not provide software support for implementing the Interrupt Status Register to share interrupts. Some operating systems, such as Windows XP and Linux, have support for sharing serial port interrupts and examples are available. The user will need to implement the appropriate software to share interrupts for the other devices.

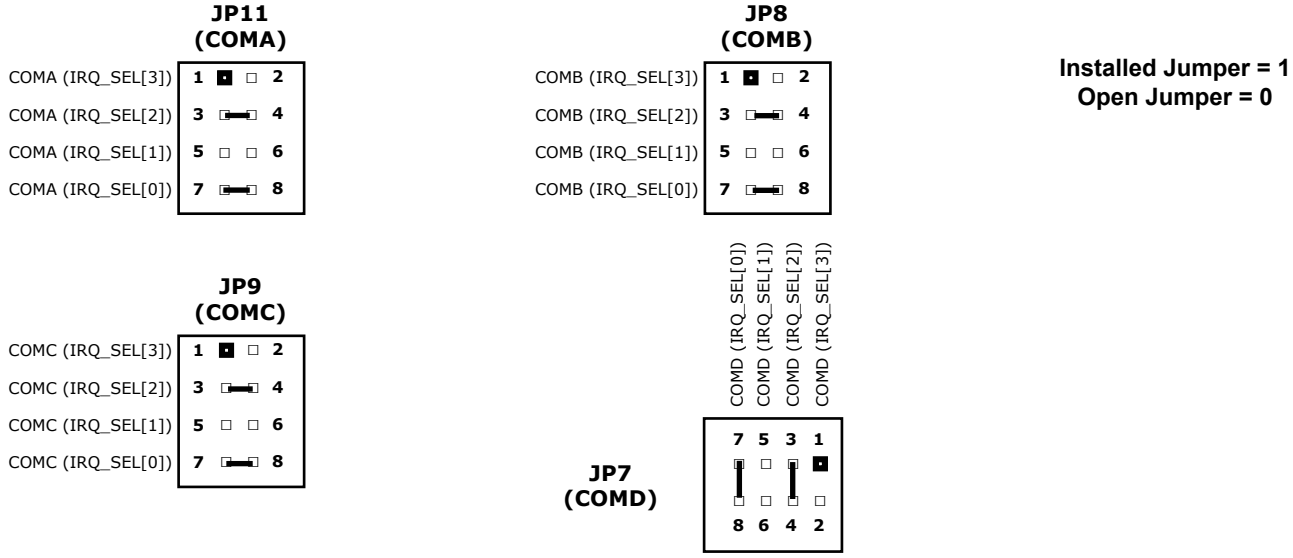
Serial UART Register Map

Standard UART 16550 Register Map

IO	REG	DESC	D7	D6	D5	D4	D3	D2	D1	D0
R	00h	RHR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
W	00h	THR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	01h	IER	0	0	0	0	MODEM STATUS INT	RX LINE STATUS	THR EMPTY	RHR EMPTY
W	02h	FCR	RX FIFO INT LEVEL [D1]	RX FIFO INT LEVEL [D0]	0	0	DMA MODE	CLEAR TX FIFO	CLEAR RX FIFO	ENABLE FIFO
R	02h	IIR	FIFO STATUS [D1]	FIFO STATUS [D0]	0	0	INTID[2]	INTID[1]	INTID[0]	INT PENDING
R/W	03h	LCF	DIV LATCH ACCESS BIT	BREAK	PAR [D2]	PAR [D1]	PAR [D0]	STOP	DATA WORD LEN [D1]	DATA WORD LEN [D0]
R/W	04h	MCF	-	-	FLOW CTRL	LOOPBACK	AUX2	AUX1	RTS	DTR
R	05h	LSR	FIFO ERROR	TSR EMPTY	THR EMPTY	RX BREAK	RX FRAME ERROR	RX DATA PAR ERROR	RX DATA OVERRUN	RX DATA READY
R	06h	MSR	CD	RI	DSR	CTS/CD	Delta RI	Delta DSR	Delta CTS	Delta
R/W	07h	SPR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	00h	DLL	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R/W	01h	DLM	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0

The PCM-SDIO uses the jumpers **JP7**, **JP8**, **JP9** and **JP11** to select the serial port interrupts. The interrupt for each port is chosen by installing jumpers to represent the binary number of the desired input. For more information on choosing a binary number see the Serial Interrupt Port Map section below.

JP11 - COMA, JP8 - COMB, JP9 - COMC, JP7 - COMD (Serial Port Interrupts)



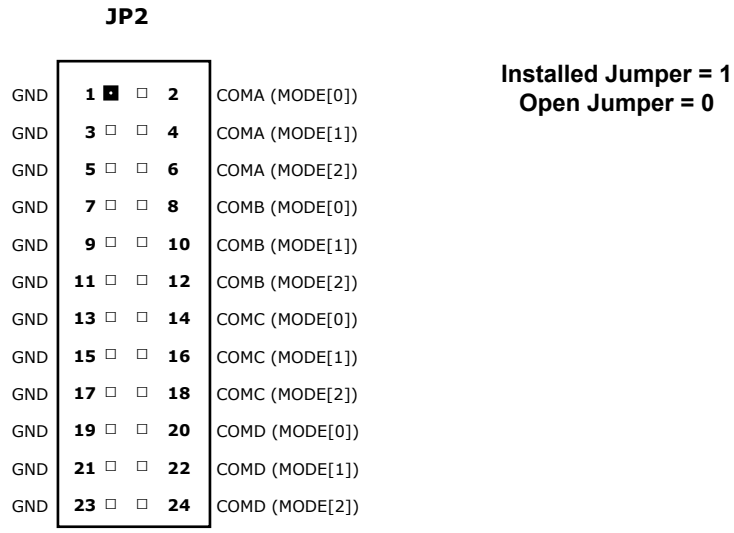
*The jumper references above represents **IRQ5** shared for each port.

Serial Port Interrupt Map (JP7, JP8, JP9, JP11)

JP7, JP8, JP9, J11 Serial Port IRQ Selection	
Binary	**IRQ**
0000	Not Used
0001	Not Used
0010	Not Used
0011	IRQ3
0100	IRQ4
0101	IRQ5
0110	IRQ6
0111	IRQ7
1000	Not Used
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	Not Used
1110	IRQ14
1111	IRQ15

JP2 - Serial Port Operation Mode

The **JP2** jumper is used to select the serial port operation mode. Each port has 6 unique operation modes which are configurable by selecting a 3-bit binary code. In RS-422 (RTS) and RS-485 (RTS) modes, the RTS (Request to Send) UART signal is used to enable the respective differential transceiver. In RS-422 AUTO and RS-485 (AUTO) modes, the transmit data bit itself is used to enable the transceiver. Nuances of the different modes can help simplify an application programmer's task. For more information on selecting modes, see the Serial Port Mode Selection Map section below.



Serial Port Mode Selection Map (JP2)

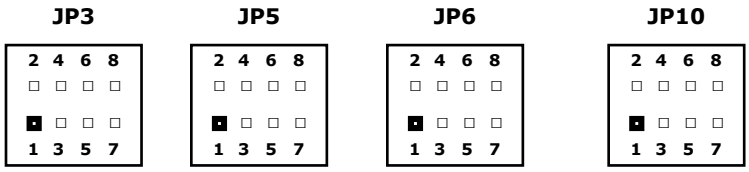
Serial port operation modes are chosen by installing jumpers on **JP2.** The table below lists the mode selections as used by the PCM-SDIO.

JP2 Serial Port Mode Selection	
Binary	**Mode**
0000	RS-232 Mode
0001	RS-422 Mode with RTS transmitter enable
0010	RS-422 Mode with auto transmitter enable
0011	RS-485 Mode with transmitter enable
0100	RS-485 Mode with transmitter enable and echo back
0101	RS-485 Mode with auto transmitter enable
0110	RS-485 Mode with auto transmitter enable and echo back
0111	Reserved

JP3, JP5, JP6, JP10 - RS-422/RS-485 Termination Resistor Installation (Optional)

The PCM-SDIO uses the jumpers **JP3**, **JP5**, **JP6** and **JP10** to optionally install RS-422/RS-485 resistors.

JP3 - COMA, JP5 - COMB, JP6 - COMC, JP10 - COMD (Termination Resistors)



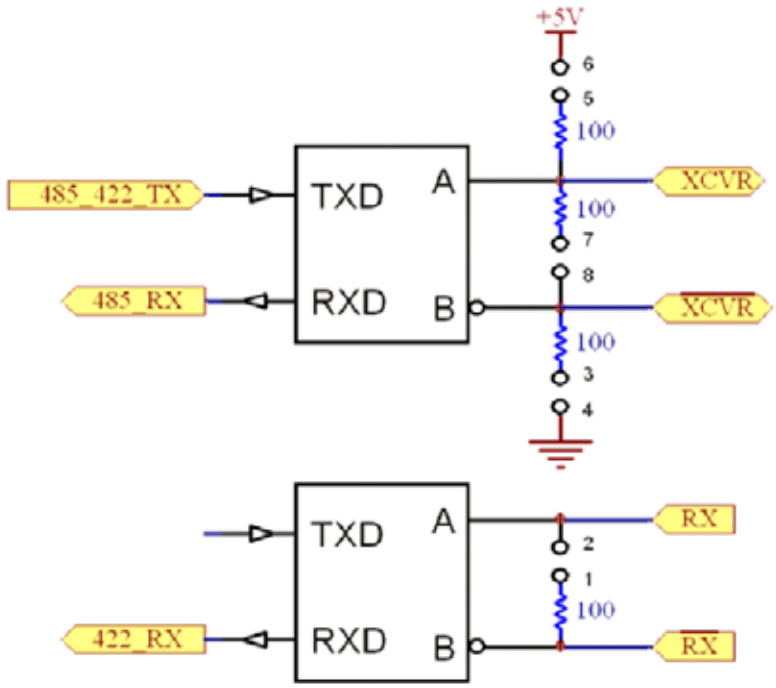
RS-422 Termination and Biasing Resistors		
TX (100): Places a 100Ω Resistor across the TX+/TX- pair		7-8
RX (100): Places a 100Ω Resistor across the RX+/RX- pair		1-2
TX/RX(300):	Places a 100Ω Resistor from +5V to TX+	5-6
	Places a 100Ω Resistor between TX+ and TX-	7-8
	Places a 100Ω Resistor from Ground to TX-	3-4

Revision B PCB products require a wire-wrap jumper from 2-3.

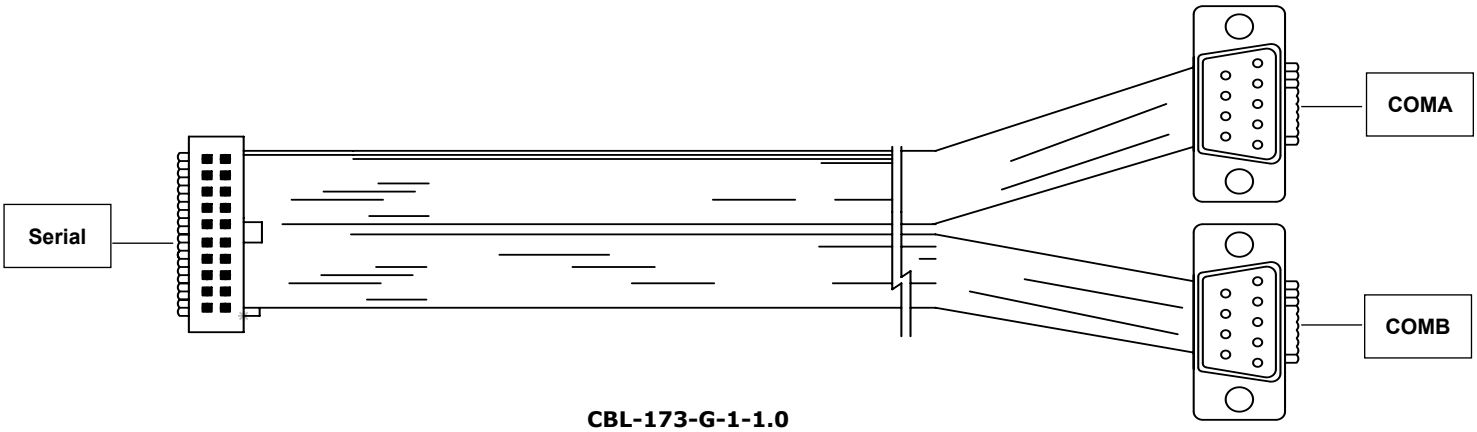
Revision B PCB products require a wire-wrap jumper from 1-4.

RS-485 Termination and Biasing Resistors		
TX/RX (100): Places a 100Ω Resistor across the TX/RX+/TX/RX- pair		7-8
TX/RX(300):	Places a 100Ω Resistor from +5V to TX/RX+	5-6
	Places a 100Ω Resistor between TX/RX+ and TX/RX-	7-8
	Places a 100Ω Resistor from Ground to TX/RX-	3-4

Revision B PCB products require a wire-wrap jumper from 1-4.

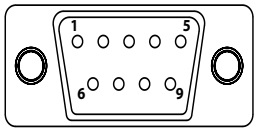


Note: Figure above illustrates the RS-422/RS-485 termination options installed when jumpers are installed on JP3, JP5, JP6, and JP10.



CBL-173-G-1-1.0

COMA, COMB [DB9 Male]



Pin	RS-232	RS-422	RS-485
1	DCD	N/A	N/A
2	RX	TX+	TX/RX+
3	TX	TX-	TX/RX-
4	DTR	N/A	N/A
5	GND	GND	GND
6	DSR	RX+	N/A
7	RTS	RX-	N/A
8	CTR	N/A	N/A
9	RI	N/A	N/A

DIGITAL I/O

Digital I/O Connectors

These 48 lines of digital I/O are terminated through two 50-pin connectors at **J1** and **J7**. The **J1** connector handles I/O ports 0 through 2 while **J7** handles ports 3 through 5.

Note: Pin 49 on each connector can supply +5V to the I/O rack.

J1, J7 - Digital I/O

Visual Index

PCB Connector: TEKA SRC225C425M126-0 (J1, J7)
Mating Connector: ITW-PANCON 050-050-455A

J1 (Ports 0/1/2)

GND	50	49	+5V
GND	48	47	Port 0 Bit 0
GND	46	45	Port 0 Bit 1
GND	44	43	Port 0 Bit 2
GND	42	41	Port 0 Bit 3
GND	40	39	Port 0 Bit 4
GND	38	37	Port 0 Bit 5
GND	36	35	Port 0 Bit 6
GND	34	33	Port 0 Bit 7
GND	32	31	Port 1 Bit 0
GND	30	29	Port 1 Bit 1
GND	28	27	Port 1 Bit 2
GND	26	25	Port 1 Bit 3
GND	24	23	Port 1 Bit 4
GND	22	21	Port 1 Bit 5
GND	20	19	Port 1 Bit 6
GND	18	17	Port 1 Bit 7
GND	16	15	Port 2 Bit 0
GND	14	13	Port 2 Bit 1
GND	12	11	Port 2 Bit 2
GND	10	9	Port 2 Bit 3
GND	8	7	Port 2 Bit 4
GND	6	5	Port 2 Bit 5
GND	4	3	Port 2 Bit 6
GND	2	1	Port 2 Bit 7

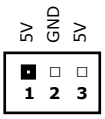
J7 (Ports 3/4/5)

Port 5 Bit 7	1	2	GND
Port 5 Bit 6	3	4	GND
Port 5 Bit 5	5	6	GND
Port 5 Bit 4	7	8	GND
Port 5 Bit 3	9	10	GND
Port 5 Bit 2	11	12	GND
Port 5 Bit 1	13	14	GND
Port 5 Bit 0	15	16	GND
Port 4 Bit 7	17	18	GND
Port 4 Bit 6	19	20	GND
Port 4 Bit 5	21	22	GND
Port 4 Bit 4	23	24	GND
Port 4 Bit 3	25	26	GND
Port 4 Bit 2	27	28	GND
Port 4 Bit 1	29	30	GND
Port 4 Bit 0	31	32	GND
Port 3 Bit 7	33	34	GND
Port 3 Bit 6	35	36	GND
Port 3 Bit 5	37	38	GND
Port 3 Bit 4	39	40	GND
Port 3 Bit 3	41	42	GND
Port 3 Bit 2	43	44	GND
Port 3 Bit 1	45	46	GND
Port 3 Bit 0	47	48	GND
+5V	49	50	GND

The I/O connectors can provide +5V to an I/O rack for miscellaneous purposes by jumpering **JP15** and **JP16**. When **JP15** is jumpered (1-2), +5V is provided at pin 49 of **J1.** When **JP16** is jumpered (1-2), then +5V is provided at pin 49 of **J7**. It is the user's responsibility to limit current to a safe value (less than 400 mA) to avoid damaging the CPU board.

JP15 - Digital I/O VCC (for J1)

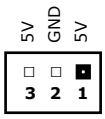
JP15



+5V is provided at pin 49 of **J1**	1-2
No Power at Pin 49 of **J1** (default)	OPEN

JP16 - Digital I/O VCC (for J7)

JP16



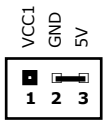
+5V is provided at pin 49 of **J7**	1-2
No Power at Pin 49 of **J7** (default)	OPEN

JP13/JP14 - Pull-Up Resistor

The jumpers **JP13** and **JP14** are used to select the pull-up resistor source for the Digital I/O on **J1** and **J7**, respectively. The system's +5V or an externally supplied VCC can be selected for each port as shown in the pinouts below. The DIO ports are grouped as three 8-bit registers. There is only one VCC jumper for each port which forces all the bits of the port to the same maximum input level.

JP13 - Pull-up Resistor (for J1)

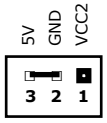
JP13



Pull-up Resistor source for +5V (default)	2-3
No Pull-up Resistor	OPEN
Pull-up Resistor source for VCC1 provided at **J8**	1-2

JP14 - Pull-up Resistor (for J7)

JP14

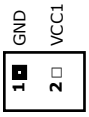


Pull-up Resistor source for +5V (default)	2-3
No Pull-up Resistor	OPEN
Pull-up Resistor source for VCC2 provided at **J9**	1-2

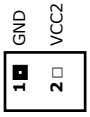
J8/J9 - External Reference Voltage

External voltage can be supplied at **J8** (**J1** Ports 0/1/2) and **J9** (**J7** Ports 3/4/5). If a different pull-up source is required, this source must be under 30 VDC.

J8
J1 Ports (0/1/2)



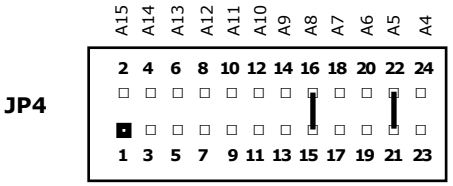
J9
J7 Ports (3/4/5)



JP4 - DIO Base Address

Visual Index

The PCM-SDIO board uses the jumper **JP4** to select the Digital I/O base address. The base address can be moved to any 16 byte boundary in the x86 I/O address space. The base address is selected by installing jumpers to represent the binary address. When a jumper is installed, the bit represents a binary 1 and when uninstalled, it represents a binary 0.



Installed Jumper = 1
Open Jumper = 0

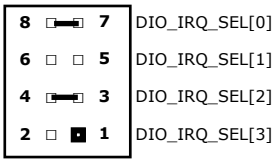
*The jumper reference above represents **120H**.

JP1 - Digital I/O Interrupt Selection

Visual Index

The PCM-SDIO board uses the jumper **JP1** to select the Digital I/O interrupt. The interrupt is chosen by installing jumpers to represent the binary number of the desired interrupt. For more information on choosing a binary number, see the Digital I/O Interrupt Map section below.

JP1



Installed Jumper = 1
Open Jumper = 0

*The jumper reference above represents **IRQ5**.

Digital I/O Interrupt Map (JP1)

Digital I/O interrupts are chosen by installing jumpers on **JP1** to represent the binary number of the desired interrupt. The table below lists IRQ resources as used by the PCM-SDIO.

JP1 DIO IRQ Selection	
Binary	**IRQ**
0000	Not Used
0001	Not Used
0010	Not Used
0011	IRQ3
0100	IRQ4
0101	IRQ5
0110	IRQ6
0111	IRQ7
1000	Not Used
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	Not Used
1110	IRQ14
1111	IRQ15

Register Definitions (WS16C48)

The PCM-SDIO uses the WinSystems exclusive ASIC device, the WS16C48. This device provides 48 lines of digital I/O. There are 16 unique registers within the WS16C48. The following table summarizes the registers, and the text that follows provides details on each of the internal registers.

I/O Address Offset	Page 0	Page 1	Page 2	Page 3
00H (J1)	Port 0 I/O	Port 0 I/O	Port 0 I/O	Port 0 I/O
01H (J1)	Port 1 I/O	Port 1 I/O	Port 1 I/O	Port 1 I/O
02H (J1)	Port 2 I/O	Port 2 I/O	Port 2 I/O	Port 2 I/O
03H (J7)	Port 3 I/O	Port 3 I/O	Port 3 I/O	Port 3 I/O
04H (J7)	Port 4 I/O	Port 4 I/O	Port 4 I/O	Port 4 I/O
05H (J7)	Port 5 I/O	Port 5 I/O	Port 5 I/O	Port 5 I/O
06H	Int_Pending	Int_Pending	Int_Pending	Int_Pending
07H	Page/Lock	Page/Lock	Page/Lock	Page/Lock
08H	Reserved	Pol_0	Enab_0	Int_ID0
09H	Reserved	Pol_1	Enab_1	Int_ID1
0AH	Reserved	Pol_2	Enab_2	Int_ID2

Register Details

Port 0 through 5 I/O

Each I/O bit in each of the six ports can be individually programmed for input or output. Writing a **0** to a bit position causes the corresponding output pin to go to a high-impedance state (pulled high by external 10 KΩ resistors). This allows it to be used as an input. When used in the input mode, a read reflects the inverted state of the I/O pin, such that a high on the pin will read as a **0** in the register. Writing a **1** to a bit position causes that output pin to sink current (up to 12 mA), effectively pulling it low.

INT_PENDING

This read-only register reflects the combined state of the INT_ID0 through INT_ID2 registers. When any of the lower three bits are set, it indicates that an interrupt is pending on the I/O port corresponding to the bit position(s) that are set. Reading this register allows an Interrupt Service Routine to quickly determine if any interrupts are pending and which I/O port has a pending interrupt.

PAGE/LOCK

This register serves two purposes. The upper two bits select the register page in use as shown here:

D7	D6	Page
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

Bits 5-0 allow for locking the I/O ports. A **1** written to the I/O port position will prohibit further writes to the corresponding I/O port.

POL0 - POL2

These registers are accessible when Page 1 is selected. They allow interrupt polarity selection on a port–by–port and bit-by-bit basis. Writing a **1** to a bit position selects the rising edge detection interrupts while writing a **0** to a bit position selects falling edge detection interrupts.

ENAB0 - ENAB2

These registers are accessible when Page 2 is selected. They allow for port-by-port and bit-by-bit enabling of the edge detection interrupts. When set to a **1**, the edge detection interrupt is enabled for the corresponding port and bit. When cleared to **0**, the bit's edge detection interrupt is disabled. Note that this register can be used to individually clear a pending interrupt by disabling and re-enabling the pending interrupt.

INT_ID0 – INT_ID2

These registers are accessible when Page 3 is selected. They are used to identify currently pending edge interrupts. A bit when read as a **1** indicates that an edge of the polarity programmed into the corresponding polarity register has been recognized. Note that a write to this register (value ignored) clears ALL of the pending interrupts in this register.

PCB Connector: **TEKA PC232-A-1A7-M (J2)**
TEKA PC220-A-1A7-M (J4)

The PC/104 bus is electrically equivalent to the 16-bit ISA bus. Standard PC/104 I/O cards can be populated on PCM-SDIO's connectors, located at **J4** and **J2**. The interface does not support hot swap capability. The PC/104 bus connector pin definitions are provided below for reference. Refer to the PC/104 Bus Specification for specific signal and mechanical specifications.

J4
(C/D)

GND	**D0**	**C0**	GND
MEMCS16#	**D1**	**C1**	SBHE#
IOCS16#	**D2**	**C2**	LA23
IRQ10	**D3**	**C3**	LA22
IRQ11	**D4**	**C4**	LA21
IRQ12	**D5**	**C5**	LA20
IRQ15	**D6**	**C6**	LA19
IRQ14	**D7**	**C7**	LA18
DACK0#	**D8**	**C8**	LA17
DRQ0	**D9**	**C9**	MEMR#
DACK5#	**D10**	**C10**	MEMW#
DRQ5	**D11**	**C11**	SD8
DACK6#	**D12**	**C12**	SB9
DRQ6	**D13**	**C13**	SD10
DACK7#	**D14**	**C14**	SD11
DRQ7	**D15**	**C15**	SD12
+5V	**D16**	**C16**	SD13
MASTER#	**D17**	**C17**	SD14
GND	**D18**	**C18**	SD15
GND	**D19**	**C19**	KEY

J2
(A/B)

IOCHK#	**A1**	**B1**	GND
SD7	**A2**	**B2**	RESET
SD6	**A3**	**B3**	+5V
SD5	**A4**	**B4**	IRQ
SD4	**A5**	**B5**	-5V
SD3	**A6**	**B6**	DRQ2
SD2	**A7**	**B7**	-12V
SD1	**A8**	**B8**	SRDY#
SD0	**A9**	**B9**	+12V
IOCHRDY	**A10**	**B10**	KEY
AEN	**A11**	**B11**	SMEMW#
SA19	**A12**	**B12**	SMEMR#
SA18	**A13**	**B13**	IOW#
SA17	**A14**	**B14**	IOR#
SA16	**A15**	**B15**	DACK3#
SA15	**A16**	**B16**	DRQ3
SA14	**A17**	**B17**	DACK1#
SA13	**A18**	**B18**	DRQ1
SA12	**A19**	**B19**	REFRESH#
SA11	**A20**	**B20**	BCLK
SA10	**A21**	**B21**	IRQ7
SA9	**A22**	**B22**	IRQ6
SA8	**A23**	**B23**	IRQ5
SA7	**A24**	**B24**	IRQ4
SA6	**A25**	**B25**	IRQ3
SA5	**A26**	**B26**	DACK2#
SA4	**A27**	**B27**	TC
SA3	**A28**	**B28**	BALE
SA2	**A29**	**B29**	+5V
SA1	**A30**	**B30**	OSC
SA0	**A31**	**B31**	GND
GND	**A32**	**B32**	GND

= Active Low Signal

NOTES:

1. Rows C and D are not required on 8-bit modules.
2. B10 and C19 are key locations. WinSystems uses key pins as connections to GND.
3. Signal timing and function are as specified in ISA specification.
4. Signal source/sink current differ from ISA values.

CABLES

Part Number	Description
CBL-115-4	4-ft., Opto rack interface
CBL-129-1	6-in., 50-pin to 50-pin 0.10-in. ribbon cable
CBL-129-4	48-in., 50-pin to 50-pin 0.10-in. ribbon cable
CBL-173-G-1-1.0	20-pin ribbon to two 9-pin male D connector adapter
CBL-208-5	13-in., 50-pin to 50-pin 0.10-in. ribbon cable

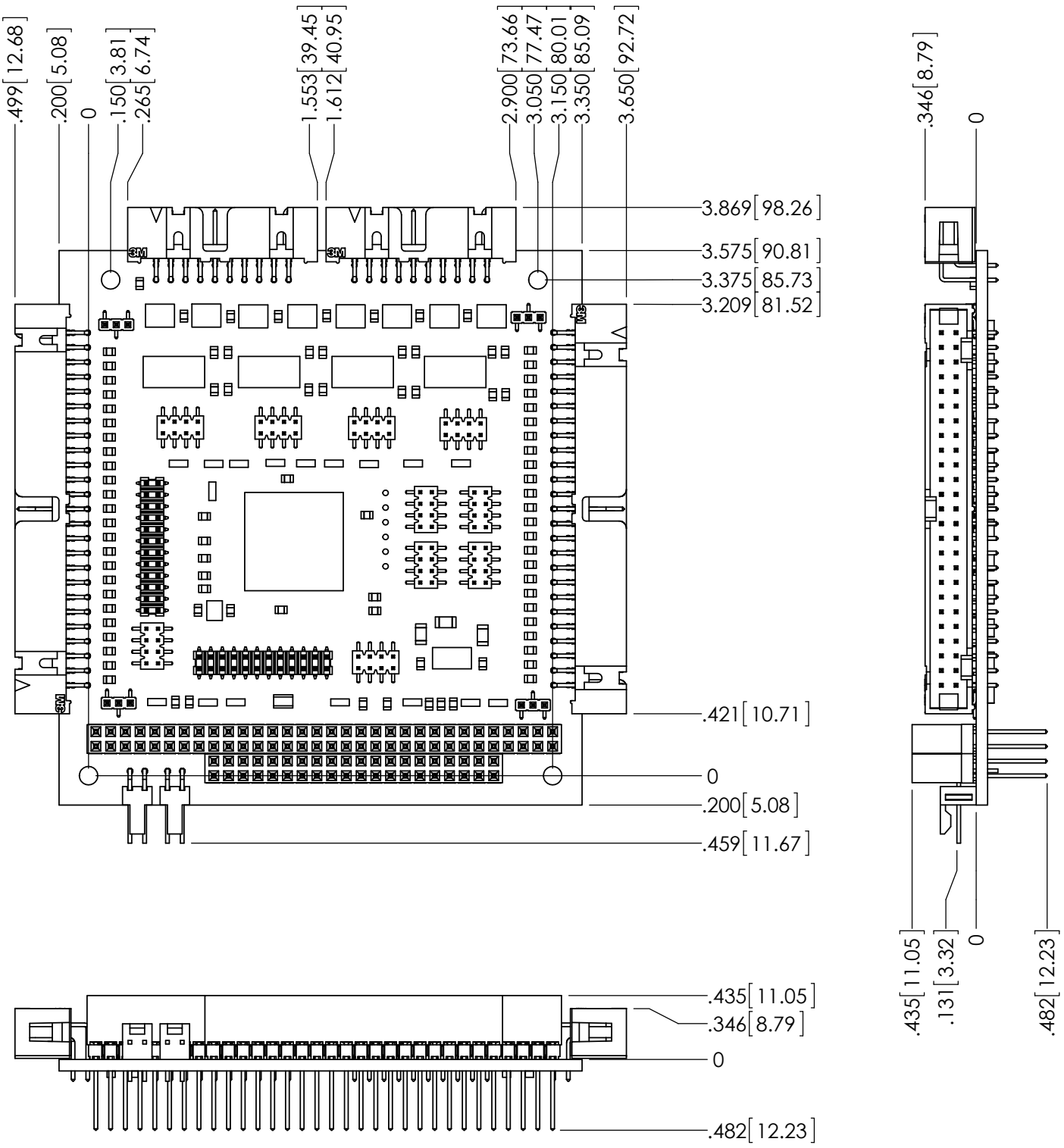
SOFTWARE DRIVERS

Software Drivers	
Application Note: Using Serial I/O with Shared Interrupt under Linux 2.6 kernel	UsingMultiportSerialCardsLinux_2_6_x.pdf
DOS Example C Functions	uio48a.zip
Linux Drivers - Kernel 2.2, 2.4	linux_uio48_96.zip
Linux Drivers - Kernel 2.6.10-17	uio48io_kernel_2.6.10.zip
Linux Drivers - Kernel 2.6.36	uio48io_kernel_2.6.36.zip
Simple C Routine using receive interrupt	8250inta.zip
Windows NT/2000/XP Registry changes for using shared interrupts with PCM-COM4A and PCM-COM8	pcom8ex.pdf
Windows XP - WS16C48 Digital I/O	wsuio48_96xp.zip

SPECIFICATIONS

Electrical		
VCC	+5V required	
	Vout	5 to 30 VDC
	Iout (source)	500 µA - 5mA
	Iin (sink)	12 mA
	Vin	5 to 30 VDC
MTBF	8,103,486 hours	
Mechanical		
Dimensions	3.60” x 3.80” (90 mm x 96 mm)	
Weight	3.2 oz (90.7 g)	
Environmental		
Operating Temperature	-40°C to 85°C	

MECHANICAL DRAWING



PCM-SDIO MECHANICAL

APPENDIX - A

BEST PRACTICES

POWER SUPPLY

The power supply and how it is connected to the Single Board Computer (SBC) is very important.

Avoid Electrostatic Discharge (ESD)
Only handle the SBC and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

Power Supply Budget
Evaluate your power supply budget. It is usually good practice to budget 2X the typical power requirement for all of your devices.

Zero-Load Power Supply
Use a zero-load power supply whenever possible. A zero-load power supply does not require a minimum power load to regulate. If a zero-load power supply is not appropriate for your application, then verify that the single board computer's typical load is not lower than the power supply's minimum load. If the single board computer does not draw enough power to meet the power supply's minimum load, then the power supply will not regulate properly and can cause damage to the SBC.

Use Proper Power Connections (Voltage)
When verifying the voltage, you should always measure it at the power connector on the SBC. Measuring at the power supply does not account for voltage drop through the wire and connectors.

The single board computer requires +5V (±5%) to operate. Verify the power connections. Incorrect voltages can cause catastrophic damage.

Populate all of the +5V and ground connections. Most single board computers will have multiple power and ground pins, and all of them should be populated. The more copper connecting the power supply to the single board computer the better.

Adjusting Voltage
If you have a power supply that will allow you to adjust the voltage, it is a good idea to set the voltage at the power connector of the SBC to 5.1V. The SBC can tolerate up to 5.25V, so setting your power supply to provide 5.1V is safe and allows for a small amount of voltage drop that will occur over time as the power supply ages and the connector contacts oxidize.

Power Harness
Minimize the length of the power harness. This will reduce the amount of voltage drop between the power supply and the single board computer.

Gauge Wire
Use the largest gauge wire that you can. Most connector manufacturers have a maximum gauge wire they recommend for their pins. Try going one size larger; it usually works and the extra copper will help your system perform properly over time.

Contact Points
WinSystems' boards mostly use connectors with gold finish contacts. Gold finish contacts are used exclusively on high speed connections. Power and lower speed peripheral connectors may use a tin finish as an alternative contact surface. It is critical that the contact material in the mating connectors is matched properly (gold to gold and tin to tin). Contact areas made with dissimilar metals can cause oxidation/corrosion resulting in unreliable connections.

Pin Contacts
Often the pin contacts used in cabling are not given enough attention. The ideal choice for a pin contact would include a design similar to Molex's or Trifurcons' design, which provides three distinct points to maximize the contact area and improve connection integrity in high shock and vibration applications.

POWER DOWN

Make sure the system is **completely off/powered down** before connecting anything.

Power Supply OFF
The power supply should always be off before it is connected to the single board computer.

I/O Connections OFF
I/O Connections should also be off before connecting them to the single board computer or any I/O cards. Connecting hot signals can cause damage whether the single board computer is powered or not.

MOUNTING AND PROTECTING THE SINGLE BOARD COMPUTER

Do Not Bend or Flex the SBC
Never bend or flex the single board computer. Bending or flexing can cause irreparable damage. Single board computers are especially sensitive to flexing or bending around Ball-Grid-Array (BGA) devices. BGA devices are extremely rigid by design and flexing or bending the single board computer can cause the BGA to tear away from the printed circuit board.

Mounting Holes
The mounting holes are plated on the top, bottom and through the barrel of the hole and are connected to the single board computer's ground plane. Traces are often routed in the inner layers right below, above or around the mounting holes.

Never use a drill or any other tool in an attempt to make the holes larger.

Never use screws with oversized heads. The head could come in contact with nearby components causing a short or physical damage.

Never use self-tapping screws; they will compromise the walls of the mounting hole.

Never use oversized screws that cut into the walls of the mounting holes.

Always use all of the mounting holes. By using all of the mounting holes you will provide the support the single board computer needs to prevent bending or flexing.

Plug or Unplug Connectors Only on Fully Mounted Boards
Never plug or unplug connectors on a board that is not fully mounted. Many of the connectors fit rather tightly and the force needed to plug or unplug them could cause the single board computer to be flexed.

Avoid cutting of the SBC
Never use star washers or any fastening hardware that will cut into the single board computer.

Avoid Overtightening of Mounting Hardware
Causing the area around the mounting holes to compress could damage interlayer traces around the mouting holes.

Use Appropriate Tools
Always use tools that are appropriate for working with small hardware. Large tools can damage components around the mounting holes.

Placing the SBC on Mounting Standoffs
Be careful when placing the single board computer on the mounting standoffs. Sliding the board around until the standoffs are visible from the top can cause component damage on the bottom of the single board computer.

Avoid Conductive Surfaces
Never allow the single board computer to be placed on a conductive surface. Almost all single board computers use a battery to backup the clock-calendar and CMOS memory. A conductive surface such as a metal bench can short the battery causing premature failure.

ADDING PC/104 BOARDS TO YOUR STACK

Be careful when adding PC/104 boards to your stack.

Never allow the power to be turned on when a PC/104 board has been improperly plugged onto the stack. It is possible to misalign the PC/104 card and leave a row of pins on the end or down the long side hanging out of the connector. If power is applied with these pins misaligned, it will cause the I/O board to be damaged beyond repair.

OPERATIONS / PRODUCT MANUALS

Every single board computer has an Operations manual or Product manual.

Manual Updates
Operations/Product manuals are updated often. Periodicially check the WinSystems website (http://www.winsystems.com) for revisions.

Check Pinouts
Always check the pinout and connector locations in the manual before plugging in a cable. Many single board computers will have identical headers for different functions and plugging a cable into the wrong header can have disastrous results.

Contact an Applications Engineer with questions
If a diagram or chart in a manual does not seem to match your board, or if you have additional questions, contact your Applications Engineer.

WARRANTY INFORMATION

(http://www.winsystems.com/company/warranty.cfm)

WinSystems warrants to Customer that for a period of two (2) years from the date of shipment any Products and Software purchased or licensed hereunder which have been developed or manufactured by WinSystems shall be free of any material defects and shall perform substantially in accordance with WinSystems' specifications therefore. With respect to any Products or Software purchased or licensed hereunder which have been developed or manufactured by others, WinSystems shall transfer and assign to Customer any warranty of such manufacturer or developer held by WinSystems, provided that the warranty, if any, may be assigned. Notwithstanding anything herein to the contrary, this warranty granted by WinSystems to the Customer shall be for the sole benefit of the Customer, and may not be assigned, transferred or conveyed to any third party. The sole obligation of WinSystems for any breach of warranty contained herein shall be, at its option, either (i) to repair or replace at its expense any materially defective Products or Software, or (ii) to take back such Products and Software and refund the Customer the purchase price and any license fees paid for the same. Customer shall pay all freight, duty, broker's fees, insurance charges for the return of any Products or Software to WinSystems under this warranty. WinSystems shall pay freight and insurance charges for any repaired or replaced Products or Software thereafter delivered to Customer within the United States. All fees and costs for shipment outside of the United States shall be paid by Customer. The foregoing warranty shall not apply to any Products of Software which have been subject to abuse, misuse, vandalism, accidents, alteration, neglect, unauthorized repair or improper installations.

THERE ARE NO WARRANTIES BY WINSYSTEMS EXCEPT AS STATED HEREIN, THERE ARE NO OTHER WARRANTIES EXPRESS OR IMPLIED INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, IN NO EVENT SHALL WINSYSTEMS BE LIABLE FOR CONSEQUENTIAL, INCIDENTIAL OR SPECIAL DAMAGES INCLUDING, BUT NOT LIMITED TO, DAMAGES FOR LOSS OF DATA, PROFITS OR GOODWILL. WINSYSTEMS' MAXIMUM LIABILITY FOR ANY BREACH OF THIS AGREEMENT OR OTHER CLAIM RELATED TO ANY PRODUCTS, SOFTWARE, OR THE SUBJECT MATTER HEREOF, SHALL NOT EXCEED THE PURCHASE PRICE OR LICENSE FEE PAID BY CUSTOMER TO WINSYSTEMS FOR THE PRODUCTS OR SOFTWARE OR PORTION THEREOF TO WHICH SUCH BREACH OR CLAIM PERTAINS.

WARRANTY SERVICE

1. To obtain service under this warranty, obtain a return authorization number. In the United States, contact the WinSystems' Service Center for a return authorization number. Outside the United States, contact your local sales agent for a return authorization number.

2. You must send the product postage prepaid and insured. You must enclose the products in an anti-static bag to protect from damage by static electricity. WinSystems is not responsible for damage to the product due to static electricity.