OPERATIONS MANUAL
PCM-POST

REVISION HISTORY
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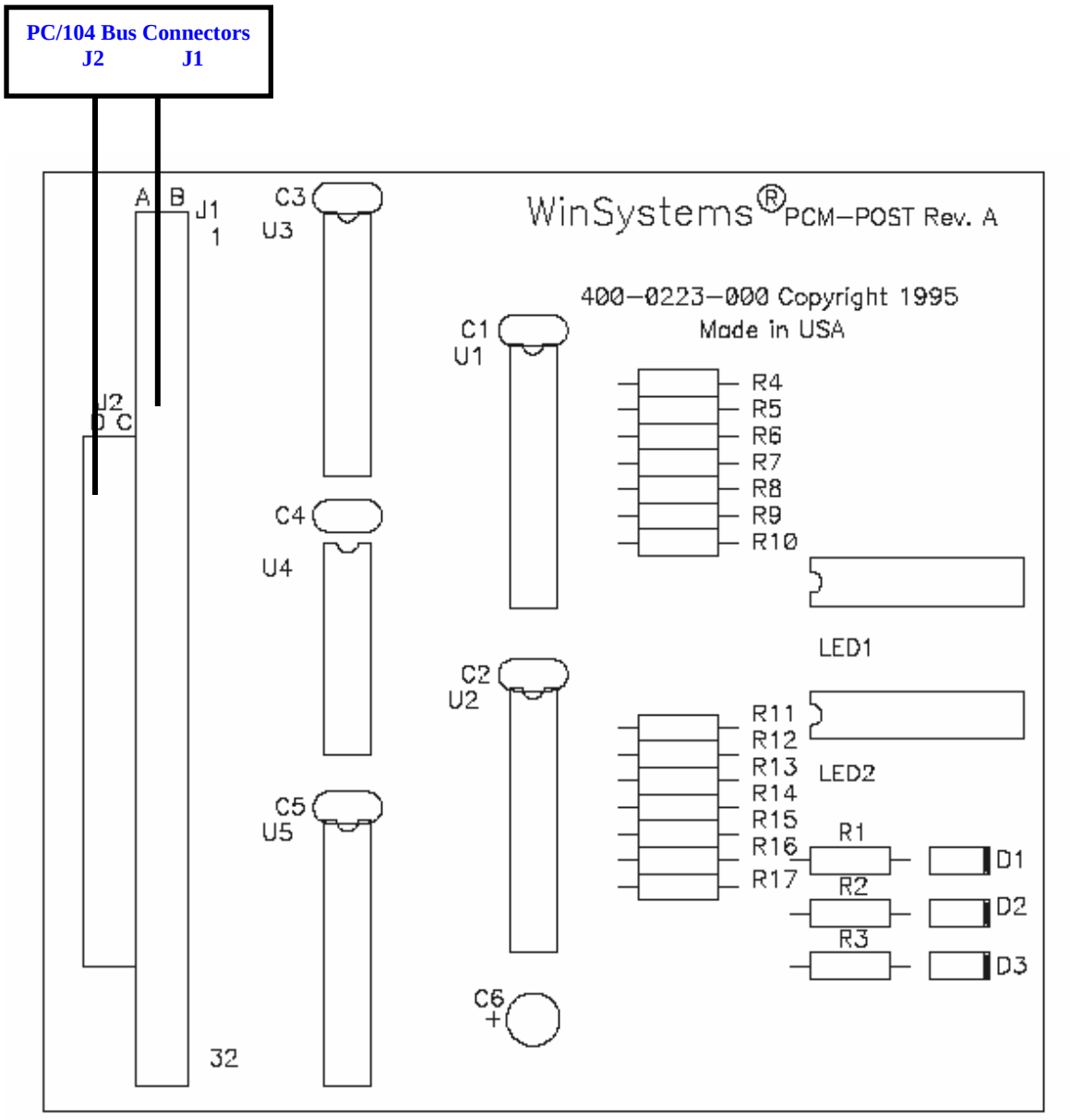
Visual Index – Quick Reference

For the convenience of the user, a copy of the Visual Index has been provided with direct links to connector and jumper configuration data.



1 General Information

1.1 Features

- Power-on System Test (POST) PC/104 module
- BIOS Diagnostic POST codes shown on two 7-segment displays
- Supports user diagnostic and status codes
- Light Emitting Diodes (LEDs) on +5, +12, and -12 volt lines provide visual status of power supplies
- Only +5 volt supply required for operation
- -40°C to +85°C operating temperature

The PCM-POST PC/104 module is a helpful diagnostic tool used for isolating power-up problems occasionally found in AT-compatible single board computers. During boot-up, the ROM BIOS (Basic Input/Output System) routines test the board's status. If a problem is found, it immediately defines and displays a status code on the digital display.

1.2 Functional Capability

PC/104 Bus Interface - The PCM-POST module is a fully compliant PC/104 board decoding a single I/O port at 80 hexadecimal.

BIOS Post Codes - The BIOS on most PC-AT compatible single board computers output Power On Self Test (POST) codes during the power-up sequence. A 2-digit HEX code is output prior to each major initialization or diagnostic step once the system is running. If the diagnostic or initialization sequence fails or locks-up, the displayed code indicates the type of operation attempted when the failure occurred. This information can be very useful in troubleshooting a system that for some reason is not booting correctly.

The PCM-POST has two seven segment displays which decode these 2-digit HEX diagnostic status values. The POST codes for the BIOS used in WinSystems' Embedded PCs are listed in the PCM-POST operation manual for easy reference.

Custom Diagnostic/Status Codes - The PCM-POST module is also useful to display an application program's status and can be used for software debugging in real-time where more intrusive debugging methods are not available or practical.

Monitor LEDs - Three LEDs on the PCM-POST provide a visual status of the power supplies. A red, green, and yellow LED is used for easy visual reference for the respective +5 volt, +12 volt and -12 volt supply lines.

1.3 Specifications

Electrical

PC/104 Bus: 8-bit, stackthrough
Power: +5V ±5% @ 175mA typ.(fully illuminated)
+12V +5% @ 15mA (for onboard LED)
-12V +5% @ 15mA (for onboard LED)

Mechanical

Dimensions: 3.6” x 3.8” x 0.6” (90mm x 96mm x 15mm)
Weight: 2.4 oz. (g)
Connectors:
PCM-POST: 32-pin double row, 0.025" square posts

Environmental

Operational Temperature: -40°C to +85°C
MTBF: 77.3 years

2 PCM-POST Technical Reference

2.1 Introduction

This section of the manual is intended to provide the necessary information regarding configuration and usage of the PCM-POST board. WinSystems maintains a Technical Support Group to help answer questions regarding usage, or programming of the board. For answers to questions not adequately addressed in this manual, contact Technical Support at (817) 274-7553 between 8AM and 5PM Central Time.

2.2 PC/104 Bus Description

(back to Visual Index)

The PCM- POST Module is a PC/104 com pliant board decoding a single I/O port at 80H. The Bus signal assignments for the J1 and J2 PC/104 connectors are shown here:

J1

GND	B1 o o A1	IOCHK		
RESET	B2 o o A2	BD7		
+5V	B3 o o A3	BD6		
IRQ9	B4 o o A4	BD5		
-5V	B5 o o A5	BD4		
DRQ2	B6 o o A6	BD3		
-12V	B7 o o A7	BD2		
0WS	B8 o o A8	BD1		
+12V	B9 o o A9	BD0		
GND	B10 o o A10	IOCHRDY		
MEMW	B11 o o A11	AEN		
MEMR	B12 o o A12	SA19		
IOW	B13 o o A13	SA18		
IOR	B14 o o A14	SA17		
DACK3	B15 o o A15	SA16		
DRQ3	B16 o o A16	SA15		
DACK1	B17 o o A17	SA14		
DRQ1	B18 o o A18	SA13		
REFRESH	B19 o o A19	SA12		
SYSCLOCK	B20 o o A20	SA11		
IRQ7	B21 o o A21	SA10		
IRQ6	B22 o o A22	SA9		
IRQ5	B23 o o A23	SA8		
IRQ4	B24 o o A24	SA7		
IRQ3	B25 o o A25	SA6		
DACK2	B26 o o A26	SA5		
TC	B27 o o A27	SA4		
BALE	B28 o o A28	SA3		
+5V	B29 o o A29	SA2		
OSC	B30 o o A30	SA1		
GND	B31 o o A31	SA0		
GND	B32 o o A32	GND		

J2

GND	C0 o o D0	GND
SBHE	C1 o o D1	MEMCS16
LA23	C2 o o D2	IOCS16
LA22	C3 o o D3	IRQ10
LA21	C4 o o D4	IRQ11
LA20	C5 o o D5	IRQ12
LA19	C6 o o D6	IRQ15
LA18	C7 o o D7	IRQ14
LA17	C8 o o D8	DACK0
MEMR	C9 o o D9	DRQ0
MEMW	C10 o o D10	DACK5
SD8	C11 o o D11	DRQ5
SD9	C12 o o D12	DACK6
SD10	C13 o o D13	DRQ6
SD11	C14 o o D14	DACK7
SD12	C15 o o D15	DRQ7
SD13	C16 o o D16	VCC
SD14	C17 o o D17	MASTER
SD15	C18 o o D18	GND
KEY	C19 o o D19	GND

APPENDIX A

AMI BIOS Post Codes

Several WinSystems boards use BIOS' Supplied by AMI. These products are:

LPM/MCM-SX386/486SLC
SAT-386SX/486SLC
SBC-386SX/486SLC

The BIOS post codes for these boards are shown in the following table.

Post Code	Description
01	Processor register test about to start, and NMI to be disabled.
02	NMI is disabled. Power on delay starting.
03	Power on delay complete. Any initialization before keyboard BAT is in process.
04	Initialization before keyboard BAT is complete. Reading keyboard SYS bit, to check soft reset or power on.
05	Soft reset/power on determined. Going to enable ROM. i.e. disable Shadow RAM or cache if any.
06	ROM enabled. Calculating ROM BIOS checksum, and waiting for KB controller input buffer to be free.
07	ROM BIOS checksum passed, KB controller I/B free. Going to issue the BAT command to keyboard controller.
08	BAT command to keyboard controller is issued. Going to verify the BAT command.
09	Keyboard controller BAT result verified. Keyboard command byte to be written next.
0A	Keyboard command byte code is issued. Going to write command data byte.
0B	Keyboard controller command byte is written. Going to issue Pin-23, 24 blocking/unblocking command.

0C	Pin 23, 24 on keyboard controller is blocked/unblocked. NOP command of keyboard controller to be issued next.
0D	NOP command processing is done. CMOS shutdown register test to be done next.
0E	CMOS shutdown R/W register test passed. Going to calculate CMOS checksum, and update DIAG byte.
0F	CMOS checksum calculation is done, DIAG byte written. CMOS init to begin (if "INIT CMOS IN EVERY BOOT IS SET").
10	CMOS initialization done (if any). CMOS status register about to init Date and Time.
11	CMOS status register initialized. Going to disable DMA and interrupt controllers.
12	DMA controllers 1 and 2 and interrupt controllers 1 and 2 disabled. About to disable Video display and init port-B.
13	Video display disabled and port-B initialized. Chipset init/auto memory detection about to begin.
14	Chipset initialization/auto memory detection over. 8254 timer test about to start.
15	Ch-2 timer test halfway. 8254 Ch-2 timer test to be complete.
16	Ch-2 timer test complete. 8254 Ch-1 timer test to be complete.
17	Ch-1 timer test over. 8254 Ch-0 timer test to be complete.
18	Ch-0 timer test over. About to start memory refresh.
19	Memory refresh started. Memory refresh test to be done next.
1A	Memory refresh line is toggling. Going to check 15 micro-second ON/OFF time.
1B	Memory refresh period 30 micro-second test complete. Base 64K memory test about to start.
20	Base 64K memory test started. Address line test to be done next.
21	Address line test passed. Going to toggle parity.

22	Toggle parity over. Going to sequential data R/W test.
23	Base 64K sequential data R/W test passed. Any setup before interrupt vector init about to start.
24	Setup required before vector initialization complete. Interrupt vector initialization about to begin.
25	Interrupt vector initialization complete. Going to read I/O port of 8042 for turbo switch (if any)
26	I/O port of 8042 is read. Going to initialize global data area for turbo switch.
27	Global data initialization is over. Any initialization after interrupt vector is to be done next.
28	Initialization after interrupt vector is complete. Going to monochrome mode setting.
29	Monochrome mode setting is done. Going for Color mode setting.
2A	Color mode setting is done. About to go for toggle parity before optional ROM test.
2B	Toggle parity over. About to give control for any setup required before optional video ROM check.
2C	Processing before video ROM control is done. About to look for optional video ROM and give control.
2D	Optional video ROM control is done. About to give control to do any processing after video ROM returns control.
2E	Return from processing after the video ROM control. If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/w test about to begin.
30	Display memory R/W test passed. About to look for retrace checking.
31	Display memory R/W test or retrace checking failed. About to do alternate display memory R/W test.
32	Alternate display memory R/W test passed. About to look for alternate display retrace checking.
33	Video display checking over. Verification of display type with switch setting and actual card to begin.

34	Verification of display adapter done. Display mode to be set next.
35	Display mode set complete. BIOS ROM data area about to be checked.
36	BIOS ROM data area complete. Going to set cursor for power on message.
37	Cursor setting for power on message is complete. Going to display the power on message.
38	Power on message display complete. Going to read new cursor position.
39	New cursor position read saved. Going to display the reference string.
3A	Reference string display is over. Going to display the "Hit <ESC>" message.
3B	"Hit <ESC>" message displayed. Virtual memory test about to start.
40	Preparation for virtual memory test started. Going to verify from video memory.
41	Return after verifying from display memory. Going to prepare the descriptor tables.
42	Descriptor tables prepared. Going to enter virtual mode for memory test.
43	Entered into virtual mode. Going to enable interrupts for diagnostic mode.
44	Interrupts enabled (if diagnostic switch is on). Going to initialize data to check memory wrap around 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding total system memory size.
46	Memory wrap around test done. Memory size calculation complete. About to go for writing patterns to test memory.
47	Patterns to be tested written in extended memory. Going to write patterns in Base 64K memory.
48	Patterns written in base memory. Going to find amount of memory below 1M.
49	Amount of memory below 1M found and verified. Going to find amount of memory above 1M.
4A	Amount of memory above 1M found and verified. Going for BIOS ROM data area check.

4B	BIOS data area check over. Going to check <ESC> and to clear memory below 1M for soft reset.
4C	Memory below 1M cleared (soft reset). Going to clear memory above 1M.
4D	Memory above 1M cleared (soft reset). Going to save the memory size.
4E	Memory test started (hard reset). About to display the first 64K memory test.
4F	Memory size display started. This will be updated during the memory test. Going for sequential and random memory test.
50	Memory test below 1M complete. Going to adjust memory size for relocation or shadowing.
51	Memory size adjusted for relocation/shadowing. Memory test above 1M to follow.
52	memory test above 1M complete. Going to prepare to go back to real mode.
53	CPU registers are saved including memory size. Going to enter into real mode.
54	Shutdown successful, CPU in real mode. Going to restore registers saved during preparation for shutdown.
55	Registers restored. Going to disable gate A20 address line.
56	A20 address line disable complete. BIOS ROM data area to be checked.
57	BIOS ROM data area check halfway. BIOS ROM data area check to be completed.
58	BIOS ROM data area check over. Going to clear "Hit <ESC>" message.
59	"Hit <ESC>" message cleared. "<Wait . . .>" message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. About to verify from display memory.
61	Display memory verification over. About to go for DMA #1 base register test.
62	DMA #1 base register test passed. About to go for DMA #2 base register test.

63	DMA #2 base register passed. About to go for BIOS ROM data area check.
64	BIOS ROM data area check halfway. BIOS ROM data area check to be completed.
65	BIOS ROM data area check over. About to program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. About to initialize the 8259 interrupt controller.
67	8259 initialization over. About to start keyboard test.
80	Keyboard test started. Clearing output buffer, checking stuck key. About to issue keyboard reset command.
81	Keyboard reset error/stuck key found. About to issue keyboard controller interface test command.
82	Keyboard controller interface test over. About to write command byte and init circular buffer.
83	Command byte written, global data init done. About to check for lock-key.
84	Lock-key checking over. About to check for memory size mismatch with CMOS.
85	Memory size check done. About to display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. Going to CMOS setup program.
88	Return from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power on screen message.
8A	First screen message displayed. About to display <Wait . . . >
8B	<Wait . . > message displayed. About to do Main and Video BIOS shadow.
8C	Main and video BIOS shadow successful. Setup options programming after CMOS setup about to start.

8D	Setup options are programmed. Mouse check and init to be done next.
8E	Mouse check and initialization complete. Going for Hard disk, floppy reset.
8F	Floppy check returns that floppy is to be initialized. Floppy setup to follow.
90	Floppy setup is over. Test for hard disk presence to be done.
91	Hard disk presence test complete. Hard disk setup to follow.
92	Hard disk setup complete. About to go for BIOS ROM data area check.
93	BIOS ROM data area check halfway. BIOS ROM data check to be complete.
94	BIOS ROM data area check over. Going to set base and extended memory size.
95	Memory size adjusted for mouse support, hdisk type-47. Going to verify from display memory.
96	Returned after verifying from display memory. Going to do any initializations before C800 optional ROM control.
97	Any initiailization before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control.
99	Any initialization required after optional ROM test is over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address set. Going to do any initialization before co-processor test.
9C	Required initialization before co-processor testing is over. Going to initialize the co-processor next.
9D	Co-processor initialized. Going to do any initialization after co-processor test.

9E	Initialization after co-processor test is complete. Going to check extended keyboard, keyboard ID, and mum-lock.
9F	Extended keyboard check is done, ID flag set, num-lock on/off. Keyboard ID command to be issued next.
A0	Keyboard ID command issued. Keyboard ID flag to be reset.
A1	Keyboard ID flag reset. Cache memory test to follow.
A2	Cache memory test complete. Going to display any soft errors.
A3	Soft error display complete. Going to set typematic rate.
A4	Keyboard typematic rate set. Going to program memory wait states.
A5	Memory wait states programming over. Screen to be cleared next.
A6	Screen cleared. Going to enable parity and NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
00	System configuration is displayed. Going to give control to initialize 19H boot loader.

APPENDIX B

AWARD BIOS Post Codes

WinSystems boards using BIOS' supplied by AWARD are:

SAT-SX/SLC
LBC-486

The BIOS post codes for these boards are shown in the following table.

Post Code	Description
C0	Turn off chipset cache
01	Processor Test 1 - Processor Status Verification, tests the processor status flags, carry zero, sign, overflow.
02	Processor Test 2 - Read/Write Verify of all CPU registers except SS, SP, and BP.
03	Initialize Chips: Disable NMI, PIE, AIE, UEi, SQVW Disable video, parity checking, DMA Reset math coprocessor Clear ALL page registers, CMOS shutdown byte Initialize Timer 0, 1, and 2 Initialize DMA Controllers 0 and 1 Initialize Interrupt Controllers 0 and 1
04	Test memory refresh toggle
05	Blank video, initialize keyboard
07	Test COMS interface and battery status
BE	Chipset Default Initialization: program chipset with power on BIOS defaults
C1	Memory presence test: size onboard memory
C5	Early Shadow: early shadow enable for fast boot
C6	Cache presence test
08	Setup low memory: early chipset initialization Memory presence test OEM chipset routines Clear low 64K memory Test first 64K memory
09	Early Cache Initialization: Cyrix CPU initialization
0A	Setup Interrupt Vector Table

0B	Test CMOS RAM Checksum
0C	Initialize keyboard: detect type of keyboard controller (optional) Set NUM LOCK status
0D	Initialize Video Interface: detect CPU clock Read CMOS location 14h to determine type of video in use Detect and initialize video adapter.
0E	Test Video Memory: write sign-on message to screen Setup shadow RAM - enable shadowing per setup
0F	Test DMA Controller 0 BIOS checksum test, keyboard detect and initialization
10	Test DMA Controller 1
11	Test DMA Page Registers
14	Test Timer Counter 2
15	Test 8259-1 Mask Bits
16	Test 8259-2 Mask Bits
17	Test stuck 8259's interrupt bits
18	Test 8259 interrupt functionality
19	Test stuck NMI bits
1A	Display CPU clock frequency
30	Size system memory
31	Test base and extended memory
3C	Setup enabled
3D	Detect and initialize mouse if present
3E	Setup cache controller
BF	Program chipset with setup values
40	Display virus protect disable or enable
41	Initialize floppy drive and controller
42	initialize hard drive and controller
43	Detect and initialize serial/parallel ports
45	Detect and initialize math coprocessor
4E	Display any non-fatal errors. Enter setup.
4F	Security password check (optional)
50	Write all CMOS values back to RAM and clear screen
51	Pre-boot enable: Enable parity checker Enable NMI, Enable cache before boot
52	Scan and initialize option ROMS
53	Initialize time value
60	Setup virus protect
61	Setup Boot speed
62	Setup MUM LOCK status
63	Boot attempt

B0	Spurious interrupt occurred in protected mode
B1	Spurious NMI occurred
FF	Boot

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