OPERATIONS MANUAL
PCM-ESCC

NOTE: *This manual has been designed and created for use as part of the WinSystems' Technical Manuals CD and/or the WinSystems' website. If this manual or any portion of the manual is downloaded, copied or emailed, the links to additional information (i.e. software, cable drawings) will be inoperable.*

REVISION HISTORY

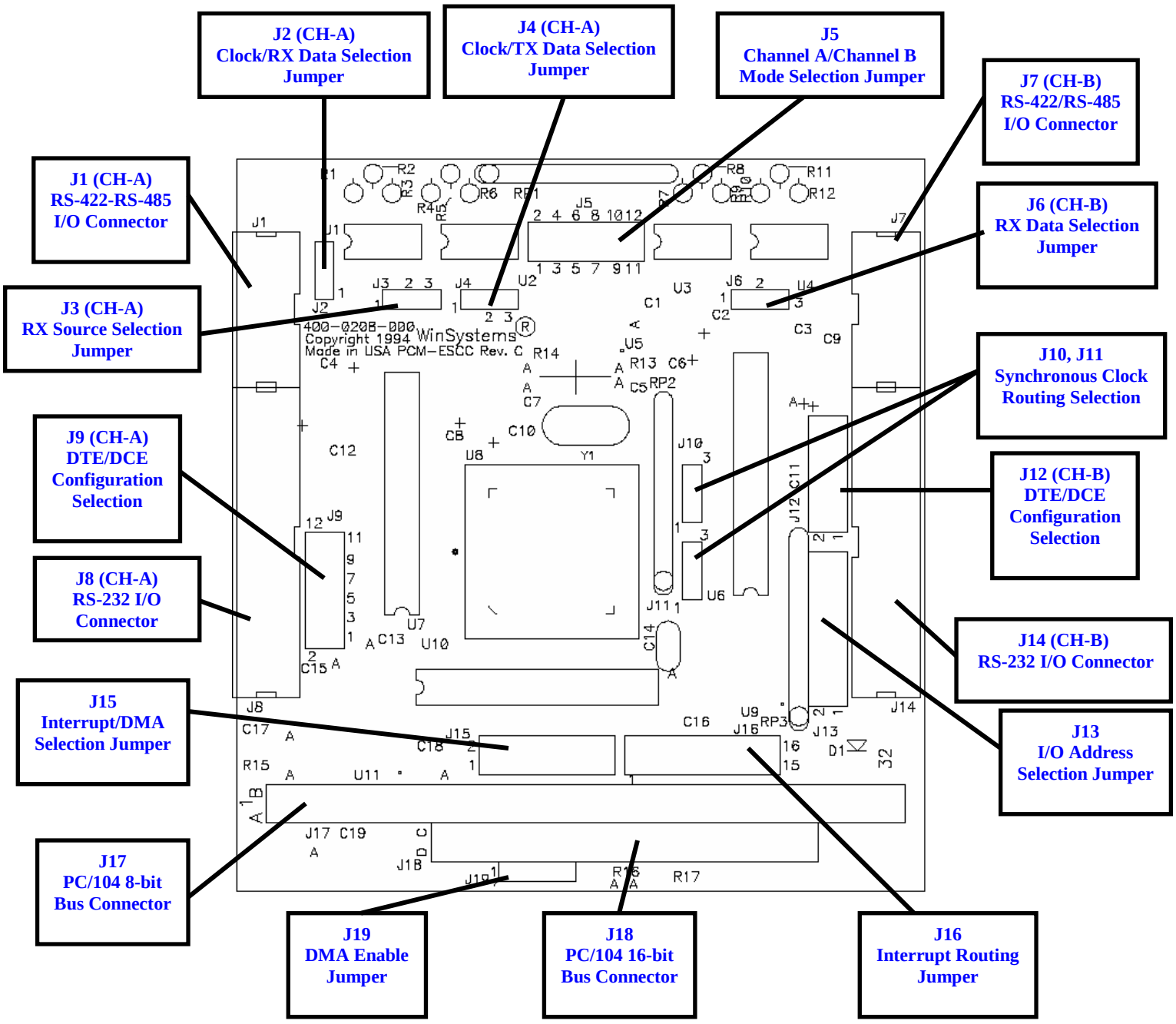
P/N 403-0208-000

ECO Number	Date Code	Revision
ORIGINATED	941202	B
95-08	950315	C
99-08	990412	C1

TABLE OF CONTENTS

Visual Index – Quick Reference

For the convenience of the user, a copy of the Visual Index has been provided with direct links to connector and jumper configuration data.



1 GENERAL INFORMATION

1.1 FEATURES

- Two independent, full-duplex serial channels
- Utilizes Zilog 85230 Enhanced Serial Communications Controller (ESCC)
- 4 byte transmit FIFO, 8 byte receive FIFO
- Asynchronous and synchronous protocols
- RS-232 Interface and RS422/RS485 interface with optional driver chip kit(s)
- RS-232 configurable as DTE or DCE
- Jumper Selectable Interrupt routing
- +5 Volt only operation
- Supports DMA transfers for Transmit and/or Receive Data

1.2 GENERAL DESCRIPTION

The PCM-ESCC is a PC/104 dual channel, multi-protocol data communications controller based upon the Zilog 85230 ESCC. The module can be configured to satisfy a wide variety of serial communications application needs.

Each channel is independent and capable of synchronous or asynchronous data communications with either RS-232 or optional RS-422/RS-485 electrical levels. In synchronous mode, the ESCC can support BISYNC, SDLC, and HDLC including CRC generation, sync character insertion/deletion and many other protocol dependent features. Each channel is configurable as Data Terminal Equipment (DTE) or Data Communications Equipment (DCE).

The onboard 85230 in addition to it's asynchronous and synchronous protocol capabilities also sports a 4 byte transmit FIFO and an 8 byte receive FIFO both of which have programmable interrupt or DMA request levels.

1.3 SPECIFICATIONS

1.3.1 Electrical

Bus Interface : PC/104 8-Bit
Optional 16-Bit connector allows access to higher number interrupts.

VCC : +5V +/-5% @ 140 mA.

I/O Addressing : Uses 4 consecutive I/O addresses, the base of which is jumper selectable from 000H to 3FFH.

1.3.2 Mechanical

Dimensions : 3.6 X 3.8 X 0.6 inches

PC Board : FR4 Epoxy Glass, with 2 signal layers and 2 power planes with screened component legend and plated through holes.

Connectors : 26 Pin 0.10" grid RN type IDH-26-LP for async/sync I/O

10 Pin 0.10" grid RN type IDH-10-LP for RS-422/RS- 485

Jumpers : 0.025" square posts on 0.10" centers

1.3.3 Environmental

Operating Temperature : -40° to 85° C

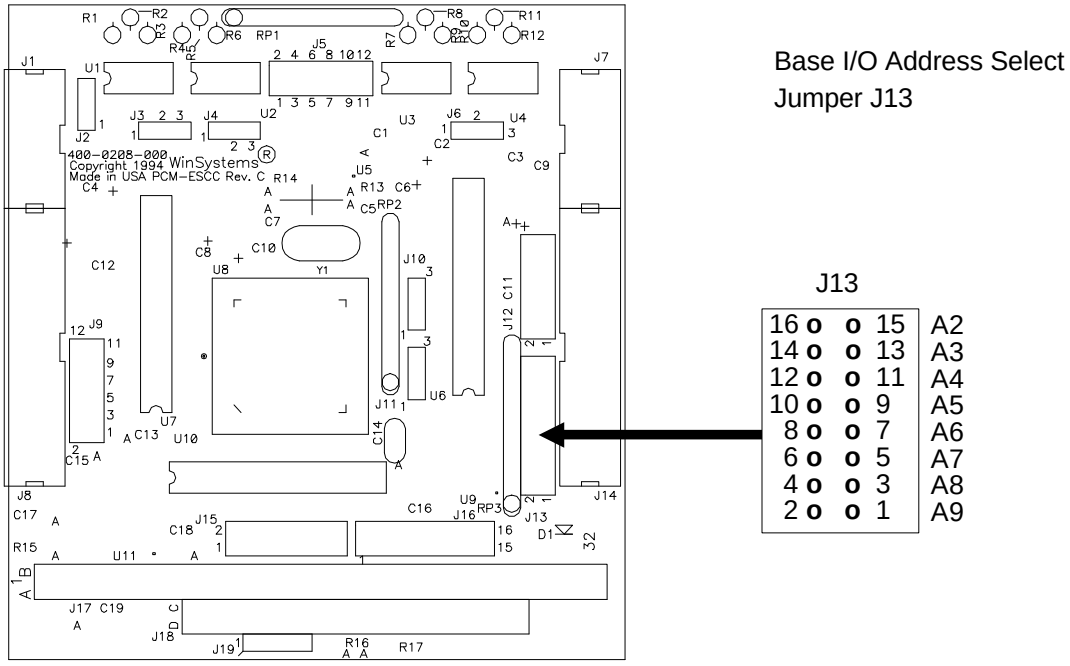
Non-Condensing relative humidity : 5% to 95%

2 PCM-ESCC Technical Reference

2.1 Introduction

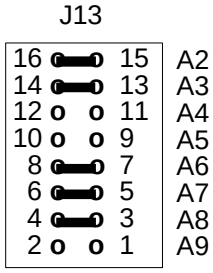
This section of the manual is intended to provide the necessary information for the configuration of the PCM-ESCC module to the desired mode of operation. The PCM-ESCC utilizes the very versatile but somewhat complex Zilog 85230 ESCC. The full text of the Zilog SCC user's manual pertaining to the 85230 is reprinted in Appendix C and should be referred to for register and programming details. WinSystems maintains a technical support group to assist in the configuration and usage of this product. Questions not adequately covered in this manual can be addressed to the technical support department at (817) 274-7553 between the hours of 8AM and 5PM Central Time. Alternately assistance can be requested via FAX at (817) 548-1358.

2.2 I/O Address Selection



The PCM-ESCC uses 4 consecutive I/O addresses beginning at the address specified by the jumpering of J13. A jumper present matches a '0' in the address where a jumper absent matches a '1' in the address. A sample jumpering for I/O address 230H is shown on the following page.

Sample I/O Select
for 230H



2.3 I/O Address assignment

The ESCC uses 4 consecutive addresses which are defined below. The BASE address is set via J13 as defined earlier. Refer to the SCC user's manual reprint in Appendix D for details regarding register and programming values.

BASE + 0 = Channel A Data Port

BASE + 1 = Channel A Command Port

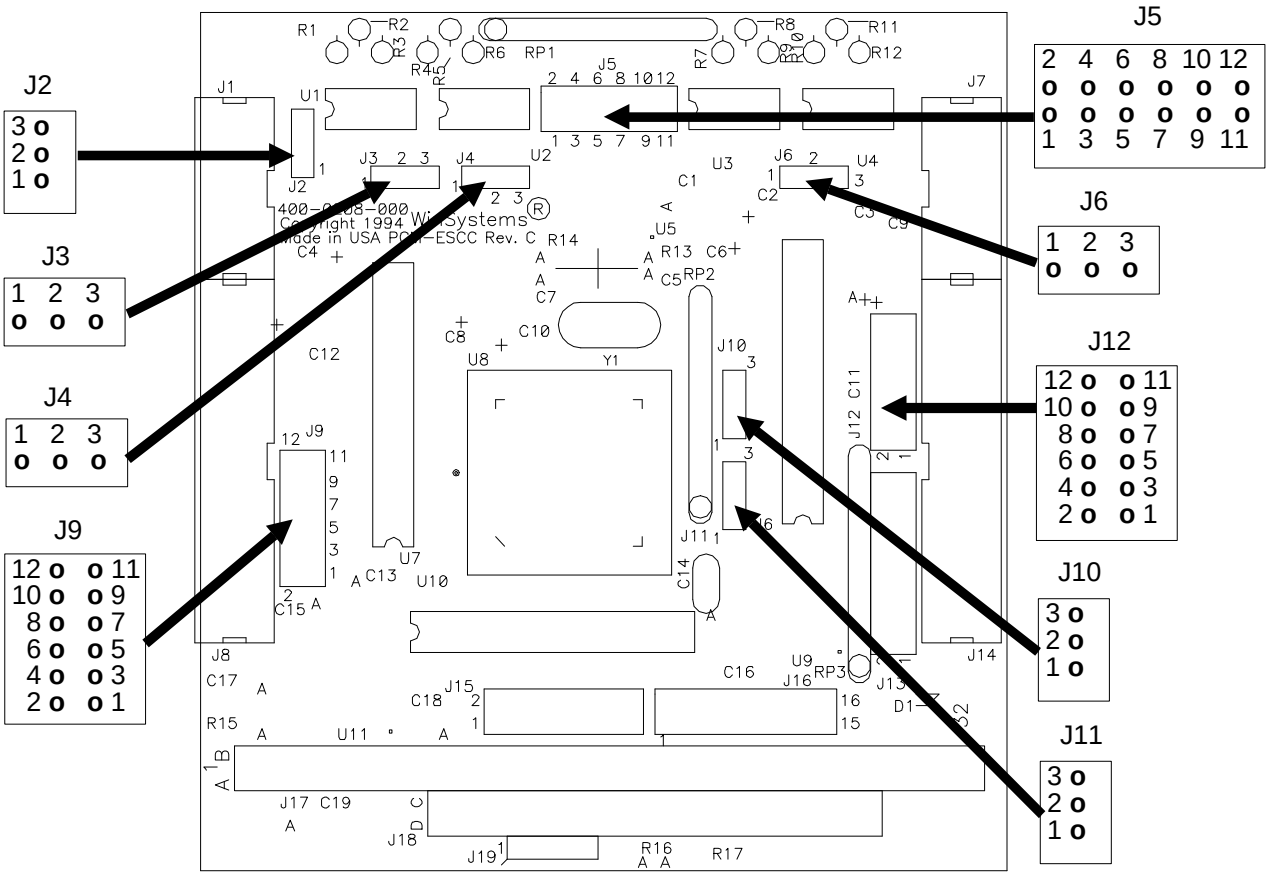
BASE + 2 = Channel B Data Port

BASE + 3 = Channel B Command Port

2.4 Serial Mode Selection

The extreme versatility of the PCM-ESCC and the 85230 presents an overwhelming challenge in attempting to document all of the possible modes and protocols. In an attempt to simplify the task the following pages will document the proper jumpering for the 9 most commonly used configurations of RS-232, RS-422 and RS-485. Reference to the PCM-ESCC schematic diagrams in Appendix D can be very helpful in understanding the usage and possible combinations for the serial configuration jumpers.

Mode Number	Channel A	Channel B
1	RS-232	RS-232
2	RS-232	RS-422
3	RS-232	RS-485
4	RS-422	RS-232
5	RS-422	RS-422
6	RS-422	RS-485
7	RS-485	RS-232
8	RS-485	RS-422
9	RS-485	RS-485



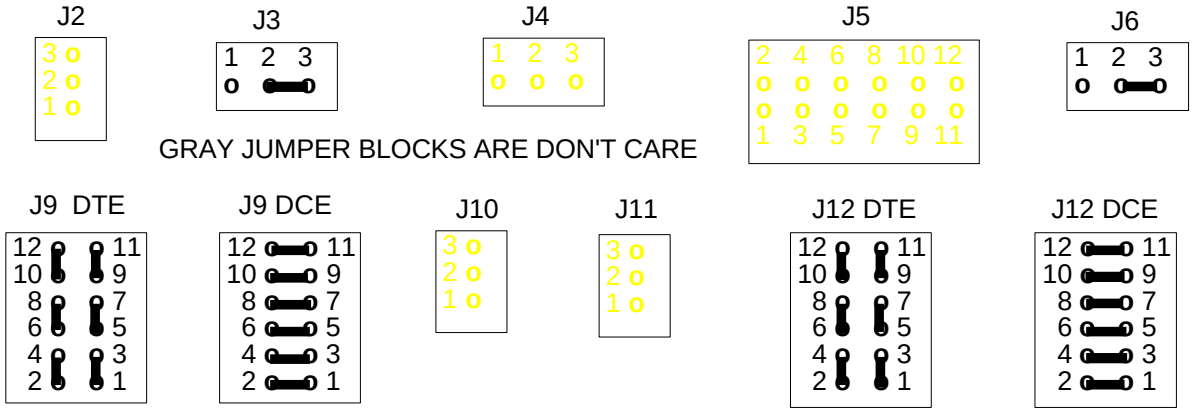
SERIAL CONFIGURATION JUMPERS

Choose a mode number that most closely matches the desired usage and jumper according to that section. Variations for synchronous support or DMA use will be addressed in a later section.

2.4.1 Mode 1

Channel A RS232, Channel B RS232

In this mode both channels are used with RS-232 Line levels. Each channel can also be configured as a DTE or DCE device. The jumpering for this mode is shown below. The Winsystems cable assembly CBL-101-3 will terminate a channel in a male DB-25 connector and the CBL-102-3 will terminate a channel in a female DB-25 connector.



CH A J8

GND	1	14	N/C
*TX_DATA (RX_DATA)	2	15	TRANSMIT CLOCK**
*RX_DATA (TX_DATA)	3	16	N/C
*RTS (CTS)	4	17	RECEIVER CLOCK*
*CTS (RTS)	5	18	N/C
*DSR*** (DTR)	6	19	N/C
GND	7	20	*DTR (***DSR)
Carrier Detect	8	21	N/C
N/C	9	22	N/C
N/C	10	23	N/C
N/C	11	24	TRANSMIT CLOCK**
N/C	12	25	N/C
N/C	13	26	N/C

*First Signal shown is for DTE configuration. Label in parenthesis is the DCE signal name.

** These are optional signals typically used for synchronous protocols only. Refer to Later section for clock routing.

*** There is no DSR input to the 85230. The DSR input pin is routed to the Carrier detect Pin on the 85230 meaning that assertion on either DSR or Carrier detect will result in a carrier detect presence at the 85230. If this is not desired remove the J9 jumper that attaches to pin 10 on J9

CH B J14

GND	1	14	N/C
*TX_DATA (RX_DATA)	2	15	N/C
*RX_DATA (TX_DATA)	3	16	N/C
*RTS (CTS)	4	17	RECEIVER CLOCK*
*CTS (RTS)	5	18	N/C
*DSR*** (DTR)	6	19	N/C
GND	7	20	*DTR (***DSR)
Carrier Detect	8	21	N/C
N/C	9	22	N/C
N/C	10	23	N/C
N/C	11	24	TRANSMIT CLOCK**
N/C	12	25	N/C
N/C	13	26	N/C

*First Signal shown is for DTE configuration. Label in parenthesis is the DCE signal name.

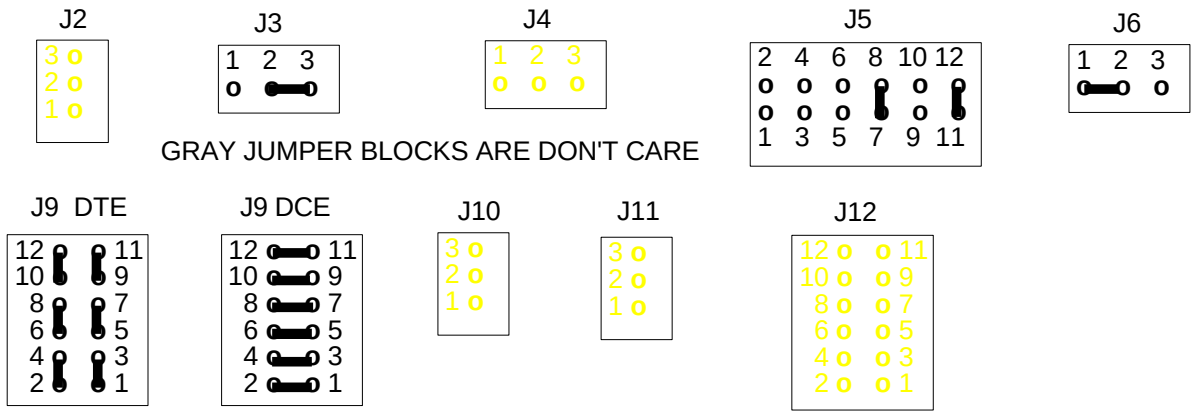
** These are optional signals typically used for synchronous protocols only. Refer to Later section for clock routing.

*** There is no DSR input to the 85230. The DSR input pin is routed to the Carrier detect Pin on the 85230 meaning that assertion on either DSR or Carrier detect will result in a carrier detect presence at the 85230. If this is not desired remove the J12 jumper that attaches to pin 3 on J12

2.4.2 Mode 2

Channel A RS-232, Channel B RS-422

In mode 2 channel A is configured for RS-232 and is terminated at J8. Channel B is configured as 4-wire RS-422 and is terminated at the 10-pin connector J7. The jumpering for this mode is shown below.



CH A J8

GND	1 o	o 14	N/C
*TX_DATA (RX_DATA)	2 o	o 15	TRANSMIT CLOCK**
*RX_DATA (TX_DATA)	3 o	o 16	N/C
*RTS (CTS)	4 o	o 17	RECEIVER CLOCK*
*CTS (RTS)	5 o	o 18	N/C
*DSR*** (DTR)	6 o	o 19	N/C
GND	7 o	o 20	*DTR (***DSR)
Carrier Detect	8 o	o 21	N/C
N/C	9 o	o 22	N/C
N/C	10 o	o 23	N/C
N/C	11 o	o 24	TRANSMIT CLOCK**
N/C	12 o	o 25	N/C
N/C	13 o	o 26	N/C

*First Signal shown is for DTE configuration. Label in parenthesis is the DCE signal name.

** These are optional signals typically used for synchronous protocols only. Refer to Later section for clock routing.

*** There is no DSR input to the 85230. The DSR input pin is routed to the Carrier detect Pin on the 85230 meaning that assertion on either DSR or Carrier detect will result in a carrier detect presence at the 85230. If this is not desired remove the J9 jumper that attaches to pin 10 on J9

CH B J7

N/C	1 o	o 6	RX+
TX+	2 o	o 7	RX-
TX-	3 o	o 8	N/C
N/C	4 o	o 9	N/C
GND	5 o	o 10	+5V

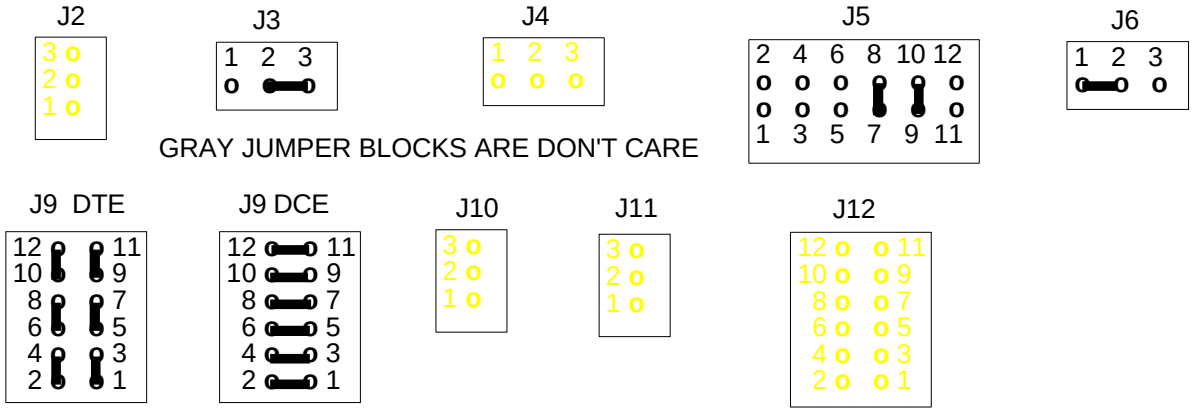
Requires the installation of 75176 driver ICs in locations U3 and U4

The RTS line must be asserted in order to enable the transmitter. User installable termination resistor locations are present on the board at R7 through R12. Refer to the schematic diagrams for specific resistor locations. +5V and ground are also available on the I/O connector in order to allow termination of the cable itself.

2.4.3 Mode 3

Channel A RS-232, Channel B RS-485

Mode 3 sets the A channel as conventional RS-232 in either a DTE or DCE configuration terminated at J8. Channel B is configured for RS-485 multi-drop terminated at J7 The RTS line on channel B controls the transmit/receive function.



CH A J8

GND	1 o o 14	N/C
*TX_DATA (RX_DATA)	2 o o 15	TRANSMIT CLOCK**
*RX_DATA (TX_DATA)	3 o o 16	N/C
*RTS (CTS)	4 o o 17	RECEIVER CLOCK*
*CTS (RTS)	5 o o 18	N/C
*DSR*** (DTR)	6 o o 19	N/C
GND	7 o o 20	*DTR (***DSR)
Carrier Detect	8 o o 21	N/C
N/C	9 o o 22	N/C
N/C	10 o o 23	N/C
N/C	11 o o 24	TRANSMIT CLOCK**
N/C	12 o o 25	N/C
N/C	13 o o 26	N/C

*First Signal shown is for DTE configuration. Label in parenthesis is the DCE signal name.

** These are optional signals typically used for synchronous protocols only. Refer to Later section for clock routing.

*** There is no DSR input to the 85230. The DSR input pin is routed to the Carrier detect Pin on the 85230 meaning that assertion on either DSR or Carrier detect will result in a carrier detect presence at the 85230. If this is not desired remove the J9 jumper that attaches to pin 10 on J9

CH B J7

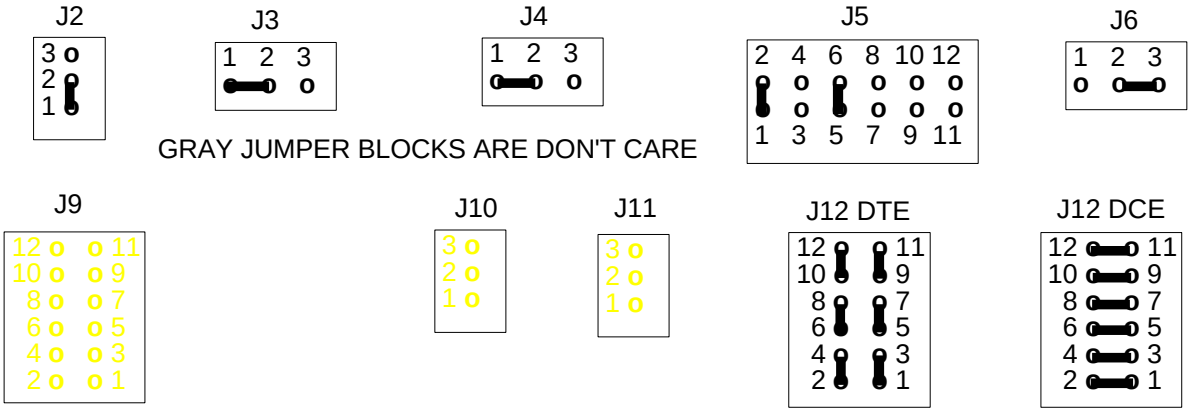
N/C	1 o o 6	N/C
TX/RX+	2 o o 7	N/C
TX/RX-	3 o o 8	N/C
N/C	4 o o 9	N/C
GND	5 o o 10	+5V

Requires installation of 75176 driver IC in location U4.

The RTS line must be asserted for transmit and disasserted for receive. Resistor locations R10 through R12 are provided on the board for user installable termination resistors. +5V and ground are also available on the I/O connector

2.4.4 Mode 4 Channel A RS-422, Channel B RS-232

Mode number 4 sets up channel A as RS-422 at J1 and Channel B as RS-232 at J14.



CH A J1

N/C	1 o	o 6	RX+
TX+	2 o	o 7	RX-
TX-	3 o	o 8	N/C
N/C	4 o	o 9	N/C
GND	5 o	o 10	+5V

Requires installation of 75176 driver ICs in locations U1 and U2.

The RTS line must be asserted in order to enable the transmitter. User installable termination resistor locations are present on the board at R1 through R6. Refer to the schematic diagrams for specific resistor locations. +5V and ground are also available on the I/O connector in order to allow termination of the cable itself.

CH B J14

GND	1 o	o 14	N/C
*TX_DATA (RX_DATA)	2 o	o 15	N/C
*RX_DATA (TX_DATA)	3 o	o 16	N/C
*RTS (CTS)	4 o	o 17	RECEIVER CLOCK*
*CTS (RTS)	5 o	o 18	N/C
*DSR*** (DTR)	6 o	o 19	N/C
GND	7 o	o 20	*DTR (***DSR)
Carrier Detect	8 o	o 21	N/C
N/C	9 o	o 22	N/C
N/C	10 o	o 23	N/C
N/C	11 o	o 24	TRANSMIT CLOCK**
N/C	12 o	o 25	N/C
N/C	13 o	o 26	N/C

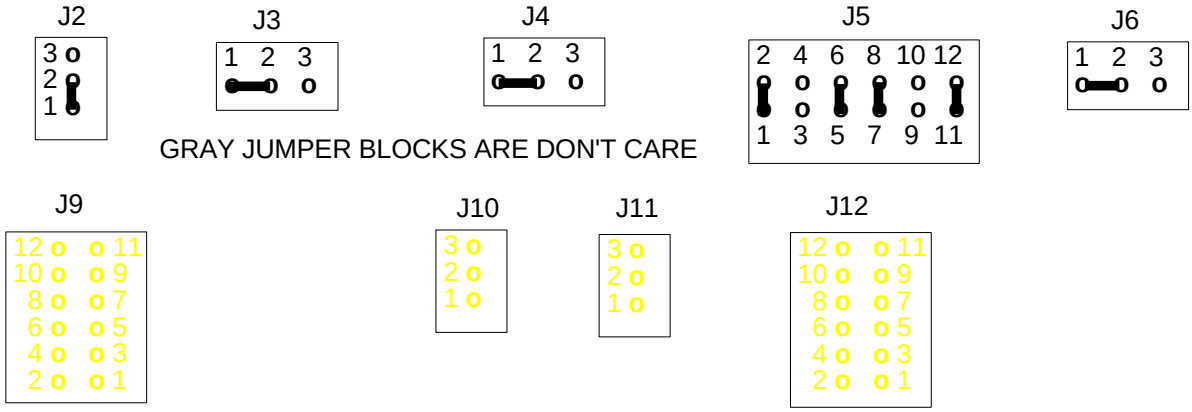
*First Signal shown is for DTE configuration. Label in parenthesis is the DCE signal name.

** These are optional signals typically used for synchronous protocols only. Refer to Later section for clock routing.

*** There is no DSR input to the 85230. The DSR input pin is routed to the Carrier detect Pin on the 85230 meaning that assertion on either DSR or Carrier detect will result in a carrier detect presence at the 85230. If this is not desired remove the J12 jumper that attaches to pin 3 on J12

2.4.5 Mode 5 Channel A RS-422, Channel B RS-422

This mode sets both the A channel at J1 and the B channel at J7 to RS-422.



CH A J1

N/C	1 o o 6	RX+
TX+	2 o o 7	RX-
TX-	3 o o 8	N/C
N/C	4 o o 9	N/C
GND	5 o o 10	+5V

Requires installation of 75176 driver ICs in locations U1 and U2.

The RTS line must be asserted in order to enable the transmitter. User installable termination resistor locations are present on the board at R1 through R6. Refer to the schematic diagrams for specific resistor locations. +5V and ground are also available on the I/O connector in order to allow termination of the cable itself.

CH B J7

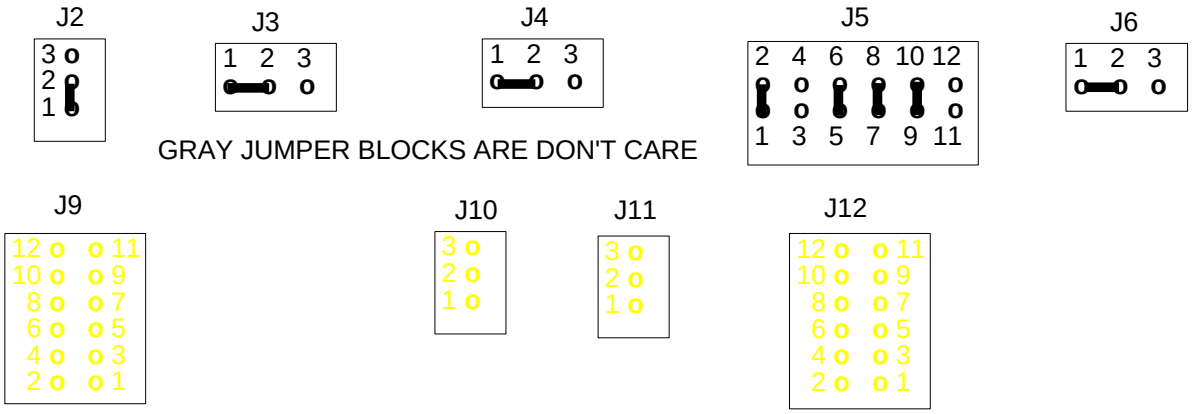
N/C	1 o o 6	RX+
TX+	2 o o 7	RX-
TX-	3 o o 8	N/C
N/C	4 o o 9	N/C
GND	5 o o 10	+5V

Requires the installation of 75176 driver ICs in locations U3 and U4.

The RTS line must be asserted in order to enable the transmitter. User installable termination resistor locations are present on the board at R7 through R12. Refer to the schematic diagrams for specific resistor locations. +5V and ground are also available on the I/O connector in order to allow termination of the cable itself.

2.4.6 Mode 6 Channel A RS-422, Channel B RS-485

Mode 6 sets channel A as RS-422 terminated at J1 and sets Channel B as RS-485 terminated at J7.



CH A J1

N/C	1 o o 6	RX+
TX+	2 o o 7	RX-
TX-	3 o o 8	N/C
N/C	4 o o 9	N/C
GND	5 o o 10	+5V

Requires installation of 75176 driver ICs in locations U1 and U2.

The RTS line must be asserted in order to enable the transmitter. User installable termination resistor locations are present on the board at R1 through R6. Refer to the schematic diagrams for specific resistor locations. +5V and ground are also available on the I/O connector in order to allow termination of the cable itself.

CH B J7

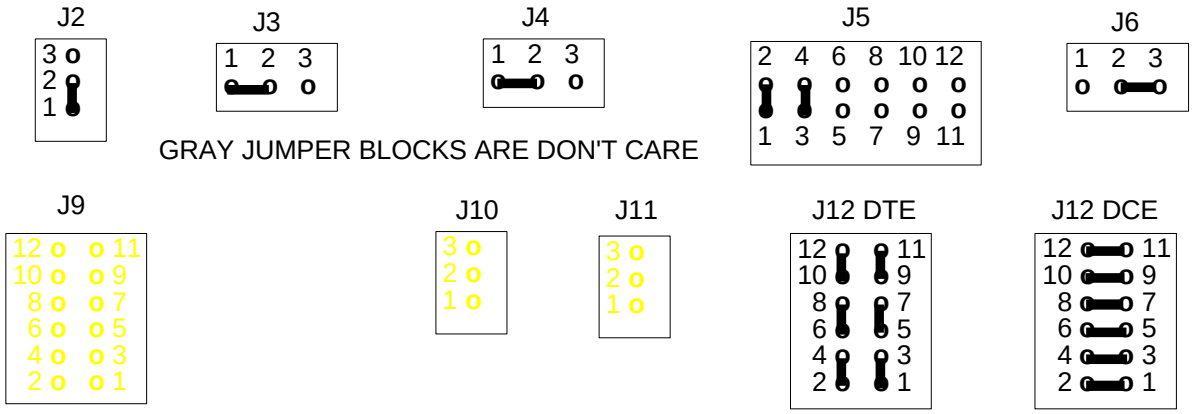
N/C	1 o o 6	N/C
TX/RX+	2 o o 7	N/C
TX/RX-	3 o o 8	N/C
N/C	4 o o 9	N/C
GND	5 o o 10	+5V

Requires the installation of 75176 driver IC in location U4.

The RTS line must be asserted for transmit and disasserted for receive. Resistor locations R10 through R12 are provided on the board for user installable termination resistors. +5V and ground are also available on the I/O connector to allow termination of the cable itself.

2.4.7 Mode 7 Channel A RS-485, Channel B RS-232

Mode number 7 sets channel A as RS-485 terminated at J1. Channel B is configured for either DTE or DCE and is terminated at J14.



CH A J1

N/C	1	6	N/C
TX/RX+	2	7	N/C
TX/RX-	3	8	N/C
N/C	4	9	N/C
GND	5	10	+5V

Requires the installation of 75176 driver IC in location U2.

The RTS line must be asserted for transmit and disasserted for receive. Resistor locations R4 through R6 are provided on the board for user installable termination resistors. +5V and ground are also available on the I/O connector to allow termination of the cable itself.

CH B J14

GND	1	14	N/C
*TX_DATA (RX_DATA)	2	15	N/C
*RX_DATA (TX_DATA)	3	16	N/C
*RTS (CTS)	4	17	RECEIVER CLOCK*
*CTS (RTS)	5	18	N/C
*DSR*** (DTR)	6	19	N/C
GND	7	20	*DTR (***DSR)
Carrier Detect	8	21	N/C
N/C	9	22	N/C
N/C	10	23	N/C
N/C	11	24	TRANSMIT CLOCK**
N/C	12	25	N/C
N/C	13	26	N/C

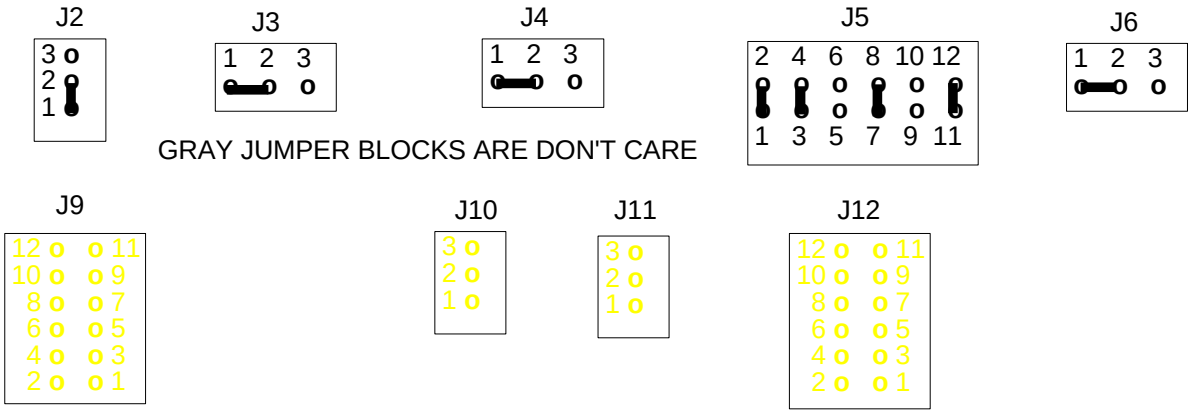
*First Signal shown is for DTE configuration. Label in parenthesis is the DCE signal name.

** These are optional signals typically used for synchronous protocols only. Refer to Later section for clock routing.

*** There is no DSR input to the 85230. The DSR input pin is routed to the Carrier detect Pin on the 85230 meaning that assertion on either DSR or Carrier detect will result in a carrier detect presence at the 85230. If this is not desired remove the J12 jumper that attaches to pin 3 on J12

2.4.8 Mode 8 Channel A RS-485, Channel B RS-422

Mode 8 sets Channel A to terminate at J1 for RS-485, it also sets channel B for RS-422 terminated at J7.



CH A J1

N/C	1 o o 6	N/C
TX/RX+	2 o o 7	N/C
TX/RX-	3 o o 8	N/C
N/C	4 o o 9	N/C
GND	5 o o 10	+5V

Requires installation of 75176 driver IC in location U2.

The RTS line must be asserted for transmit and disasserted for receive. Resistor locations R4 through R6 are provided on the board for user installable termination resistors. +5V and ground are also available on the I/O connector to allow termination of the cable itself.

CH B J7

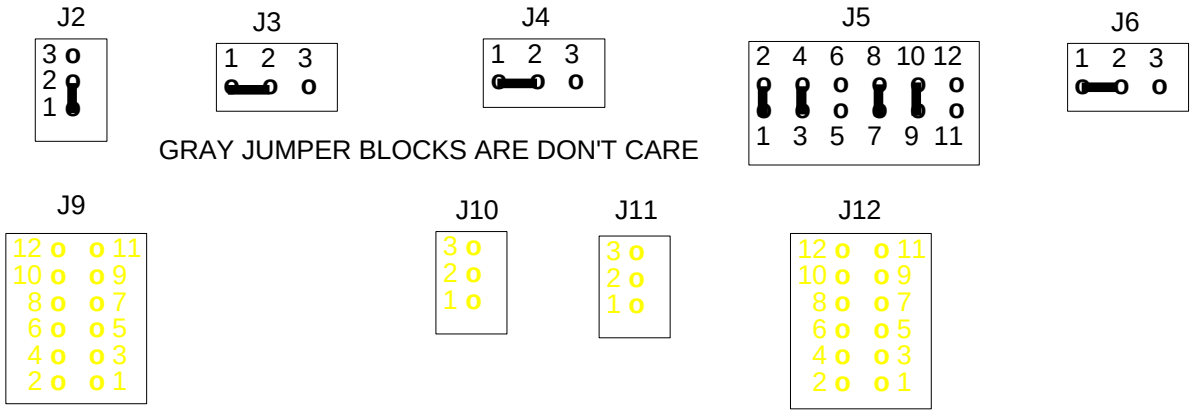
N/C	1 o o 6	RX+
TX+	2 o o 7	RX-
TX-	3 o o 8	N/C
N/C	4 o o 9	N/C
GND	5 o o 10	+5V

Requires installation of 75176 driver ICs in locations U3 and U4.

The RTS line must be asserted in order to enable the transmitter. User installable termination resistor locations are present on the board at R7 through R12. Refer to the schematic diagrams for specific resistor locations. +5V and ground are also available on the I/O connector in order to allow termination of the cable itself.

2.4.9 Mode 9 Channel A RS-485, Channel B RS-485

In mode 9 both channels A and B are set for RS-485 and terminated at J1 and J7 respectively.



CH A J1

N/C	1 o o 6	N/C
TX/RX+	2 o o 7	N/C
TX/RX-	3 o o 8	N/C
N/C	4 o o 9	N/C
GND	5 o o 10	+5V

Requires installation of 75176 driver IC in location U2.

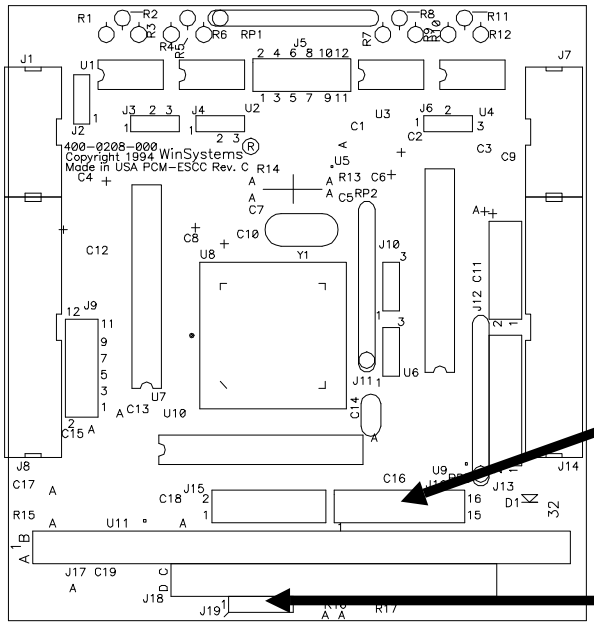
The RTS line must be asserted for transmit and disasserted for receive. Resistor locations R4 through R6 are provided on the board for user installable termination resistors. +5V and ground are also available on the I/O connector to allow termination of the cable itself.

CH B J7

N/C	1 o o 6	N/C
TX/RX+	2 o o 7	N/C
TX/RX-	3 o o 8	N/C
N/C	4 o o 9	N/C
GND	5 o o 10	+5V

Requires installation of 75176 driver IC in location U4.

The RTS line must be asserted for transmit and disasserted for receive. Resistor locations R10 through R12 are provided on the board for user installable termination resistors. +5V and ground are also available on the I/O connector to allow termination of the cable itself.



DMA Configuration jumpers J19 and J16.

J16

2	4	6	8	10	12	14	16
o	o	o	o	o	o	o	o
o	o	o	o	o	o	o	o
1	3	5	7	9	11	13	15

J19

1	2	3	4
o	o	o	o

2.5 DMA Configuration

The PCM-ESCC and the Zilog 85230 can be configured for DMA data transfers using DMA channels 1 and 3 on the PC/104 bus. The jumper block at J19 and the top two pins of J16 are used to configure the DMA channel routing. Refer to the reprint of the ESCC user's manual for programming details. The supported DMA options are shown below.

J16

2	4	6	8	10	12	14	16
▮	▮	o	o	o	o	o	o
		o	o	o	o	o	o
1	3	5	7	9	11	13	15

J19

1	2	3	4
o	o	o	o

DMA DISABLED

J16

2	4	6	8	10	12	14	16
o	▮	o	o	o	o	o	o
o		o	o	o	o	o	o
1	3	5	7	9	11	13	15

J19

1	2	3	4
▬		▬	

Channel A RX DMA - DRQ1
Channel A TX DMA - DRQ3

J16

2	4	6	8	10	12	14	16
▮	o	o	o	o	o	o	o
	o	o	o	o	o	o	o
1	3	5	7	9	11	13	15

J19

1	2	3	4
	▬		▬

Channel B RX DMA - DRQ1
Channel B TX DMA - DRQ3

J16

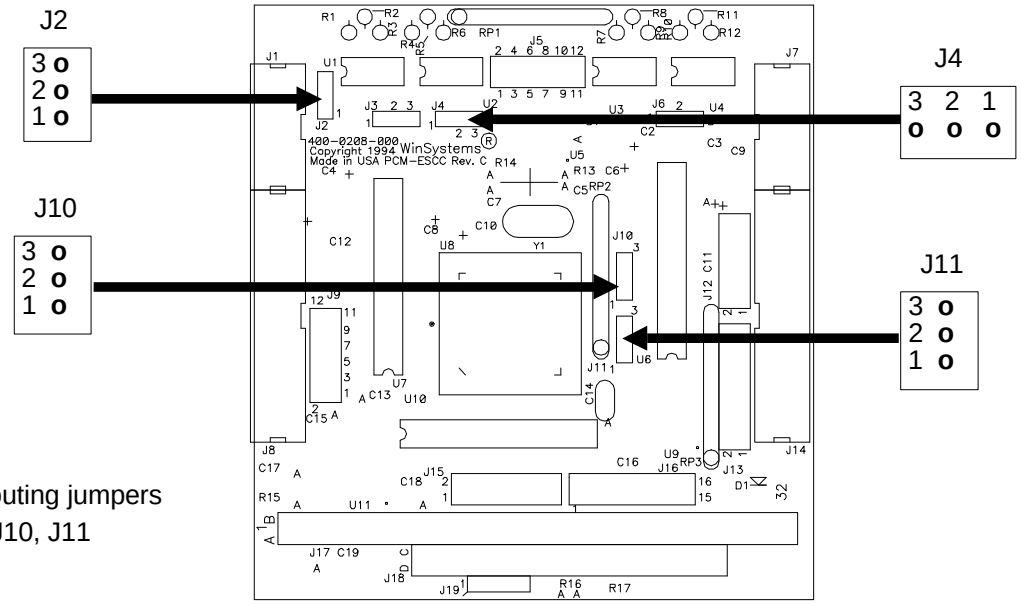
2	4	6	8	10	12	14	16
o	o	o	o	o	o	o	o
o	o	o	o	o	o	o	o
1	3	5	7	9	11	13	15

J19

1	2	3	4
▬		▬	

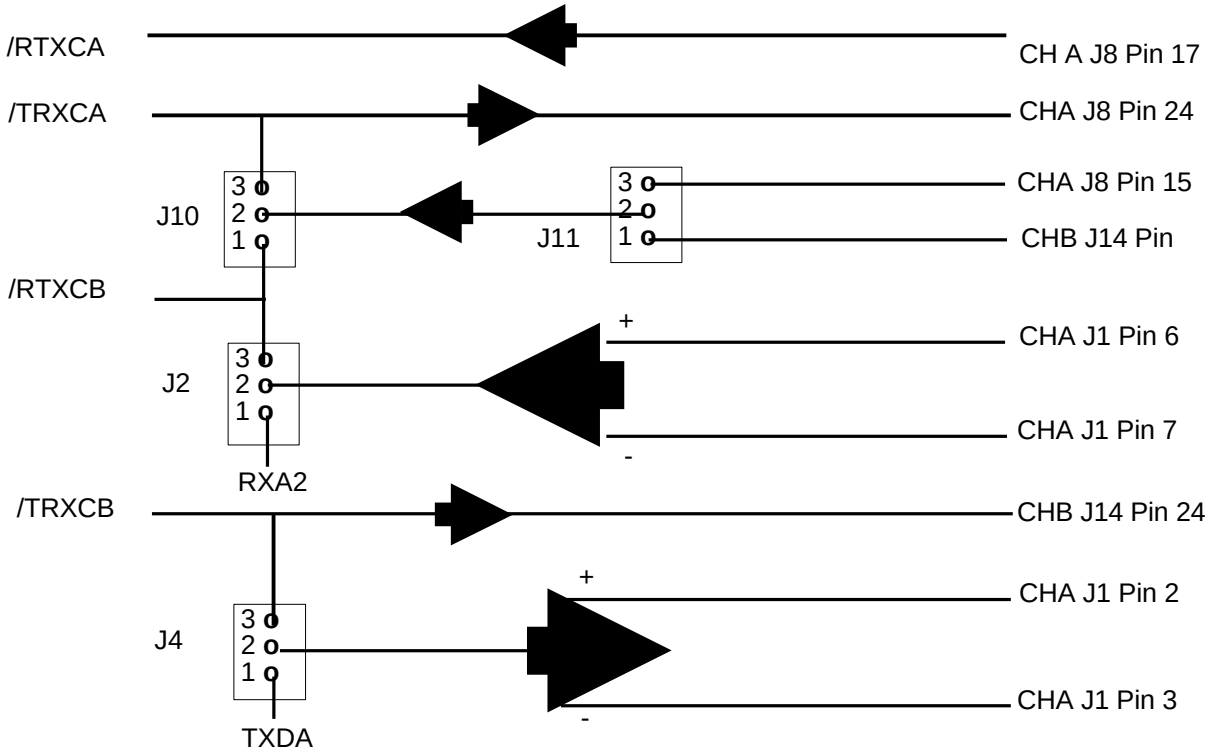
Channel A TX/RX DMA - DRQ1
Channel B TX/RX DMA - DRQ3

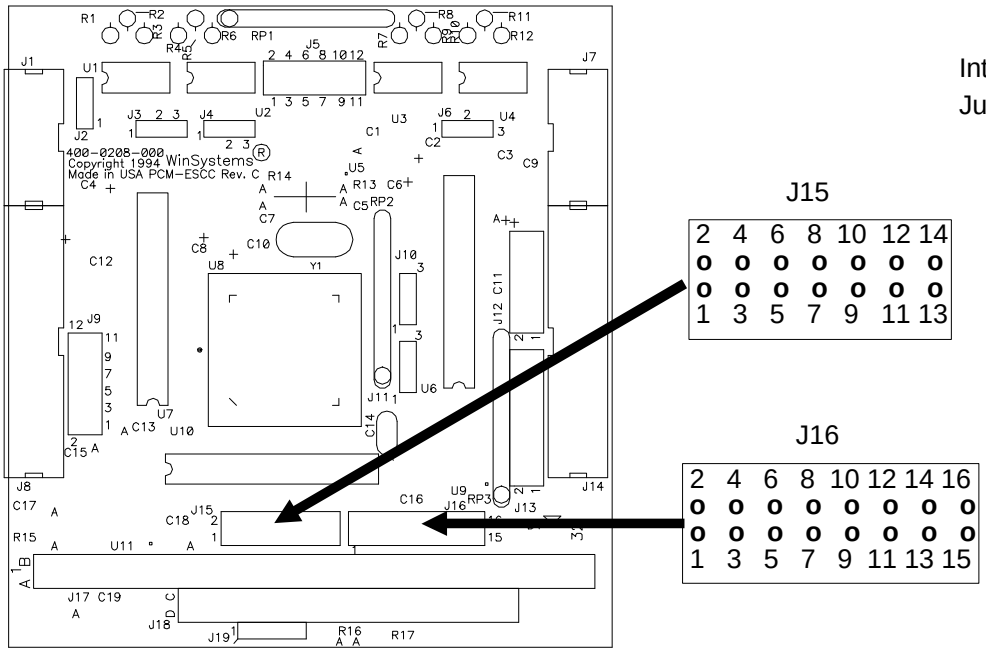
2.6 Synchronous Mode Options



Clock routing jumpers
J2, J4, J10, J11

When programmed for synchronous modes it is often necessary to provide or recognize the Transmit/Receive Clock(s) from/to the I/O device. There are several routing jumpers available to provide maximum flexibility in clock routing. The clock routing jumpers are shown below.





2.7 Interrupt Routing

The 85230 interrupt can be routed to any free PC/104 Bus interrupt using J16. If the optional PCM-ESCC-16 board is used there are additional interrupt choices available by selecting via J15. J15 also provides support for interrupt sharing. The diagrams below detail the interrupt routing and sharing jumpers.

J16

	1 o o	2
	3 o o	4
IRQ7	5 o o	6
IRQ6	7 o o	8
IRQ5	9 o o	10
IRQ4	11 o o	12
IRQ3	13 o o	14
IRQ2	15 o o	16

J15

IRQ10	1 o o	2
IRQ11	3 o o	4
IRQ12	5 o o	6
IRQ15	7 o o	8
IRQ14	9 o o	10
	11 o o	12
	13 o o	14

The PCM-ESCC is also capable of sharing a bus interrupt with another PCM-ESCC module or another PC/104 module supporting interrupt sharing. Either the base CPU board or one of the modules sharing the interrupt must terminate the interrupt with a pulldown resistor. WinSystems CPU boards do NOT provide this pulldown so it must be enabled at the PC/104 module. To enable interrupt sharing remove the factory installed jumper at J15 pins 13-14 and place it on J15 pins 11-12. For non-shared interrupts a jumper should always be in place at J15 pins 13-14. The pulldown resistor is connected by jumpering J15 pins 11-12.

2.8 PC/104 Bus Connectors

The 8-bit PC/104 connector J17 and the 16-Bit PC/104 connector J18 are both shown here:

J17

IOCHK	A1	B1		GND
SD7	A2	B2		RESET
SD6	A3	B3		+5V
SD5	A4	B4		IRQ2
SD4	A5	B5		-5V
SD3	A6	B6		DRQ2
SD2	A7	B7		-12V
SD1	A8	B8		0WS
SD0	A9	B9		+12V
IOCHRDY	A10	B10		GND
AEN	A11	B11		SMEMW
SA19	A12	B12		SMEMR
SA18	A13	B13		IOW
SA17	A14	B14		IOR
SA16	A15	B15		DACK3
SA15	A16	B16		DRQ3
SA14	A17	B17		DACK1
SA13	A18	B18		DRQ1
SA12	A19	B19		DACK0
SA11	A20	B20		CLK
SA10	A21	B21		IRQ7
SA9	A22	B22		IRQ6
SA8	A23	B23		IRQ5
SA7	A24	B24		IRQ4
SA6	A25	B25		IRQ3
SA5	A26	B26		DACK2
SA4	A27	B27		T/C
SA3	A28	B28		BALE
SA2	A29	B29		+5V
SA1	A30	B30		OSC
SA0	A31	B31		GND
GND	A32	B32		GND

J18

GND	D0	C0		GND
MEMCS16	D1	C1		SBHE
IOCS16	D2	C2		LA23
IRQ10	D3	C3		LA22
IRQ11	D4	C4		LA21
IRQ12	D5	C5		LA20
IRQ15	D6	C6		LA19
IRQ14	D7	C7		LA18
DACK0	D8	C8		LA17
DRQ0	D9	C9		MEMR
DACK5	D10	C10		MEMW
DRQ5	D11	C11		SD8
DACK6	D12	C12		SD9
DRQ6	D13	C13		SD10
DACK7	D14	C14		SD11
DRQ7	D15	C15		SD12
+5V	D16	C16		SD13
MASTER	D17	C17		SD14
GND	D18	C18		SD15
GND	D19	C19		KEY

2.9 Connector/Jumper Summary

Connector/ Jumper	Description	Page Reference
J1	CH A RS-422/RS-485 I/O connector	2-7
J2	CH A Clock/RX Data Select Jumper	2-3
J3	CH A RX source select jumper	2-3
J4	CH A Clock/TX Data Select Jumper	2-3
J5	CHA/CHB Mode Select Jumper	2-3
J6	CH B RX Data select jumper	2-3
J7	CH B RS-422/RS-485 I/O Connector	2-5
J8	CH A RS-232 I/O Connector	2-4
J9	CH A DTE/DCE configuration select	2-3
J10	Synchronous Clock routing select	2-3
J11	Synchronous Clock routing select	2-3
J12	CH B DTE/DCE configuration select	2-3
J13	I/O Address Select jumper	2-1
J14	CH B RS-232 I/O Connector	2-4
J15	Interrupt/DMA Select jumper	2-15
J16	Interrupt routing jumper	2-15
J17	PC/104 8-Bit bus connector	2-16
J18	PC/104 16-Bit bus connector	2-16
J19	DMA Enable jumper	2-13

APPENDIX A

Zilog's ESCC User's Manual Reprint	ESCC.ZIP

APPENDIX

Zilog ESCC User's Manual Reprint

Zilog's ESCC User's Manual	scc_escc_um.pdf
User Manual Errata	scc_up0026.pdf

Cable Drawings

Part Number	Description
CBL-101-3	26-pin ribbon to 25-pin male "D" connector adapter
CBL-102-3	25-pin ribbon to 25-pin female "D" connector adapter

Telephone: 817-274-7553 . . Fax: 817-548-1358
http://www.winsystems.com . . E-mail: info@winsystems.com

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2. Reason for the return.
3. Invoice number and date of purchase (if available), and original purchase order number.
4. Name, address, telephone and FAX number of the person making the request.
5. Do not debit WinSystems for the repair. WinSystems does not authorize debits.

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The customer must send the product freight prepaid and insured. The product must be enclosed in an anti-static bag to protect it from damage caused by static electricity. Each bag must be completely sealed. Packing material must separate each unit returned and placed as a cushion between the unit(s) and the sides and top of the shipping container. WinSystems is not responsible for any damage to the product due to inadequate packaging or static electricity.