OPERATIONS MANUAL
PCM-CTC

REVISION HISTORY

P/N 403-0198-000

ECO Number	Date Code	Rev Level
Originated	940217	B
99-52	990430	B1

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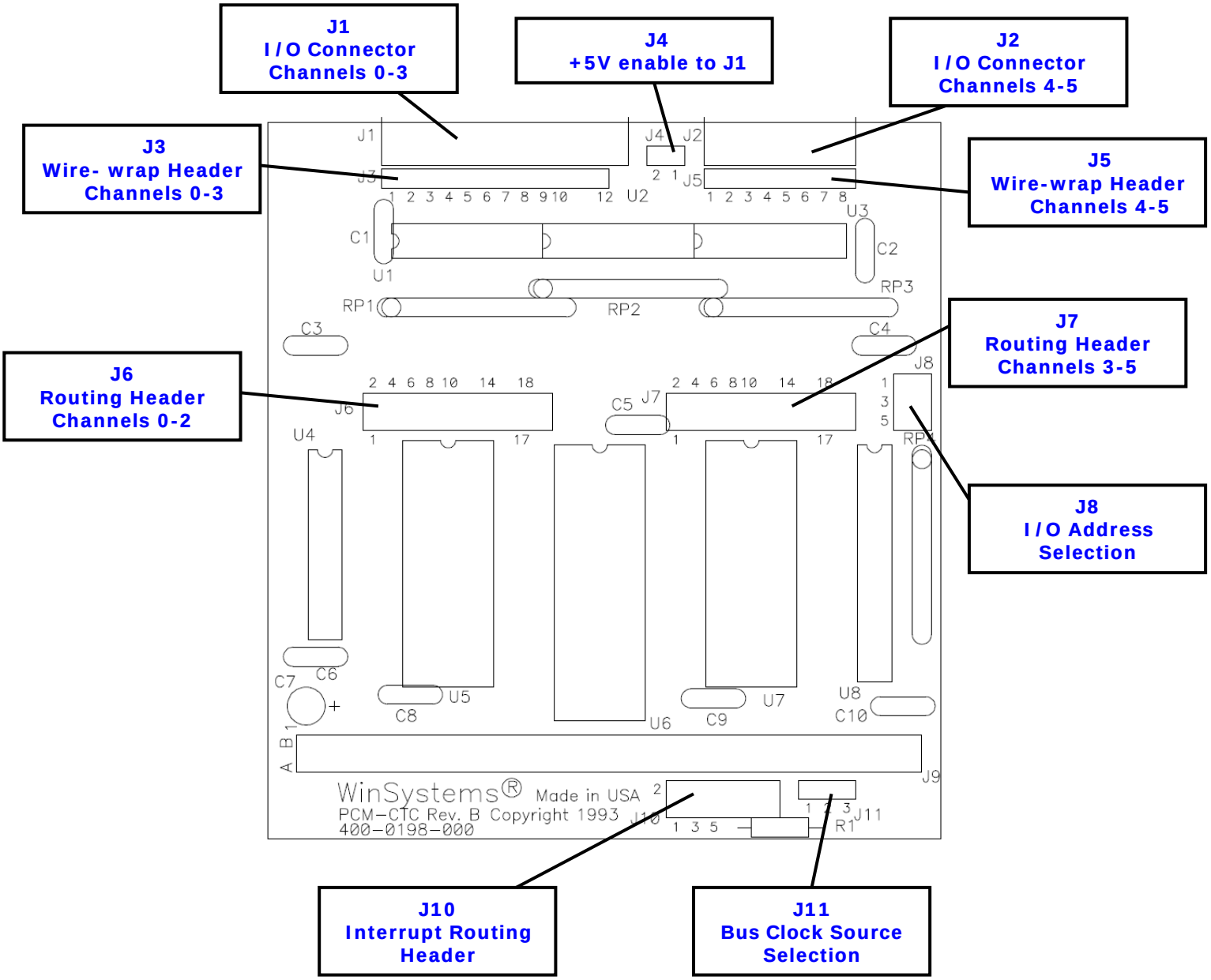
Visual Index – Quick Reference

For the convenience of the user, a copy of the Visual Index has been provided with direct links to connector and jumper configuration data.



1 GENERAL INFORMATION

1.1 FEATURES

- Six independent 16-Bit Counter/Timers
- Full input/output buffering for all Clock, Gate and output signals
- Jumper selectable daisy-chaining for cascading counts
- Utilizes industry standard 8254 timers
- Counts frequencies up to 8Mhz
- Onboard 8259 provides interrupt identification
- Auxiliary Interrupt inputs
- PC/104 stackthrough design
- Jumper selectable I/O address
- +5 Volt only operation
- Multiple internal or external clock selection

1.2 General Description

The PCM-CTC card is designed to solve the common timing problems in industrial systems design. Six independent 16-bit channels are capable of frequency/event counting from DC to 8MHz, pulse marker or square-wave generation, time interval measurements, and one-shot simulation. All six channels have a buffered clock, Gate and output available. Jumper selectable routing headers allow source selection and cascading to provide maximum flexibility.

1.3 SPECIFICATIONS

1.3.1 Electrical

Bus Interface : PC/104 8-Bit stackthrough

Power Requirements: +5V +/-5% at 40 mA typical

1.3.2 Mechanical

Dimensions : 3.6 X 3.8 X 0.6"

PC Board : FR4 Epoxy glass with 2 signal layers with screened component legend and plated through holes.

Jumpers : 0.025" square posts on 0.10" centers.

Connectors : J1 I/O - RN type IDH-26-LP
J2 I/O - RN type IDH-8-LP

1.3.3 Environmental

Operating Temperature : -40° to 85° C

Non-Condensing Humidity : 5% to 95%

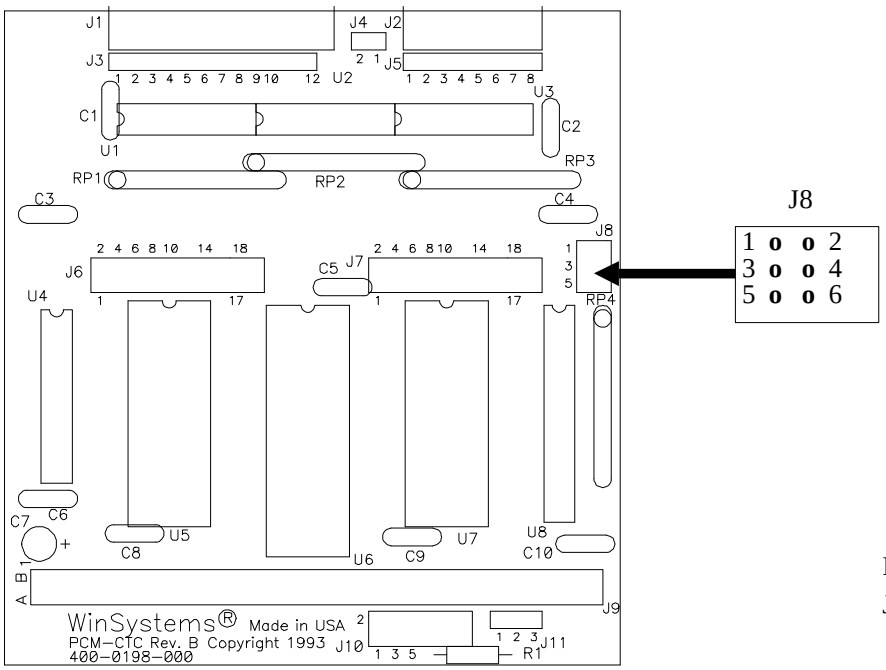
2 PCM-CTC Technical Reference

2.1 Introduction

This section of the manual is intended to provide sufficient information for the configuration, installation, and programming of the PCM-CTC module. for answers to questions not adequately covered in this section, contact the WinSystems Technical Support group via telephone at (817) 274-7553, via FAX at (817) 548-1358 or through the support BBS at (817) 861-8739. Appendices C and D provide technical datasheet reprints on the 8254 counter timer chips and the 8259 Interrupt controller IC. Refer to these documents for detailed programming, and register mapping information.

The PCM-CTC is a multi-purpose counter/timer module allowing event counting, precision timing intervals and a variety of hardware and software controlled modes of operation. Six 16-Bit counter channels are terminated at two I/O connectors. Each channel may use an independent external clock source or any channel may use one of two onboard clock sources. The gates for each timer are externally available and may be controlled from external hardware or from the output of another channel. All of the counter outputs are available as external buffered outputs and may also serve as interrupt sources when enabled with the onboard 8259 interrupt controller. Two auxiliary interrupt input pins are also available.

2.2 I/O Address Select

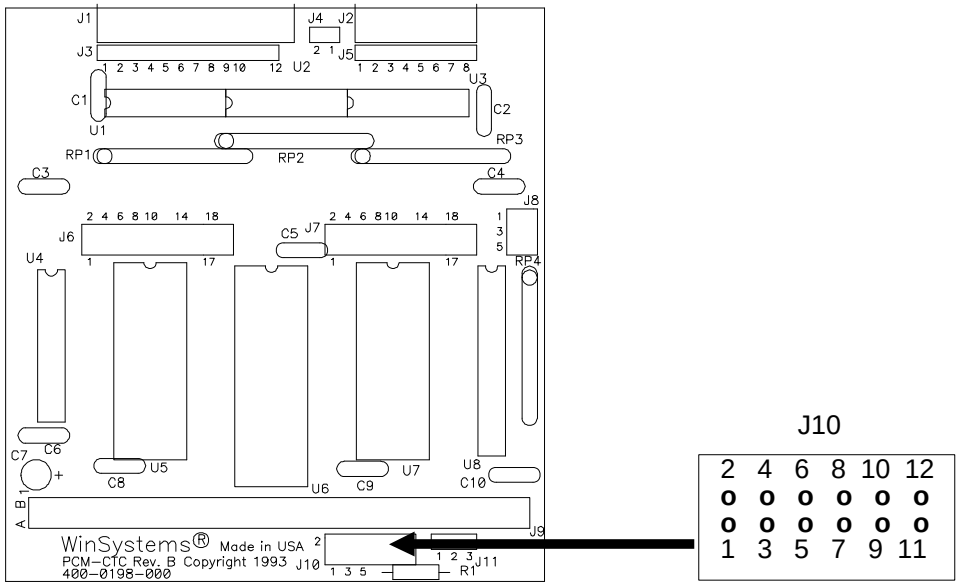


I/O Address Select
Jumper J8

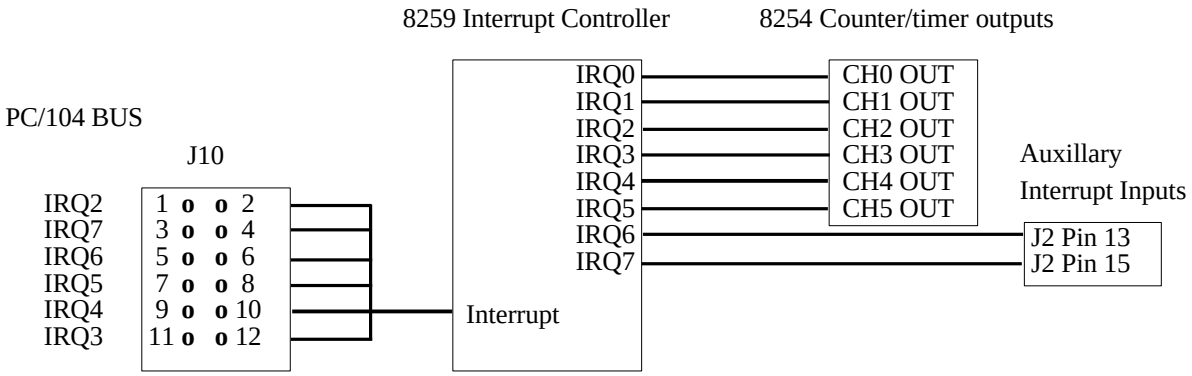
The Base address of the PCM-CTC is set via user installable jumpers on J8. The table below shows the J8 jumpering and the I/O addresses of the on-board devices.

J8 Jumpering	CH0-CH2 Counter/Timer Address	CH3-CH5 Counter/Timer Address	Interrupt Controller Address	INTAK I/O Port Address
1-2, 3-4, 5-6	100H	104H	108H	10CH
3-4, 5-6	110H	114H	118H	11CH
1-2, 5-6	120H	124H	128H	12CH
5-6	130H	134H	138H	13CH
1-2, 3-4	140H	144H	148H	14CH
3-4	150H	154H	158H	15CH
1-2	160H	164H	168H	16CH
none	170H	174H	178H	17CH

2.3 Interrupt Routing Select



All of the counter/timer output pins as well as 2 auxiliary input pins are routed to the on-board 8259 interrupt controller. The interrupt output from the 8259 is then routed to a user configuration block at J10 allowing selection of any of 6 PC/104 interrupt pins to carry the interrupt to the processor. The pictorial on the following illustrates the interrupt routing.



PCM-CTC Interrupt Routing

2.3.1 Interrupt usage

Due to the limitations of the PC/104 bus which does not allow for slaved interrupt controllers on the bus, a special technique is required to utilize the onboard interrupt controller and to obtain a unique vector corresponding to the source of the interrupt. The following steps illustrate how to overcome this shortcoming using the special capabilities of the PCM-CTC

1. Initialize the interrupt controller onboard the PCM-CTC as if it were a master controller. Program the base vector number as 0.

The following initialization pseudo-code demonstrates the controller setup.

```
out PIC_BASE,13H        ; Edge triggered, single mode
out PIC_BASE+1,0        ; Base vector of 0
out PIC_BASE+1,0dh      ; Buffered mode master
out PIC_BASE,+1,0ffh    ; Mask all interrupts
```

2. Install the interrupt service routine for the main interrupt controller to service PCM-CTC requests at the appropriate vector depending on the routing of J10.

3. Unmask the interrupt at the main interrupt controller to which the PCM-CTC's interrupt is routed.

4. Program the PCM-CTC counter/timers for the desired mode(s) of operation.

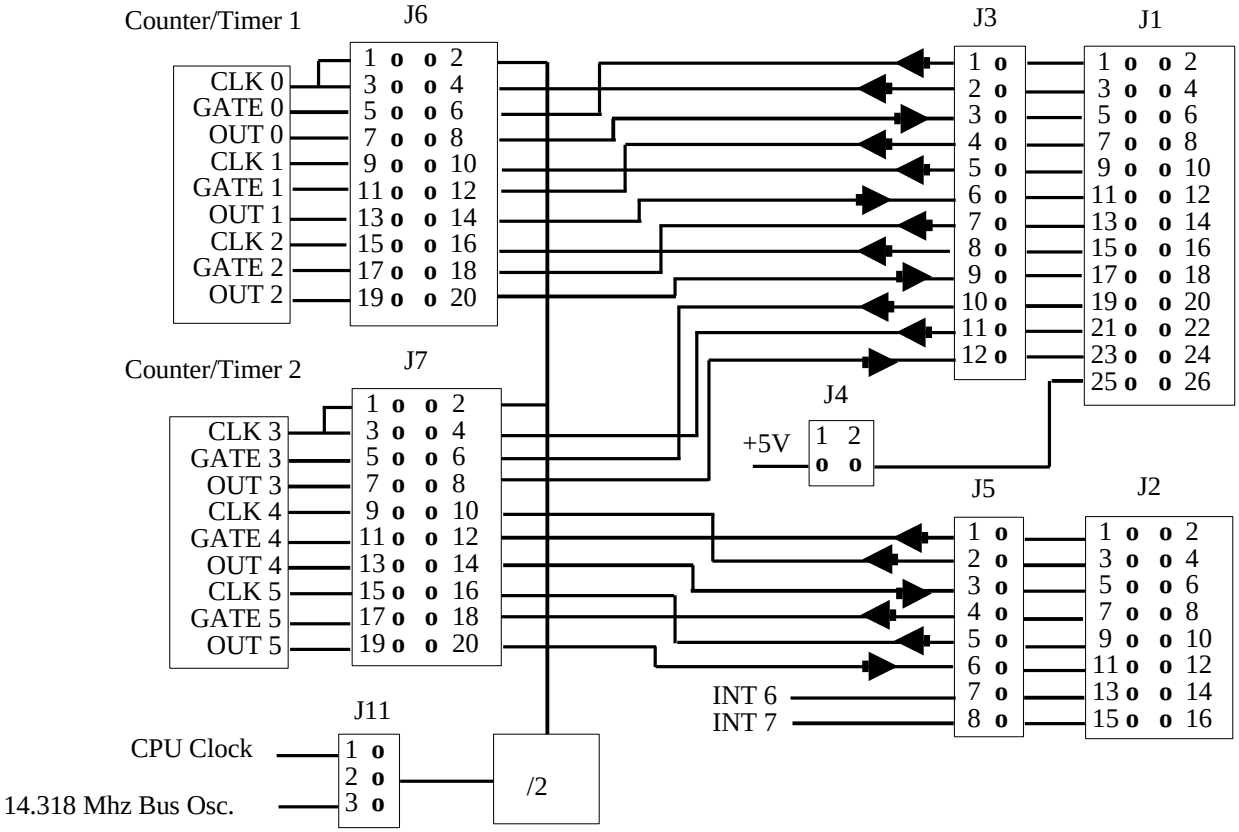
5. Unmask the desired interrupt inputs to the PCM-CTC's interrupt controller.

6. When an interrupt occurs the interrupt service routine issues two reads from the INTAK I/O port. The first value read is ignored. The second value read will be the interrupt number on the PCM-CTC requiring service ,a jump to the appropriate handler can be calculated using this value.

7. Before exiting the interrupt service routine issue the EOI (End of interrupt) command to both interrupt controllers.

2.4 External Connections

The PCM-CTC allows for nearly unlimited versatility in connecting to the outside world. All of the Clock, Gate, and Output lines are buffered and available for interconnection via the I/O connectors at J1 and J2. In parallel with the I/O connectors are two wire-wrap headers at J3 and J5 respectively which allow for additional interconnection capability. A pictorial of the I/O connectors, the routing headers J6 and J7 are shown below:



Note : that the I/O signals at J1, J2, J3, and J5 are all buffered using inverting Schmidt triggered gates. When making external connections keep in mind that the signals are inverted from the input or output polarity at the counter timer itself.

When used with the TRM-500-3 termination board a jumper placed on J4 will route 5 Volts to pin 25 of J1, allowing the termination board to be powered from the PCM-CTC directly through the I/O cable.

2.5 Connector/Jumper Summary

Connector Jumper	Description	Page Reference
J1	I/O Connector Channels 0-3	2-4
J2	I/O Connector Channels 4-5	2-4
J3	Wire-Wrap header Channels 0-3	2-4
J4	+5 Volt enable to J1	2-4
J5	Wire-wrap header Channels 4-5	2-4
J6	Routing Header Channels 0-2	2-4
J7	Routing Header Channels 3-5	2-4
J8	I/O Address Select	2-1, 2-2
J9	PC/104 Bus connector	N/A
J10	Interrupt routing header	2-2, 2-3
J11	Bus Clock source select	2-4

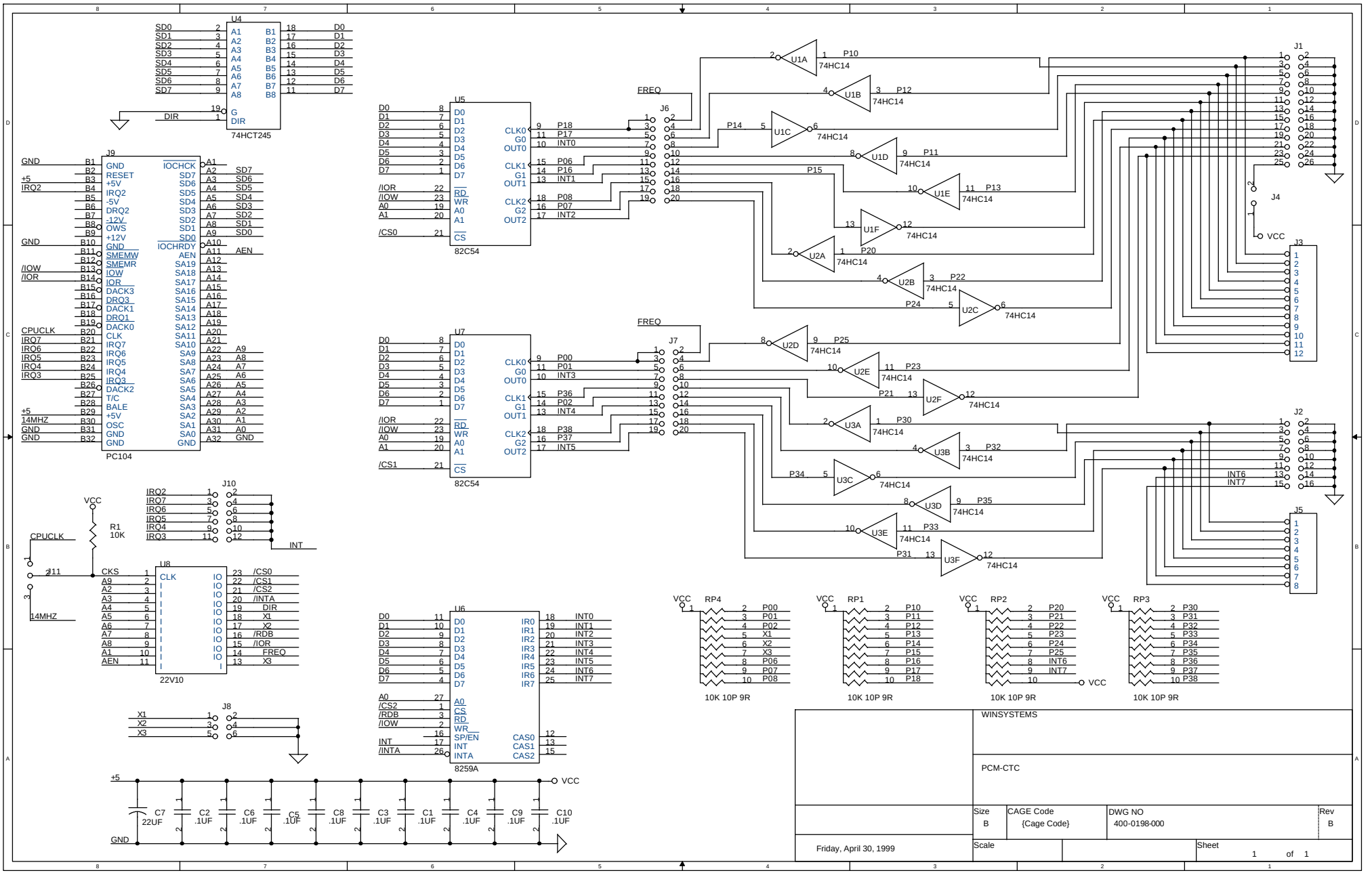
Appendix A

Datasheet Reprint

Printable datasheet in PDF format	intel8254.pdf
Printable datasheet in PDF format	intel8259a.pdf

Appendix B

PCM-CTC Schematic Diagram


U4
74HCT245
DIR
U5
82C54
U7
82C54
J6
J7
FREQ
U1A
U1B
U1C
U1D
U1E
U1F
U2A
U2B
U2C
U2D
U2E
U2F
U3A
U3B
U3C
U3D
U3E
U3F
74HC14
J1
J2
J3
J4
J5
VCC
J9
PC104
J10
INT
R1
10K
J11
CPUCLK
14MHZ
U8
22V10
U6
8259A
J8
RP4
RP1
RP2
RP3
10K 10P 9R
C7 22UF
C2 .1UF
C6 .1UF
C5 .1UF
C8 .1UF
C3 .1UF
C1 .1UF
C4 .1UF
C9 .1UF
C10 .1UF
GND
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Size B
CAGE Code {Cage Code}
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Rev B
Friday, April 30, 1999
Scale
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2. Reason for the return.
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4. Name, address, telephone and FAX number of the person making the request.
5. Do not debit WinSystems for the repair. WinSystems does not authorize debits.

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