

OPERATIONS MANUAL

LPM/MCM-OUT48

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REVISION HISTORY
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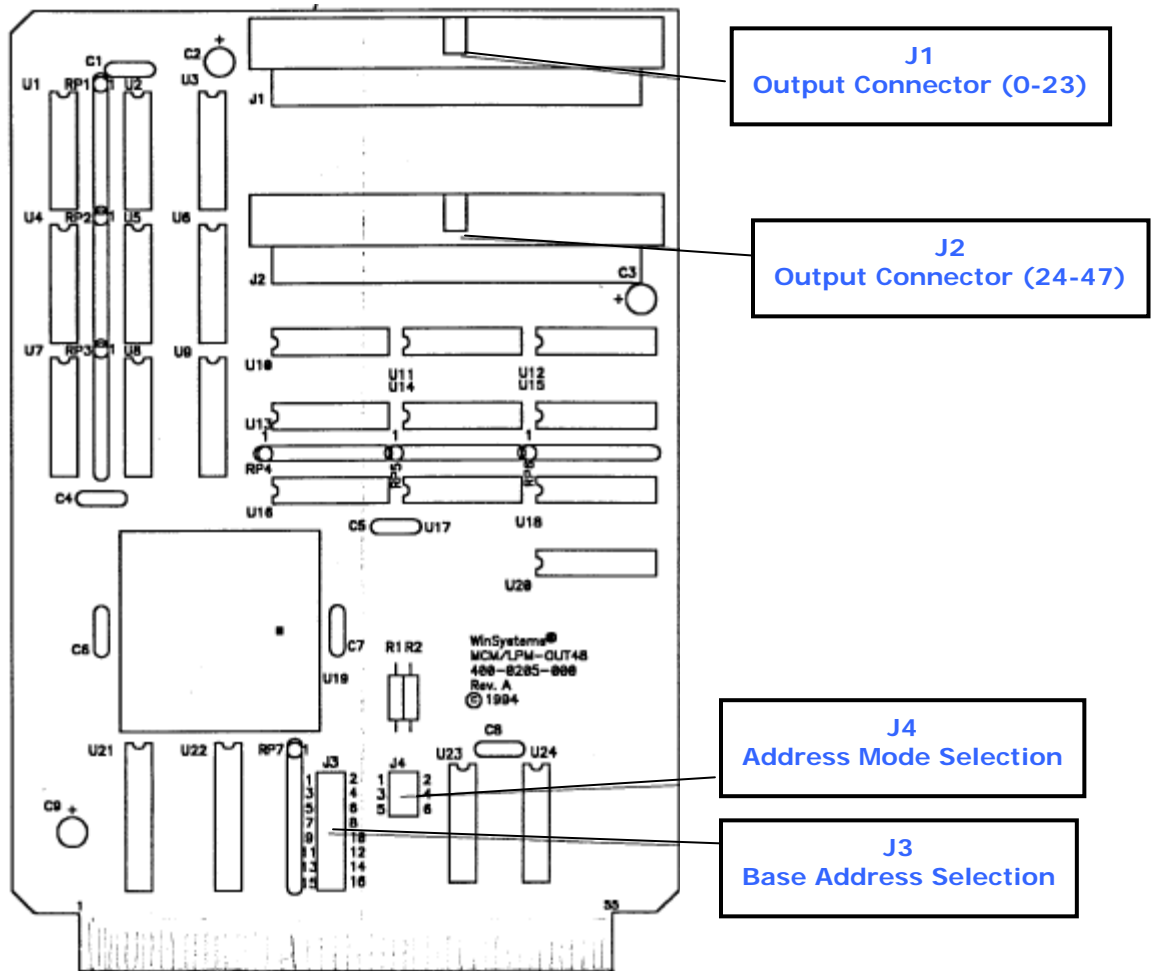
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Visual Index – Quick Reference

For the convenience of the user, a copy of the Visual Index has been provided with direct links to connector and jumper configuration data.



General Information

Features

- 48 optically isolated digital output pin per card
- read back available for each pin
- 50-pin connector directly interfaces to Opto Racks
- 8-bit STD-Bus interface

General Information

The LPM/MCM-OUT48 is a low cost high density Output ONLY card.

Specifications

Electrical

Bus Interface	: STD-Bus and CMOS STD-Bus compatible
LPM – VCC	: +5V @ 12mA (no outputs loaded)
MCM – VCC	: +5V @ 120mA (no outputs loaded)
Outputs	: +7V to +30V @ 100mA each, maximum

Memory

Addressing	: 10-bits, or 8+IOEXP, jumper selectable
I/O Space	: each board occupies 8 ports

Mechanical

Dimensions	: 4.5" x 6.5" x .06"
PC Board	: FR4 Epoxy Glass with 2 signal layers, 2 power planes, screened component legend, gold plated fingers, and plated through holes.
Jumpers	: .025" square posts on 0.1" centers
Connectors	: two 2 x 25 .1" spaced shrouded male IDH connectors with .025" square pins

Environmental

Operating Temperature	: -40°C to +85°C (LPM) 0°C to 65°C (MCM)
Non-condensing Humidity	: 5 to 95%

LPM/MCM-OUT48 Technical Reference

Introduction

This manual is intended to provide the necessary information regarding configuration and usage of the PCM-DC/DC board. WinSystems maintains a Technical Support Group to help answer questions regarding usage, or programming of the board. For answers to questions not adequately addressed in this manual, contact Technical Support at (817) 274-7553 between 8AM and 5PM Central Time.

LPM/MCM-OUT48 Chipset

The LPM/MCM-OUT48 board uses the WS16C148 single-chip I/O. This WinSystems' exclusive device has many state-of-the-art features which greatly enhance performance.

Connector Pinout

Connectors **J1** and **J2** are used to connect the LPM/MCM-OUT48 to the outside world. These connectors are .1" spaced 2 x 25 pin shrouded headers with .025" square posts, compatible with IDC female headers.

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J1			J2		
O0	1 0 0 2	IGND	O24	1 0 0 2	IGND
O1	3 0 0 4	IGND	O25	3 0 0 4	IGND
O2	5 0 0 6	IGND	O26	5 0 0 6	IGND
O3	7 0 0 8	IGND	O27	7 0 0 8	IGND
O4	9 0 0 10	IGND	O28	9 0 0 10	IGND
O5	11 0 0 12	IGND	O29	11 0 0 12	IGND
O6	13 0 0 14	IGND	P30	13 0 0 14	IGND
O7	15 0 0 16	IGND	O31	15 0 0 16	IGND
O8	17 0 0 18	IGND	O32	17 0 0 18	IGND
O9	19 0 0 20	IGND	O33	19 0 0 20	IGND
O10	21 0 0 22	IGND	O34	21 0 0 22	IGND
O11	23 0 0 24	IGND	O35	23 0 0 24	IGND
O12	25 0 0 26	IGND	O36	25 0 0 26	IGND
O13	27 0 0 28	IGND	O37	27 0 0 28	IGND
O14	29 0 0 30	IGND	O38	29 0 0 30	IGND
O15	31 0 0 32	IGND	O39	31 0 0 32	IGND
O16	33 0 0 34	IGND	O40	33 0 0 34	IGND
O17	35 0 0 36	IGND	O41	35 0 0 36	IGND
O18	37 0 0 38	IGND	O42	37 0 0 38	IGND
O19	39 0 0 40	IGND	O43	39 0 0 40	IGND
O20	41 0 0 42	IGND	O44	41 0 0 42	IGND
O21	43 0 0 44	IGND	O45	43 0 0 44	IGND
O22	45 0 0 46	IGND	O46	45 0 0 46	IGND
O23	47 0 0 48	IGND	O47	47 0 0 48	IGND
+Vin	49 0 0 50	+Vin	+Vin	49 0 0 50	+Vin

O 0-47 are the Output pins. Output pins provide a sink for each of the loads. +Vin is the connection to the positive side of the supply sourcing the loads. It provides a

path for the suppression diodes contained in the drivers. IGND is the Isolated Ground to which the loads are sunk. Both +Vin and IGND are optically isolated from the supply present at the STD-Bus.

I/O Map

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Each board has 6 registers accessible through 6 ports as follows:

Port	D7	D6	D5	D4	D3	D2	D1	D0
0	O7	O6	O5	O4	O3	O2	O1	O0
1	O15	O14	O13	O12	O11	O10	O9	O8
2	O23	O22	O21	O20	O19	O18	O17	O16
3	O31	O30	O29	O28	O27	O26	O25	O24
4	O39	O38	O37	O36	O35	O34	O33	O32
5	O47	O46	O45	O44	O43	O42	O41	O40

Ports 0-2 (O0-23) correspond to J1.

Ports 3-5 (O24-47) correspond to J2.

O0-47: Output registers. A '1' written to any given bit causes the corresponding output pin to sink current. A '0' causes the output to float (open collector, no pull-up). The voltage applied must not exceed 30 Volts.

All 6 registers are set to all '0's with System Reset (STD-Bus pin 47).

STD Bus Interface

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The LPM/MCM-OUT 48 is designed for use in STD-Bus systems.

J3: Base Address Select. This value will be added to the Port number to give the actual address of a given port. For instance a base address of 100h gives Port 3 an actual address of 103h.

J4: Addressing mode configuration.

Jumper J4 (1-2), (3-4) to enable 10 bit addressing. Leave J4 (1-2), (3-4) and J3 (11-12), (13-14) open to use only 8 bits.

Jumper J4 (5-6) to enable IOEXP, then J3 (15-16) jumpered to qualify IOEXP low, or open to qualify IOEXP high. You must be in 8 bit mode to use IOEXP.

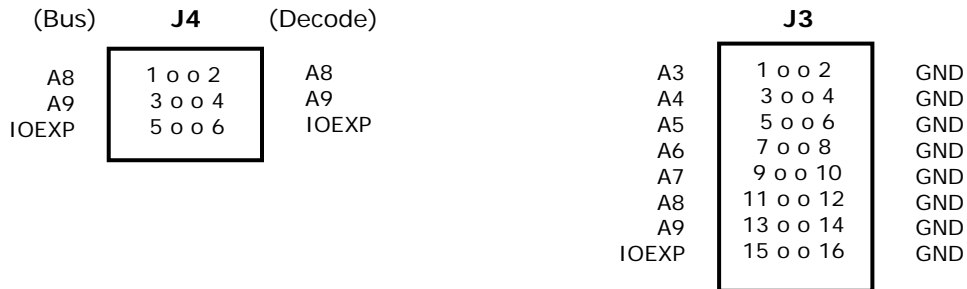
A jumper installed is a zero.

Example: 110h, 10 bit addressing, no IOEXP.

J4: 1-2, 3-4

J3: 1-2, 5-6, 7-8, 9-10, 13-14

Extended 10bit addressing for PC implementations. In 8 bit systems (Z80), IOEXP can be used to double the addressing range to 512 ports. IOEXP can be qualified high, or low.



APPENDIX A

Sample Code / Examples

The LPM/MCM-out48 is a relatively simple board from a software standpoint. It is essentially six output latches with read back. To turn on the current sink[s], set the appropriate bit[s]. To turn off the current sink[s], rest the appropriate bit[s]. All six ports may be written to read at any time. While the read back of these ports does reflect the pin at the I.C., it does not necessarily reflect the status of the actual output. The read back should be considered to be simply the contents of the latch, as last written.

Writing a '1' to the last significant bit of the least significant port of a connector will activate the current sink associates with pin 1 of that connector.

i.e.

```
outp(BASE,1);      /*Connect J1's pin 1 to IGround, Odd pins 3-15 released*/  
outo(BASE+3, 1):  /*Connect J2's pin 1 to IGround, Odd pins 3-15 released*/
```

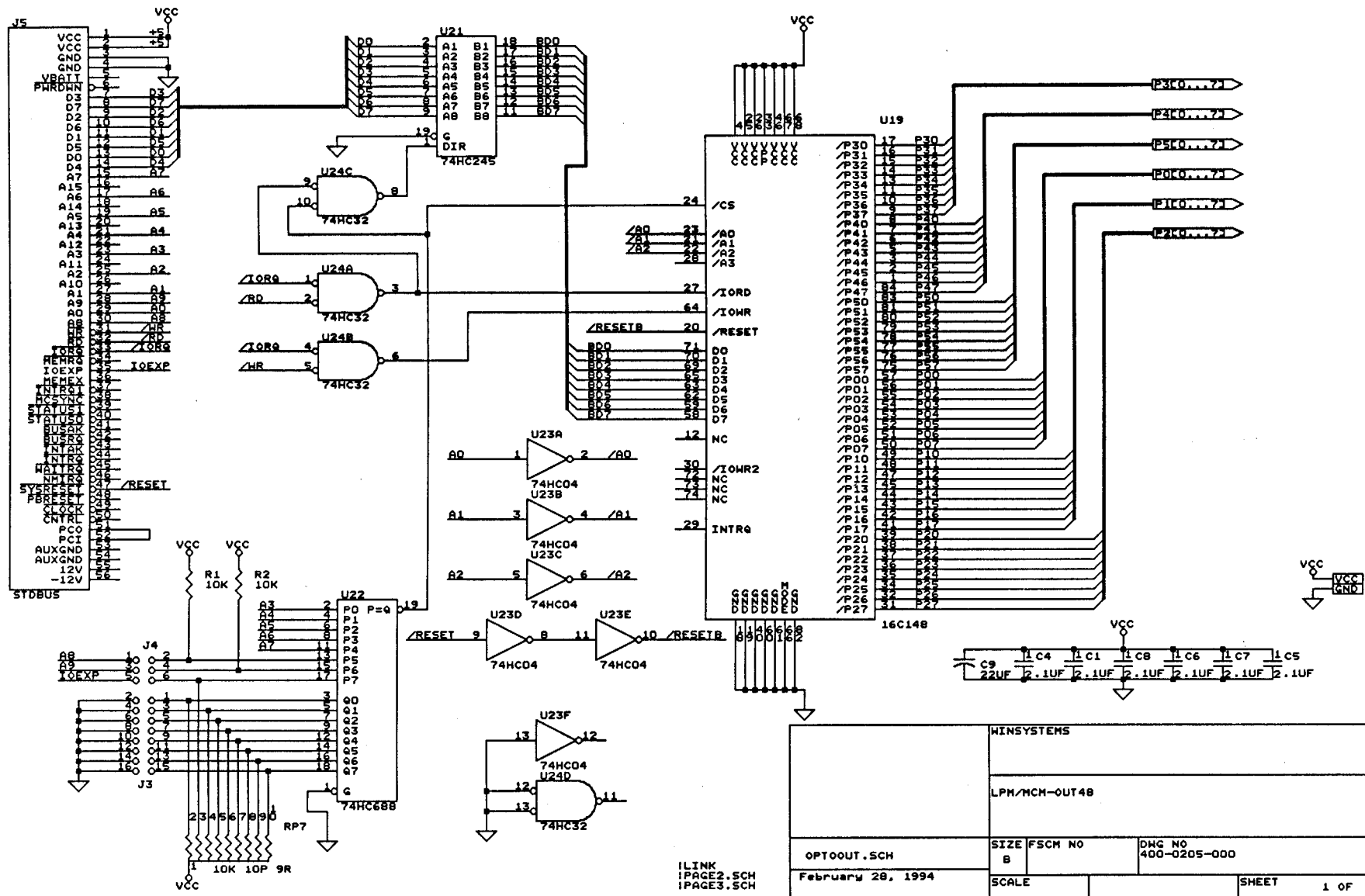
Conversely, writing a '0' will release the pin from IGround.

i.e.

```
outp(BASE,0);      /*Release J1's Odd pins from IGround*/  
outo(BASE+3, 0):  /*Release J2's Odd pins from IGround*/
```

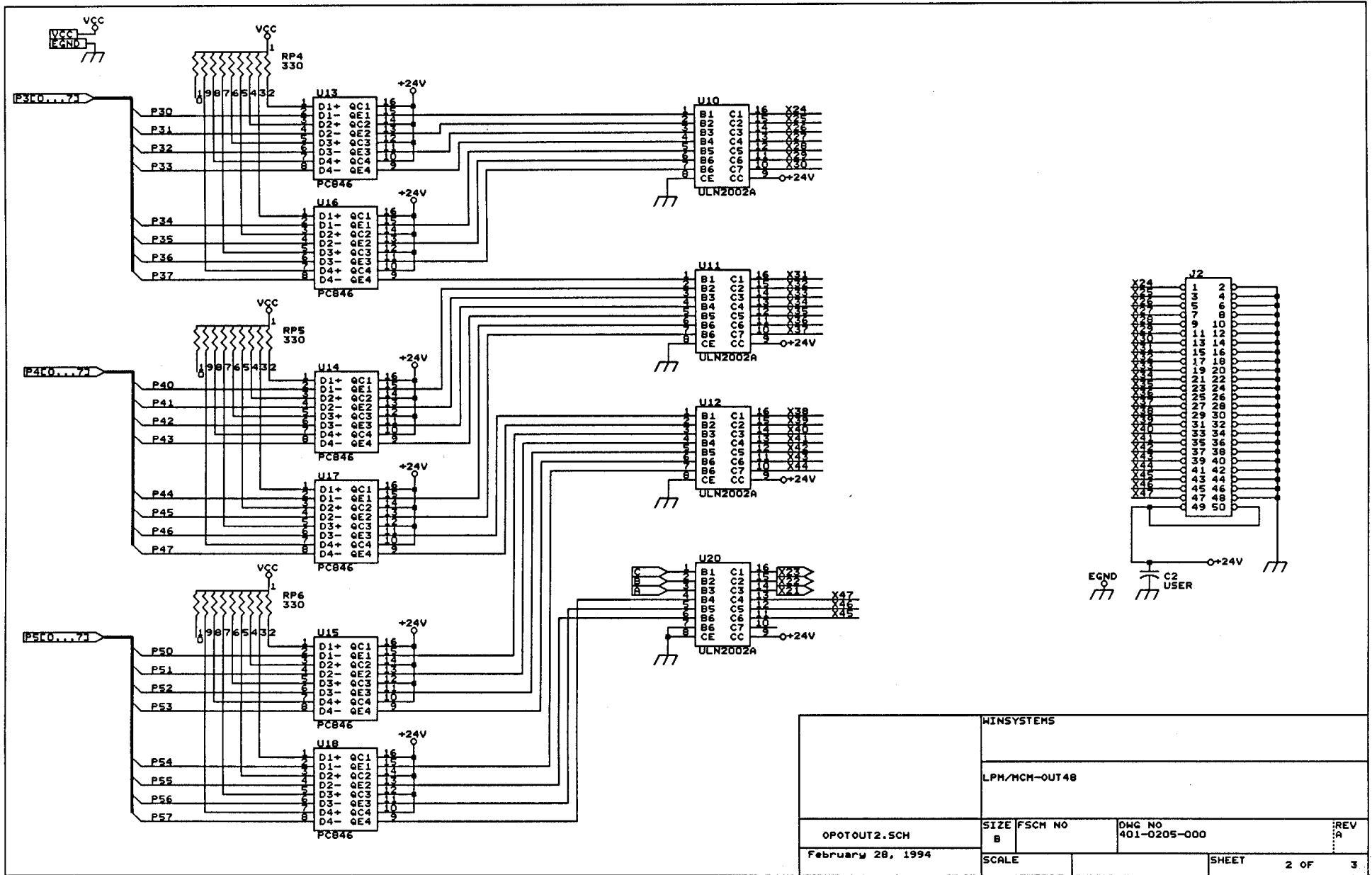
APPENDIX B

LPM/MCM-OUT48 Schematic Diagram

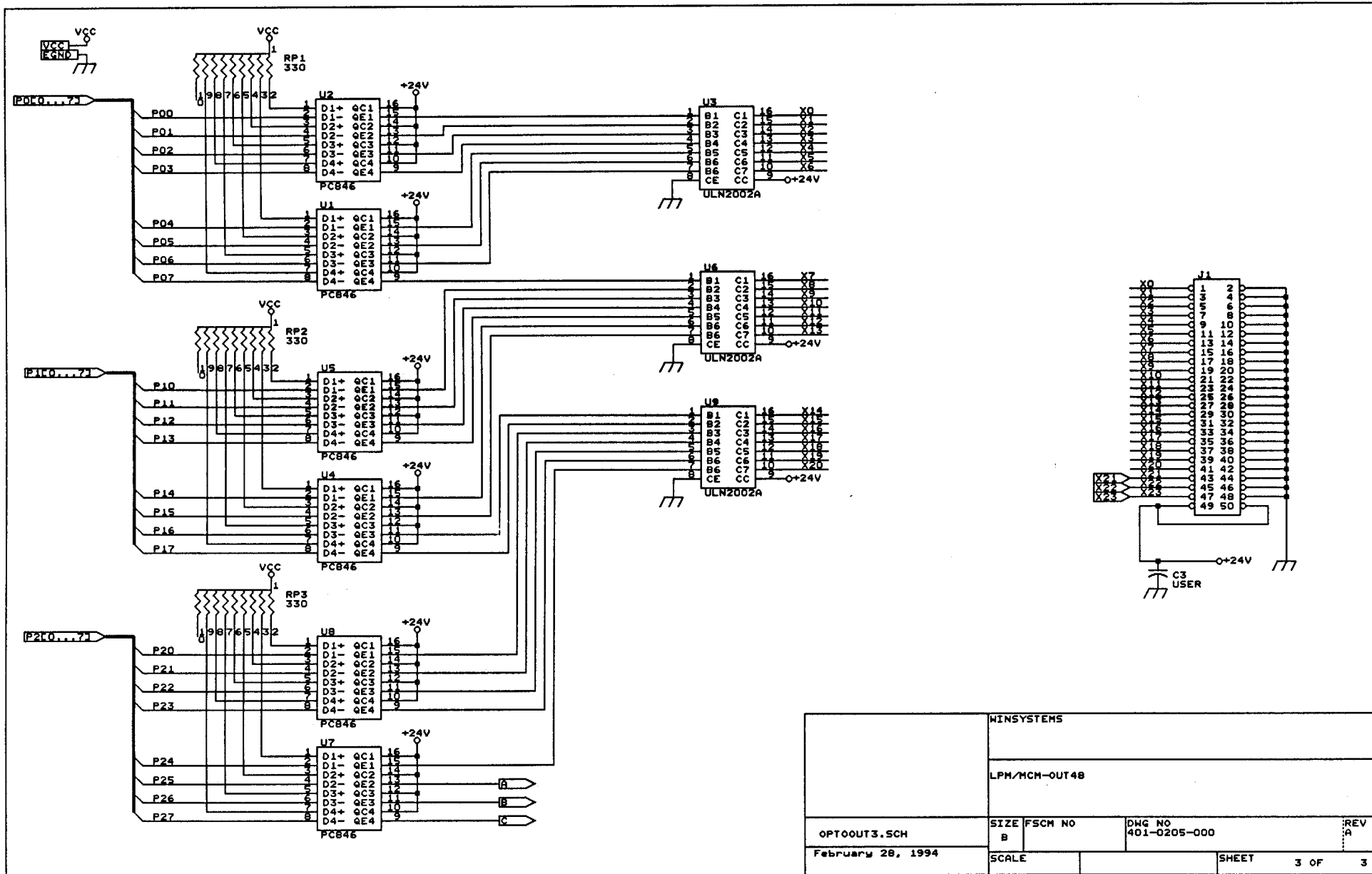


ILINK
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IPAGE3.SCH

OPTOOUT.SCH		WINSYSTEMS	
February 28, 1994		LPH/MCH-OUT48	
SIZE B	FSCM NO	DWG NO 400-0205-000	REV A
SCALE		SHEET 1 OF 3	



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OP0TOUT2.SCH	SIZE B	FSC# NO	DWG NO 401-0205-000
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		SHEET	2 OF 3



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OPT00T3.SCH	SIZE B	FSCM NO	DWG NO 401-0205-000
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		SHEET	3 OF 3

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2. Reason for the return.
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