OPERATIONS MANUAL
LPM/MCM-OPTO48

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REVISION HISTORY
P/N 403-0204-000

ECO Number	Date Code	Rev Level
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1 General Information

1.1 Features

- 48 Optically Isolated Digital Input pins per card.
- Extensive Interrupt Capabilities, bit selectable.
- Interrupt ID register for more efficient ISR's.
- Read back / Input available for each pin.
- 50 Pin connector directly interfaces to Opto Racks.
- All 48 Inputs are hardware debounced.
- 8-bit STD-Bus interface.

1.2 General Description

The LPM/MCM-OPTO48 is a low cost high density Input Only card with extensive interrupt capabilities.

1.3 Specifications

1.3.1 Electrical

Bus Interface: STD-Bus & CMOS STD-Bus compatible.

VCC	+5V	@	12mA	(LPM)
VCC	+5V	@	120mA	(MCM)

1.3.2 Memory

Addressing: 10-bits, Jumper selectable.

I/O Space: Each board occupies 16 ports.

1.3.3 Mechanical

Dimensions: 4.5 x 6.5 x 0.6 inches.

PC Boards: FR-4 epoxy glass with 2 signal layers, screened component legend, gold plated fingers, and plated through holes.

Jumpers: .025" square posts on 0.1" centers.

Connectors: Two 2 x 25 .1" spaced shrouded male IDH connectors with .025" square pins.

1.3.4 Environmental

Operating Temperature -40° to 85° C (LPM)
0° to 65° C (MCM)

Non-condensing Humidity: 5 to 95%

2.3 Connector Pinout

Connectors J1 and J2 are used to connect the LPM/MCM-OPTO48 to the outside world. These connectors are .1" spaced 2x25 pin shrouded headers with .025" square posts, compatible with IDC female headers.

	J 1		
Signal	Pin No.		Signal
S0+	1	2	S0-
S1+	3	4	S1-
S2+	5	6	S2-
S3+	7	8	S3-
S4+	9	10	S4-
S5+	11	12	S5-
S6+	13	14	S6-
S7+	15	16	S7-
S8+	17	18	S8-
S9+	19	20	S9-
S10+	21	22	S10-
S11+	23	24	S11-
S12+	25	26	S12-
S13+	27	28	S13-
S14+	29	30	S14-
S15+	31	32	S15-
S16+	33	34	S16-
S17+	35	36	S17-
S18+	37	38	S18-
S19+	39	40	S19-
S20+	41	42	S20-
S21+	43	44	S21-
S22+	45	46	S22-
S23+	47	48	S23-
J3.49	49	50	J3.50

	J 2		
Signal	Pin No.		Signal
S24+	1	2	S24-
S25+	3	4	S25-
S26+	5	6	S26-
S27+	7	8	S27-
S28+	9	10	S28-
S29+	11	12	S29-
S30+	13	14	S30-
S31+	15	16	S31-
S32+	17	18	S32-
S33+	19	20	S33-
S34+	21	22	S34-
S35+	23	24	S35-
S36+	25	26	S36-
S37+	27	28	S37-
S38+	29	30	S38-
S39+	31	32	S39-
S40+	33	34	S40-
S41+	35	36	S41-
S42+	37	38	S42-
S43+	39	40	S43-
S44+	41	42	S44-
S45+	43	44	S45-
S46+	45	46	S46-
S47+	47	48	S47-
J4.49	49	50	J4.50

In addition, J3 parallels J1 and J4 parallels J2. This is to allow the user to install .1" spaced shorting bars if it is desired to provide common returns for two or more inputs.

2.4 I/O Map

Each Board has 20 registers accessible through 16 ports as follows:
(Ports 0-7 are always available)

Port	D7	D6	D5	D4	D3	D2	D1	D0
0	I 7	I 6	I 5	I 4	I 3	I 2	I 1	I 0
1	I 15	I 14	I 13	I 12	I 11	I 10	I 9	I 8
2	I 23	I 22	I 21	I 20	I 19	I 18	I 17	I 16
3	I 31	I 30	I 29	I 28	I 27	I 26	I 25	I 24
4	I 39	I 38	I 37	I 36	I 35	I 34	I 33	I 32
5	I 47	I 46	I 45	I 44	I 43	I 42	I 41	I 40
6	0	0	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
7	**IA1**	**IA0**	0	0	0	0	0	0

(Ports 8-D with IA1 & IA0 = 00) recommended rest position.

8	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0
A	0	0	0	0	0	0	0	0
B	0	0	0	0	0	0	0	0
C	0	0	0	0	0	0	0	0
D	0	0	0	0	0	0	0	0

(Ports 8-D with IA1 & IA0 = 01)

8	Pol 7	Pol 6	Pol 5	Pol 4	Pol 3	Pol 2	Pol 1	Pol 0
9	Pol 15	Pol 14	Pol 13	Pol 12	Pol 11	Pol 10	Pol 9	Pol 8
A	Pol 23	Pol 22	Pol 21	Pol 20	Pol 19	Pol 18	Pol 17	Pol 16
B	Pol 31	Pol 30	Pol 29	Pol 28	Pol 27	Pol 26	Pol 25	Pol 24
C	Pol 39	Pol 38	Pol 37	Pol 36	Pol 35	Pol 34	Pol 33	Pol 32
D	Pol 47	Pol 46	Pol 45	Pol 44	Pol 43	Pol 42	Pol 41	Pol 40

(Ports 8-D with IA1 & IA0 = 10)

8	Ena 7	Ena 6	Ena 5	Ena 4	Ena 3	Ena 2	Ena 1	Ena 0
9	Ena 15	Ena 14	Ena 13	Ena 12	Ena 11	Ena 10	Ena 9	Ena 8
A	Ena 23	Ena 22	Ena 21	Ena 20	Ena 19	Ena 18	Ena 17	Ena 16
B	Ena 31	Ena 30	Ena 29	Ena 28	Ena 27	Ena 26	Ena 25	Ena 24
C	Ena 39	Ena 38	Ena 37	Ena 36	Ena 35	Ena 34	Ena 33	Ena 32
D	Ena 47	Ena 46	Ena 45	Ena 44	Ena 43	Ena 42	Ena 41	Ena 40

(Ports 8-D with IA1 & IA0 = 11)

8	P/C 7	P/C 6	P/C 5	P/C 4	P/C 3	P/C 2	P/C 1	P/C 0
9	P/C 15	P/C 14	P/C 13	P/C 12	P/C 11	P/C 10	P/C 9	P/C 8
A	P/C 23	P/C 22	P/C 21	P/C 20	P/C 19	P/C 18	P/C 17	P/C 16
B	P/C 31	P/C 30	P/C 29	P/C 28	P/C 27	P/C 26	P/C 25	P/C 24
C	P/C 39	P/C 38	P/C 37	P/C 36	P/C 35	P/C 34	P/C 33	P/C 32
D	P/C 47	P/C 46	P/C 45	P/C 44	P/C 43	P/C 42	P/C 41	P/C 40

2.4 I/O Map (Cont.)

IA1-IA0: Internal Address bits. These bits provide a window into the register array for the interrupt portion of the chip. They are configured by a write to the two most significant bits of port 7. These two bits determine the access available through ports 8-D. Zero has no write function, and always reads zeroes. It is recommended that all routines that deal with interrupt configuration registers return IA1-IA0 to zero, to prevent accidental writes.

Ports 0-2 (I0-23) correspond to J1, and can always be read.

Ports 3-5 (I24-47) correspond to J2, and can always be read.

I0-47: Input registers (read only). A current source of 10mA = 1 and 0mA = 0. A switch in series with a power source and Ix+ - Ix- will show a reading of 1 for that pin when the switch is closed. A zero read-back means the pin is floating at less than 10 mA. The voltage applied must not exceed 30 Volts.

IRQ5-0: Interrupt I.D. bits. IRQ5-0 indicate an interrupt(s) from I/O Port(s) 5-0 respectively.

Pol 0-47: These bits determine the edge polarity of the interrupt, if the interrupt is enabled (see Ena 0-47). For each of these bits, a zero indicates that the corresponding pin will produce an interrupt on the rising edge. (Pin switching from 0 volts to 5 volts). Please note that upon receiving the interrupt, the I/O port address will have a ZERO for this bit. Conversely, a one in the Pol register will produce an interrupt on the falling edge, with a one at the I/O port.

Ena 0-47: These bits determine whether or not a pin will produce an interrupt. Setting a bit to 1 will enable the interrupt for the corresponding pin. Note: clearing the enable bit also clears the Pending bit. You may clear individual bits in a Pending register by toggling the corresponding enable bit.

P/C 0-47: Pending / Clear bits. Reading these registers gives you the interrupt(s) pending. Writing any value clears that byte. I.E., any output to register 8 will clear all bits in register 8. These bits are latched by the event, so that even a short duration pulse will be recognized. See Ena 0-47 above for information on clearing individual bits.

All 20 registers are set to all zero's with System Reset (STD-BUS pin 47).

2.5 Interrupt Routing

The LPM/MCM-OPTO48 has only one interrupt output. This pin must be routed to the appropriate BackPlane Interrupt line with J7. The jumpering for J7 is shown below.

Jumper 1-2 for STD-Bus pin 44 (INTRQ).
Jumper 3-4 for STD-Bus pin 37 (INTRQ1).
Jumper 5-6 for STD-Bus pin 50 (CNTRL).
Jumper 7-8 for STD-Bus pin 46 (NMIRQ).

	J 7		
	Pin	No.	
Std 44	1	2	IRQ
Std 37	3	4	IRQ
Std 50	5	6	IRQ
Std 46	7	8	IRQ

2.6 STD Bus Interface

The LPM/MCM-OPTO48 is designed for use in STD-Bus systems.

J6: Base Address Select. This value will be added to the Port number to give the actual address of a given port. For instance a base address of 100h gives Port 7 an actual address of 107h.

J5: Addressing mode configuration.

Jumper J5(1-2),(3-4) to enable 10 bit addressing. Leave J5(1-2),(3-4) & J6(9-10),(11-12) open to use only 8 bits.

Jumper J5(5-6) to enable IOEXP, then J6(13-14) jumpererd to qualify IOEXP low, or open to qualify IOEXP high. You must be in 8 bit mode to use IOEXP.

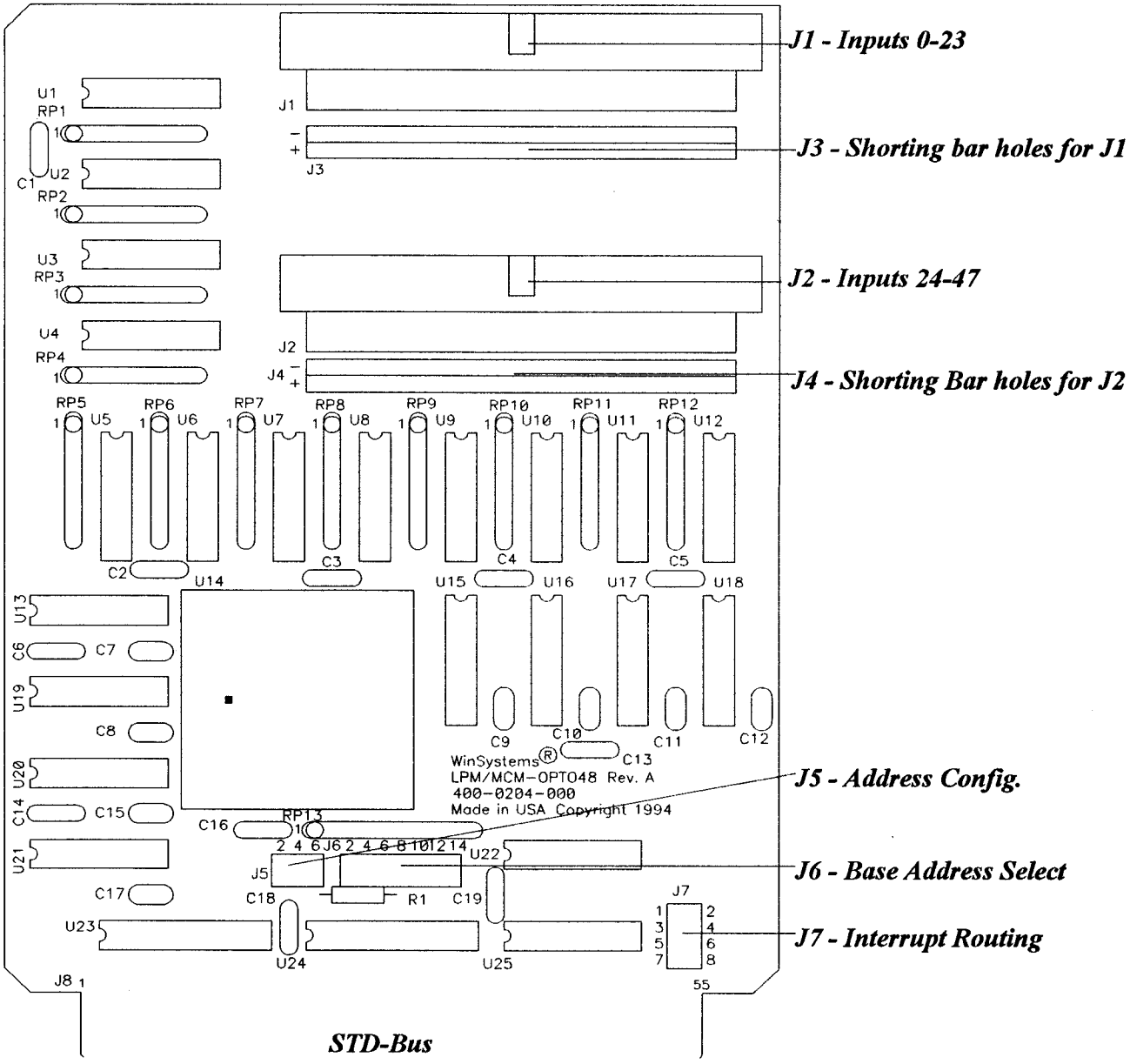
A jumper installed is a zero.
Example: 110h, 10 bit addressing, no IOEXP;
J5: 1-2 , 3-4
J6: 3-4 , 5-6 , 7-8 , 11-12.
Extended 10 bit addressing is for PC implementations. In 8 bit systems (Z80), IOEXP can be used to double the addressing range to 512 ports. IOEXP can be qualified high, or low.

(Bus)	J 5		(Decode)
Signal	Pin	No.	Signal
A8	1	2	A8
A9	3	4	A9
IOEXP	5	6	IOEXP

	J 6		
Signal	Pin	No.	Signal
A4	1	2	GND
A5	3	4	GND
A6	5	6	GND
A7	7	8	GND
A8	9	10	GND
A9	11	12	GND
IOEXP	13	14	GND

2.7 Connector/Jumper Summary

Connector:	Page	Description:
J1-2	2-2	Input Connectors
J3-4	2-2	Bus-Bar Holes
J5	2-5	Address Mode Select
J6	2-5	Base Address Select
J7	2-5	Interrupt Routing Jumper



Appendix A Sample Code / Examples

Example 1: Set up for interrupt on falling edge of input I12 (J1 pins 23 & 24).

When voltage is applied across J1 pins 23 & 24, an interrupt will be generated. As these are edge triggered interrupts, another event will not occur until voltage is removed, and re-applied.

BASE = Base address of card.

Initialization code:
First, turn off interrupts.

Then set the polarity:
Output 40h to port BASE+7
Output 10h to port BASE+9

Now set the enable:
Output 80h to port BASE+7
Output 10h to port BASE+9

At this point the chip is initialized, and you should initialize your ISR, 8259, enable the mask bit in the 8259, clear any pending interrupts triggered during initialization, and finally, re-enable interrupts.

Your ISR should read the IRQ register at BASE+6 to determine which port generated the interrupt, or if in fact it came from THIS card. (You may have more than one card sharing the same interrupts). Once the port(s) have been determined, you should read each of the P/C ports indicated to read the actual Pending bits. This method is preferable to simply reading the Input port because the P/C bits latch the event, while the Input is the present status. If the bit which caused the interrupt has since returned to the other state, a read of the Input port would not yield an inaccurate result. However, the Pending register will still show a one in the appropriate position indicating the event. Finally, your ISR should write to the P/C port(s) to clear the bits for the next event. If it is desired to clear only one of the bits, this may be done by reading the appropriate Enable port, XORing it against the desired bit, writing it, then writing the original value back out. In other words, toggle the appropriate Enable bit. This will clear the associated Pending bit without disturbing other bits in the Pending register.

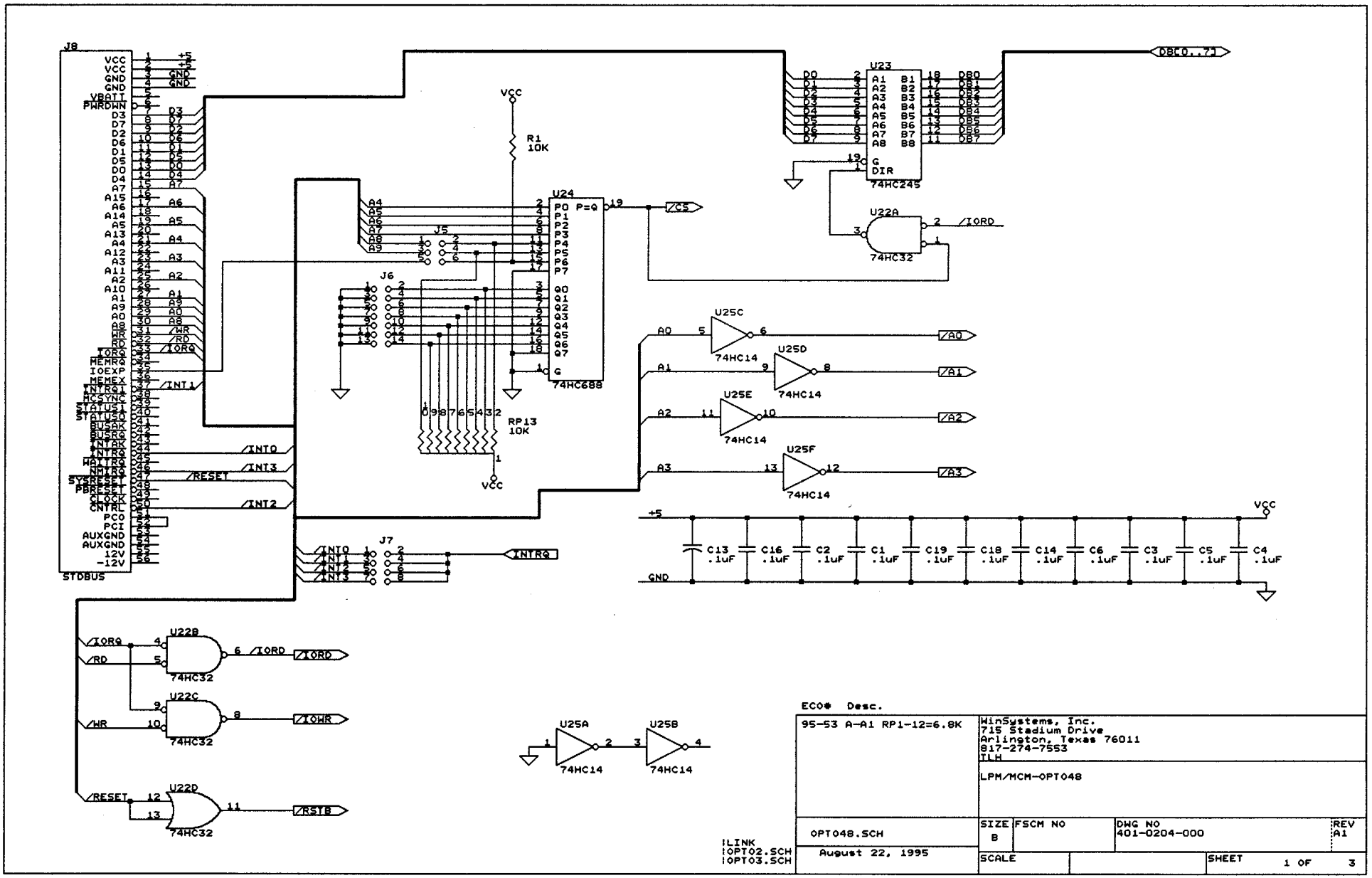
ISR:
Input from BASE+6 to determine which port(s).
Output C0h to BASE+7 to select pending registers.
Input from BASE+(8-D) to get actual pending bits.
Process information gathered.
Clear pending bits using one of the methods mentioned above.
Send EOI command to 8259 for end of interrupt.
Exit from ISR ASAP to minimize possibility of missing interrupts.

Note: If there is another way of knowing which interrupt has been received, such as having only one enabled, it is not necessary to read BASE+6 or BASE+(8-D) as reading these ports has no effect on the I.C. other than providing the CPU with the information.

C code example:

```
/* Note: this is an incomplete code fragment for demonstration purposes only.
   it will not compile due to omissions of detail. */
#define BASE = 0x300
unsigned char pends[6],intwaiting;
void main(void)
{
unsigned char a;
        for(a = 0; a < 6; a++)
                pends[a] = 0;
        intwaiting = 0;
        disable();                      /* Turn off interrupts */
        outp(BASE+7,0x40);              /* Point to Polarity Registers */
        outp(BASE+9,0x10);              /* Setting the appropriate bit means Falling Edge */
        outp(BASE+7,0x80);              /* Point to Enable Registers */
        outp(BASE+9,0x10);              /* Enable this bit. */
        outp)BASE+7,0);                 /* Set to safe place */
        /* code here to set up 8259 PIC */
        enable();
        while(!kbhit())                 /* Do this 'till someone hits a key */
        {
                if(intwaiting != 0)     /* If the ISR picked up something, process. */
                {
                        for(a = 0; a < 6; a++)      /* Display Results */
                        {
                                c = pends[a];
                                for(b = 0; b < 8; b++)
                                {
                                        if(c & 1)
                                        printf("Bit %d of port %d falling edge.\n",b,a);
                                }
                        }
                        intwaiting--;               /* Reset flag for next event */
                }
        }
}
void _interrupt far Isr(void)
{
unsigned char a;
        intwaiting++;
        outp(BASE+7,0xc0);              /* Point to Pending Registers */
        for( a = 0; a < 6; a++)
        {
                pends[a] = inp(BASE+8+a);
                outp(BASE+8+a,0);
        }
        outp(BASE+7,0);                 /* Set to safe place */
}
```

Appendix B Schematics



ECO# Desc.

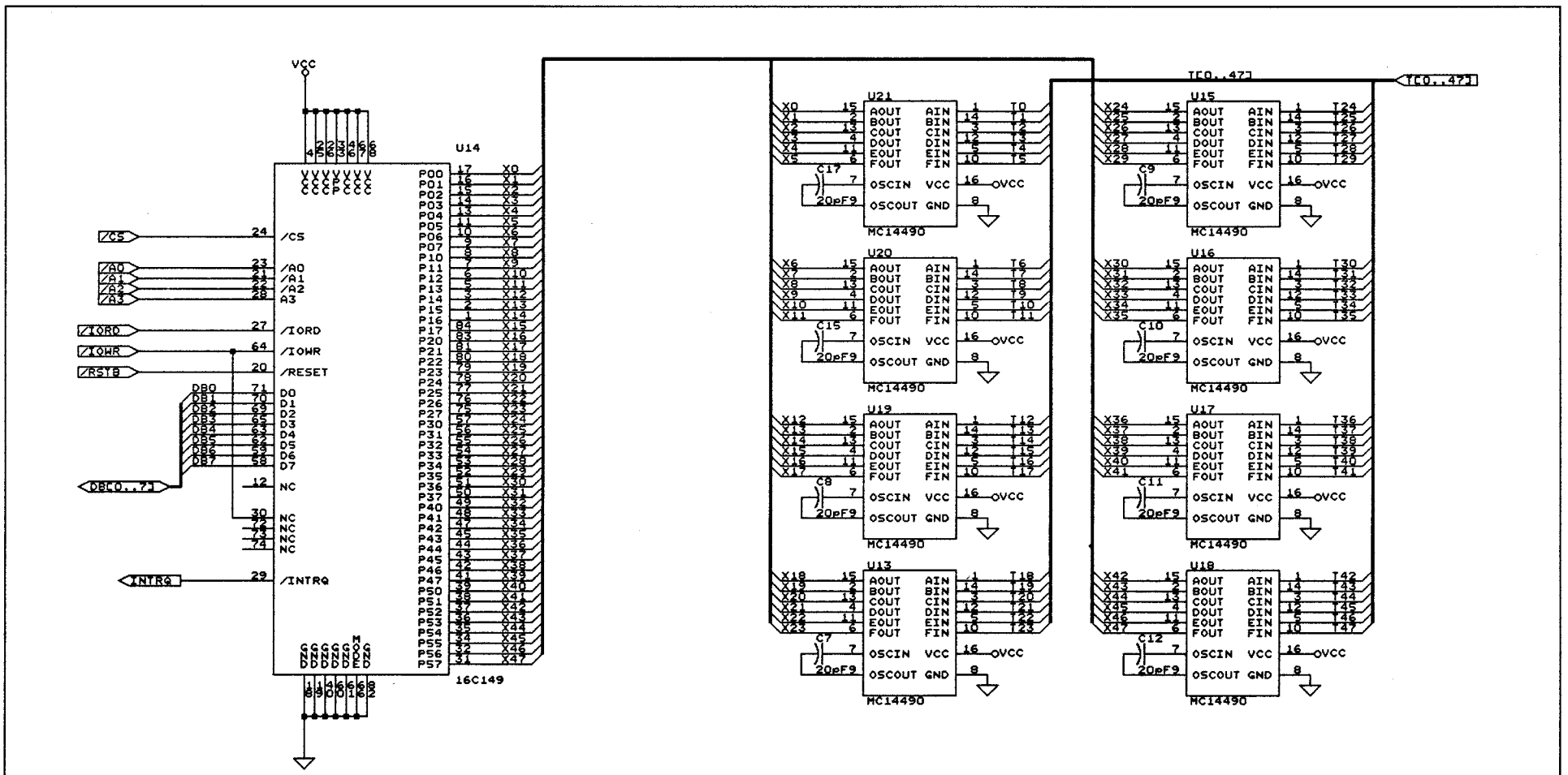
95-53 A-A1 RP1-12=6.8K

WinSystems, Inc.
715 Stadium Drive
Arlington, Texas 76011
817-274-7553
TLH

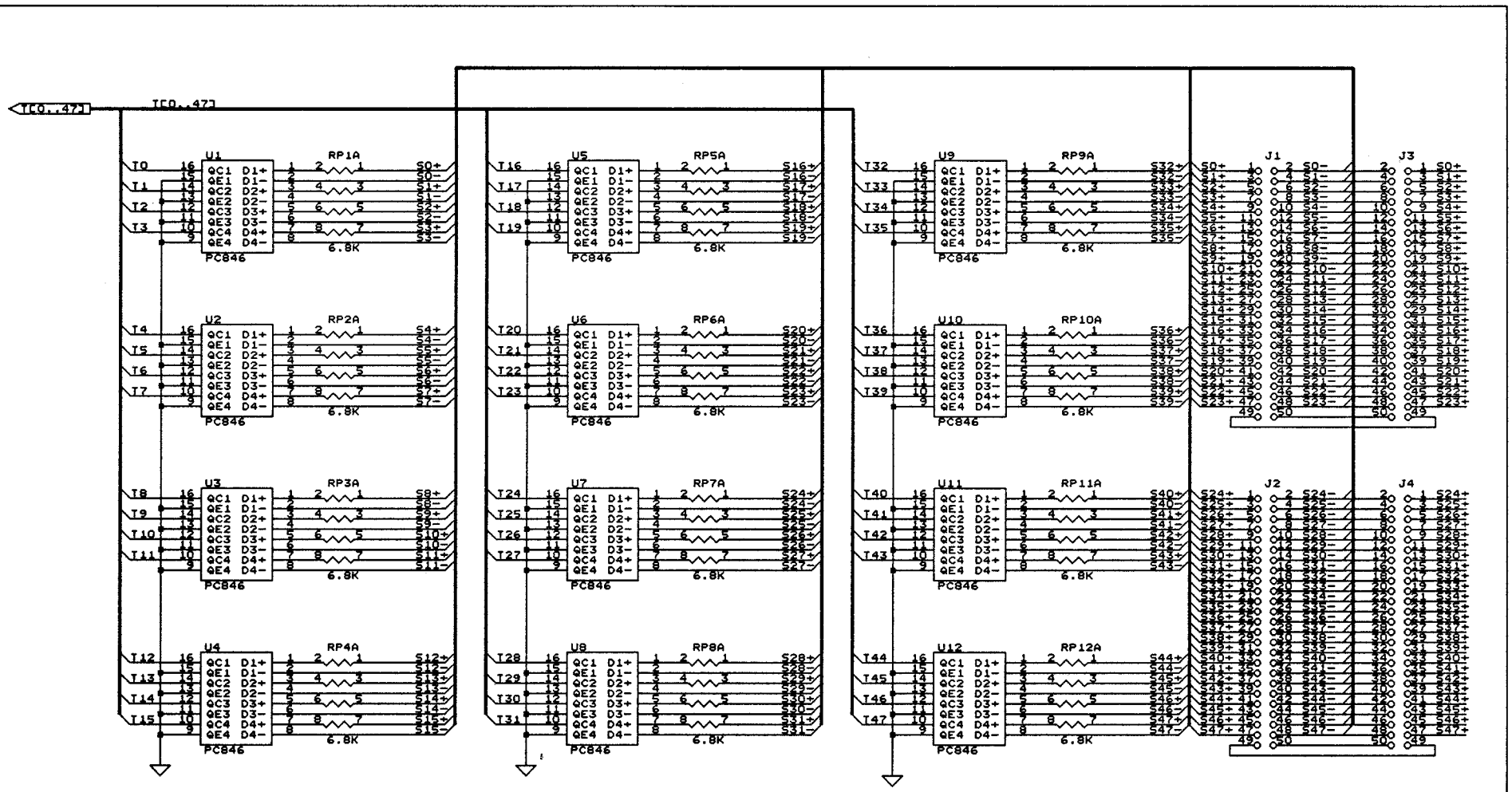
LPM/MCM-OPT048

OPT048.SCH	SIZE B	FSCM NO	DWG NO 401-0204-000 REV A1
August 22, 1995	SCALE		SHEET 1 OF 3

!LINK
!OPT02.SCH
!OPT03.SCH



	WinSystems, Inc. 715 Stadium Drive Arlington, Texas 76011 817-274-7553 TLH		
	LPM/MCM-OPT048		
OPT02.SCH August 22, 1995	SIZE B	FSCM NO	DWG NO 401-0204-000 REV A1
	SCALE		SHEET 2 OF 3



	WinSystems, Inc. 715 Stadium Drive Arlington, Texas 76011 817-274-7553 TLH			
	LPM/MCM-OPT048			
OPT03.SCH	SIZE B	FSCM NO	DWG NO 401-0204-000	REV A1
August 22, 1995	SCALE		SHEET 3 OF 3	

BEGINNING RANGE: LPM-OPTO48 ENDING RANGE: LPM-OPTO48

LEVEL	ITEM KEY	ITEM DESCRIPTION	BOM DESCRIPTION	LOC	OVHD KEY	ITEM TYPE	QTY REQUIRED
1	LPM-OPTO48	CMOS 48 LINE OPTO ISOLATED INPUT	BOARD				1
2	999-9999-001	SPECIAL NOTES	03-29-94 RC	ARLIN		Inv	1
2	0204-100-0000	ASSY LPM-OPTO48 REV A1	ASSY LPM-OPTO48 REV A	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	07-17-95 MEB ECO 95-53	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	03-29-94 RC RELEASED	ARLIN		Inv	1
3	>110-0010-003	CAP .1uF .2SP CER RAD C322C104M5	C1-C6,C13,C14,C16,C18,C19	ARLIN		Inv	11
3	>110-0029-003	CAP 22PF CER RAD ULTRA C315C220K	C7-C12,C15,C17	ARLIN		Inv	8
3	>114-0103-450	RESISTOR 10K 1/4 5%, CR25 10k 5%	R1	ARLIN		Inv	1
3	>117-0103-050	RN SIP 10P-9 10K L101S103 (BKMN)	RP13	ARLIN		Inv	1
3	>119-0682-050	RN SIP 8P-4, 6.8K CSC08A03682G	RP1-RP12	ARLIN		Inv	12
3	>201-0050-121	HEADER RA 2X25 IDH-50LP-SR3-TG/T	J1,J2	ARLIN		Inv	2
3	>201-0072-120	HDR 2X36 UN TSW-136-07-G-D	J5=2X3 J6=2X7 J7=2X4	ARLIN		Inv	.388
3	>230-0084-150	SOCKET 213084401 84 PLCC (510)	U14	ARLIN		Inv	1
3	>400-0204-000	PCB, LPM/MCM OPTO 48 REV A	PCB LPM/MCM OPTO 48 REV A	ARLIN		Inv	1
3	>500-0001-000	EJECTOR SCANBE S208	SATMP (BLUE) OPTO48	ARLIN		Inv	1
3	>500-0002-000	ROLL PIN MS171492	ROLL PIN MS171492	ARLIN		Inv	1
3	>741-0014-200	IC, 74HC14	U25	ARLIN		Inv	1
3	>741-0032-200	IC, 74HC32	U22	ARLIN		Inv	1
3	>741-0245-200	IC, 74HC245	U23	ARLIN		Inv	1
3	>741-0688-200	IC, 74HC688	U24	ARLIN		Inv	1
3	>743-0032-000	IC PC846N SHARP, ILQ621	U1-U12	ARLIN		Inv	12
3	>743-0034-000	IC, MC14490P	U13,U15-U21	ARLIN		Inv	8
3	>999-9999-001	SPECIAL NOTES	MASK HOLES FOR J3,J4	ARLIN		Inv	1
2	0204-300-0000	SUB ASSY L/MCM-OPTO48 REV A	SUB ASSY L/MCM-OPTO48 REV A	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	03-29-94 RC RELEASED	ARLIN		Inv	1
3	>901-0030-000	IC, A1020B-PL84C (16) ACTEL	U14 SEE ENG. FOR PROGRAM BEFORE STUFFING	ARLIN		Inv	1
3	>201-0002-000	PLUG JUMPER 999-19-310-00	J5=1-2 3-4	ARLIN		Inv	7
3	>999-9999-001	SPECIAL NOTES	J6=1-2 3-4 5-6 7-8	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J7=3-4	ARLIN		Inv	1
2	950-0001-000	BAG STATIC BARRIER 07-0610	BAG ANTISTATIC 6X10 SC420610	ARLIN		Inv	1
2	910-0024-000	LABEL, STATIC SENSITIVE 130-02	APPLY TO ANTI-STATIC BAG TO SEAL	ARLIN		Inv	1

REPORT RECAP

0 WARNING(S) * Indicates no BOM Found for Item
0 ERROR(S)

REPORT PARAMETERS

ASSEMBLY RANGE : LPM-OPTO48 to LPM-OPTO48
TYPE : RWF

COMPONENT RANGE : <FIRST> to <LAST>
TYPE : RWF

MASKING : Inv-Explode Specific Inv Items (No Masks)

QUANTITY (TO EXPLODE): 1

DESC LENGTH: ITEM : 32
COMMENT : 40
LOCATION: 0
OVERHEAD: 0

NESTING INDENT LENGTH: 20

TOTAL REPORT WIDTH : 132

Telephone: 817-274-7553 • Fax: 817-548-1358
http://www.winsystems.com • E-mail: info@winsystems.com

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WARRANTY SERVICE

All products returned to WinSystems must be assigned a Return Material Authorization (RMA) number. To obtain this number, please call or FAX WinSystems' factory in Arlington, Texas and provide the following information:

1. Description and quantity of the product(s) to be returned including its serial number.
2. Reason for the return.
3. Invoice number and date of purchase (if available), and original purchase order number.
4. Name, address, telephone and FAX number of the person making the request.
5. Do not debit WinSystems for the repair. WinSystems does not authorize debits.

After the RMA number is issued, please return the products promptly. Make sure the RMA number is visible on the outside of the shipping package.

The customer must send the product freight prepaid and insured. The product must be enclosed in an anti-static bag to protect it from damage caused by static electricity. Each bag must be completely sealed. Packing material must separate each unit returned and placed as a cushion between the unit(s) and the sides and top of the shipping container. WinSystems is not responsible for any damage to the product due to inadequate packaging or static electricity.