OPERATIONS MANUAL
LPM/MCM-MDVGA

REVISION HISTORY

P/N 403-0258-000

ECO Number	Date Code	Rev Level
ORIGINATED	970613	C
01-29	010518	C1

TABLE OF CONTENTS

1 General Information

1.1 Features

- 16-Bit STD-BUS CRT/Flat Panel VGA Controller
- Uses the CHIPS™ 65545 High Performance Video Controller
- Supports CRT outputs of up to 1024 X 768 with 256 colors
- Supports Flat Panel resolutions up to 1024 X 768
- High-Performance zero wait-state writes
- Supports Tru-Color and Hi-Color displays of up to 640 X 480
- Optional Multi-Video Support
- SMARTMAP intelligent color to gray scale conversion
- Fully IBM VGA compatible
- Optional FPA adapter modules for Flat Panel use

1.2 General Description

The MD-VGA is a third generation CRT/Flat Panel controller board. It supports standard VGA output to a CRT monitor as well as to a variety of flat panel displays using optional Flat Panel Adapter (FPA) modules. Optional support for Multi-Video display is also available. The MDVGA uses the Chips and Technologies 6554X series of high-performance VGA controllers. This CHIPS™ controller supports standard and Super-VGA modes as well as Color and Monochrome panels with 8,9,12,15,16,18, and 24-bit interfaces. WinSystems provides flat panel support for the MDVGA through a series of FPA (Flat Panel Adapter) modules. Contact your WinSystems Applications Engineer for the most current list of available FPAs and supported panels.

1.3 Specifications

1.3.1 Electrical

Bus Interface :	STD-BUS 16-Bit interface
VCC :	+5V +/-5% @ 300mA typical w/CRT output and 512KB video RAM
VCC1	+12V +/-5% FPA Modules only
VCC2 :	-12V +/-5% FPA Modules only

1.3.2 Mechanical

Dimensions :	4.5" X 6.5" X 0.6"
PC Board :	FR4 Epoxy Glass with 2 signal layers and 2 power planes with screened component legend, plated through holes, and gold plated fingers.
Jumpers :	0.025" square posts on 0.10" centers
Connectors :	CRT : DB15F or 10 pin RN type IDH-10-LP
	Panel Interface : 50 pin RN type IDH-50-LP

1.3.3 Environmental

Operating Temperature : 0° to 70° C MCM-MDVGA

-40° to +85° C LPM-MDVGA

Non-condensing relative humidity : 5% to 95%

2 LPM/MCM-MDVGA Technical Reference

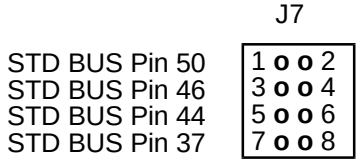
2.1 Introduction

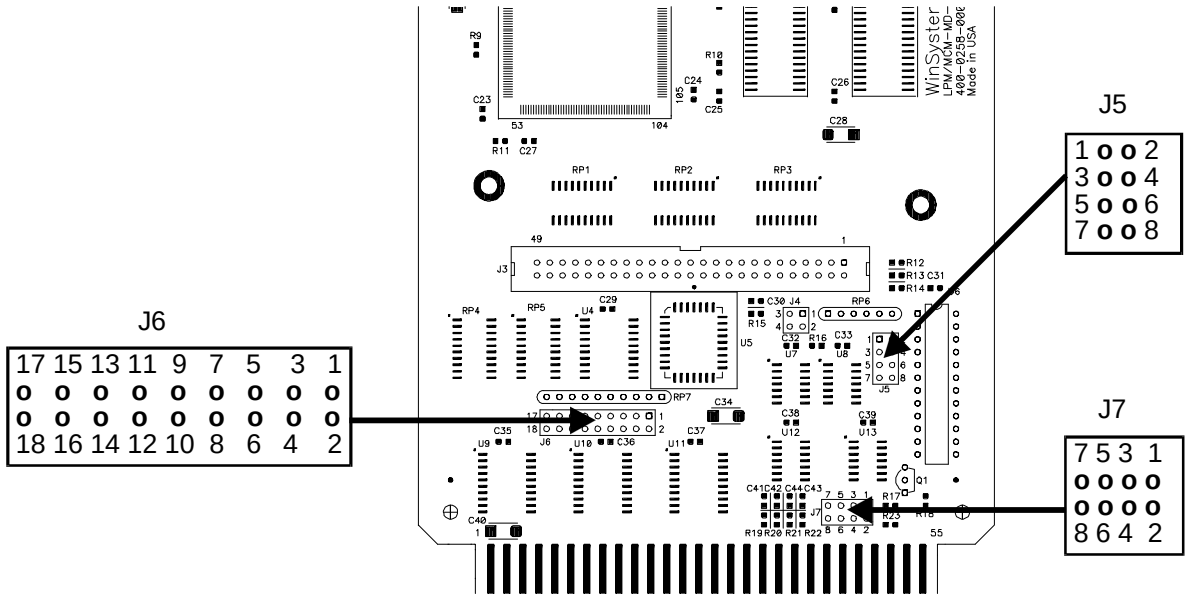
The MDVGA is a fully IBM compatible display module capable of CRT or Flat Panel output. Optional FPA (Flat Panel Adapter) modules allow for easy interfacing to a variety of color and monochrome Flat Panel displays. Details regarding interfacing to specific Flat Panels is not provided in this manual but should be referenced in the documentation accompanying the FPA module. Attempted connection to any flat panel not directly supported by a WinSystems FPA module is at the user's risk and extreme care should be exercised to avoid damaging or destroying the panel. To request assistance with the MDVGA or the WinSystems FPA, modules contact the Technical Support Group at (817) 274-7553 between 8AM and 5PM Central Time.

Hazard Warning : LCD panels can require a high voltage for the panel backlight. This high-frequency voltage can exceed 1000 volts and can present a shock hazard. To avoid danger of shock and to avoid damaging fragile and expensive panels, make all connection changes with the power removed.

2.2 Interrupt Routing

To maintain compatibility with older EGA software, a retrace interrupt is available by placing a jumper on J7. J7 allows for the selection of any of 4 STD-BUS backplane pins over which the retrace interrupt can be routed. The MDVGA is shipped from the factory with no jumper on J7 which is compatible with all modern VGA modes.





2.3 Multi-Video Configuration

When the multi-video option is populated, up to 15 MDVGA boards may be simultaneously installed and individually controlled by software. The I/O address of the board select register is controlled by jumper block J6. All boards installed in the same system must be set to the same I/O address. The address is selected as shown below :

Jumper present = 0
Jumper absent = 1

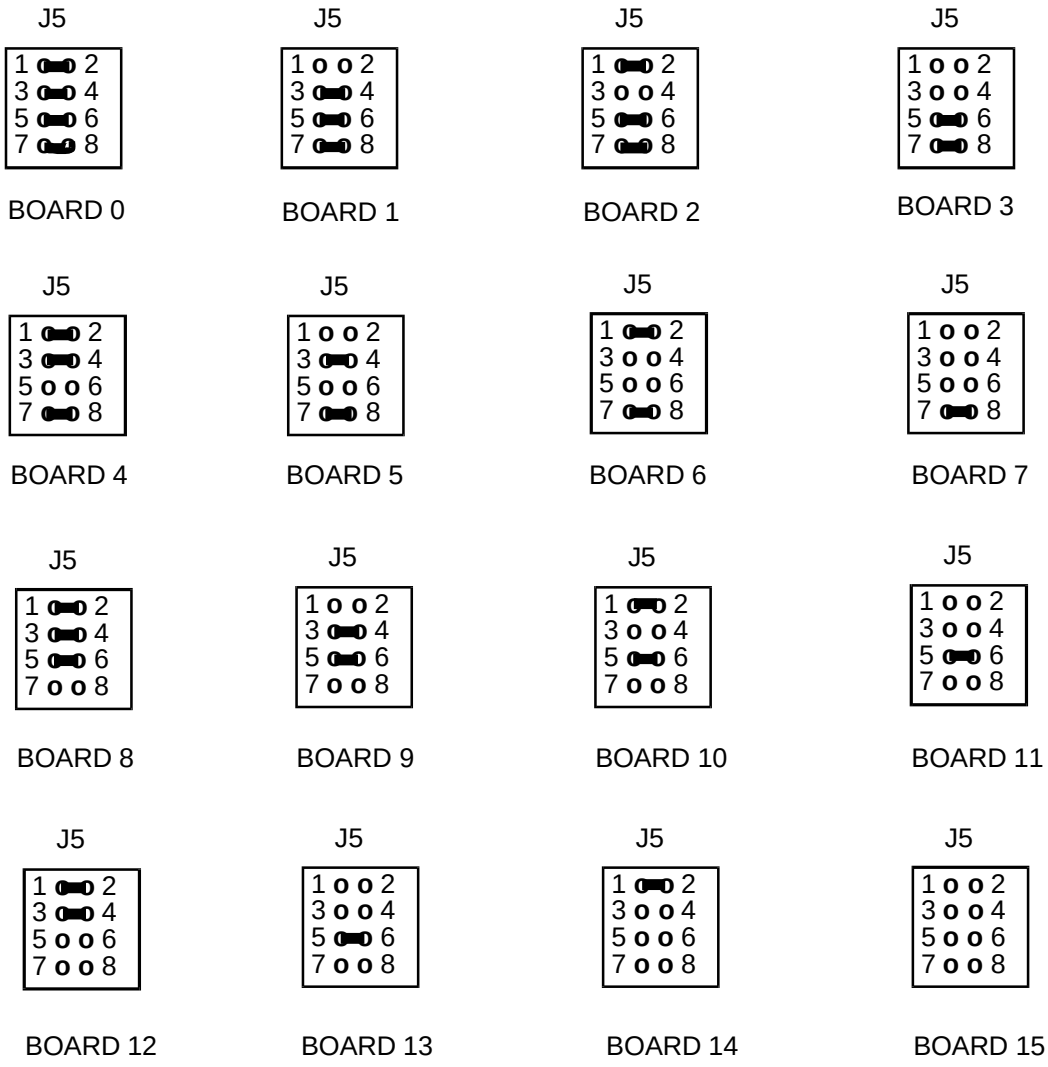
J6

ENABLE	1 2
A2	3 4
A3	5 6
A4	7 8
A5	9 10
A6	11 12
A7	13 14
A8	15 16
A9	17 18

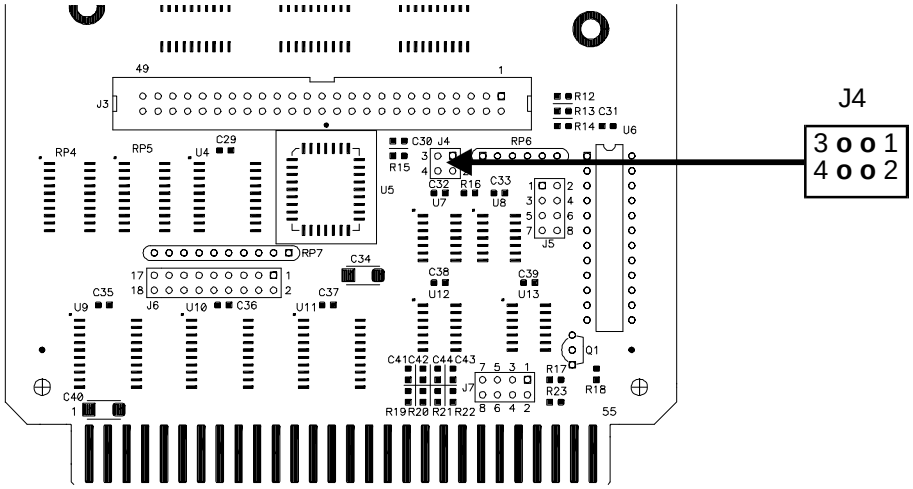
Sample Jumpering for
I/O Address 280H

2.3.1 Board ID Select

Up to 15 boards can be installed in a single system. Each board must be jumpered with a unique board ID number between 1 and 15. This board ID is selected with the jumper block at J5. When using only a single board, select board number 1 and remove the enable jumper at pins 1-2 of J6. When multiple boards are used, ID numbers must be assigned beginning with 1, and preceding sequentially. The jumpering detail for J5 is shown below :

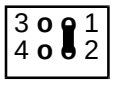


2.4 BIOS ROM Type Selection



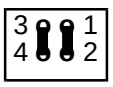
The MDVGA comes standard with a video BIOS expansion ROM populated at U5. Various ROM sizes can be used to support a variety of flat panel configurations each needing its own BIOS image. The FPA modules automatically select the correct BIOS image for the Panel family when the FPA is installed onto J3. The factory will ordinarily configure the BIOS ROM select jumper(s) for the BIOS ROM size provided. The jumpering details for J4 are shown here :

J4



128K 27C010
256K 27C020
512K 27C040

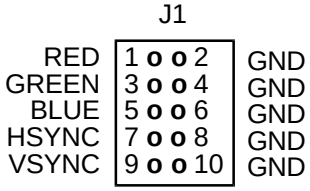
J4

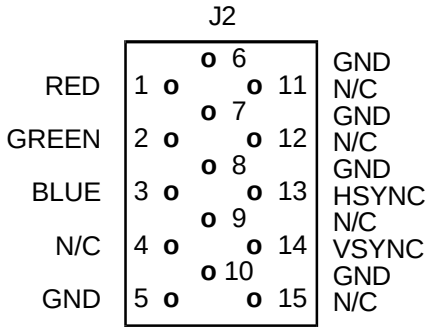


1M 27C080

2.5 CRT output connection

The MDVGA supports connection to standard VGA monitors through connectors at both J1 and J2. J1 is a dual-row 10-pin header to which the WinSystems adapter cable P/N CBL-207-1 may be attached. This allows for remote mounting of the CRT connector. Also provided is J2 is a standard DB15 VGA connector, for direct attachment of a VGA monitor. The pin definitions for J1 and J2 are shown here :





2.6 Flat Panel Output Connection

Connection to all flat panels is made via the 50-pin connector at J3. This connector is cabled to the appropriate FPA (Flat Panel Adapter) module which then breaks out the necessary cabling for attachment to the panel itself. The FPA module also supplies any special controls that may be needed for the panel. Refer to the FPA documentation for specific hook-up instructions. The pin definitions for the J3 connector are shown here.

J3

SW0	1 o o 2	SW1
SW2	3 o o 4	SW3
P23	5 o o 6	P22
P21	7 o o 8	P20
P19	9 o o 10	P18
GND	11 o o 12	GND
P17	13 o o 14	P16
P15	15 o o 16	P14
P13	17 o o 18	P12
GND	19 o o 20	GND
P11	21 o o 22	P10
P9	23 o o 24	P8
P7	25 o o 26	P6
GND	27 o o 28	GND
P5	29 o o 30	P4
P3	31 o o 32	P2
P1	33 o o 34	P0
GND	35 o o 36	GND
SHFCLK	37 o o 38	LP
FLM	39 o o 40	M
ENVCC	41 o o 42	ENBKL
ENVEE	43 o o 44	PHS
PVS	45 o o 46	-12V
+12V	47 o o 48	+12V
VCC	49 o o 50	VCC

2.7 Video Mode Tables

The MD-VGA supports a number of standard and extended VGA modes. The following tables extracted from the CHIPS 65540/65545 databook shows the video modes along with the required amount of RAM.

Standard Video Modes - VGA Standard

Mode # (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Resolution	Dot Clock (MHz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)	Video Memory	CRT CODE
0+, 1+	Text	16	40 X 25 40 X 25 40 X 25	9 X 16 8 X 14 8 X 8	360 X 400 320 X 350 320 X 200	28.322 25.175 25.175	31.5	70	256KB	A,B,C
2+, 3+	Text	16	80 X 25 80 X 25 80 X 25	9 X 16 8 X 14 8 X 8	720 X 400 640 X 350 620 X 200	28.322 25.175 25.175	31.5	70	256KB	A,B,C
4	Graphics	4	40 X 25	8 X 8	320 X 200	25.175	31.5	70	256KB	A,B,C
5	Graphics	4	40 X 25	8 X 8	320 X 200	25.175	31.5	70	256KB	A,B,C
6	Graphics	2	80 X 25	8 X 8	640 X 200	25.175	31.5	70	256KB	A,B,C
7+	Text	Mono	80 X 25 80 X 25 80 X 25	9 X 16 9 X 14 9 X 8	720 X 400 720 X 350 720 X 350	28.322	31.5	70	256KB	A,B,C
D	Planar	16	40 X 25	8 X 8	320 X 200	25.175	31.5	70	256KB	A,B,C
E	Planar	16	80 X 25	8 X 8	640 X 200	25.175	31.5	70	256KB	A,B,C
F	Planar	Mono	80 X 25	8 X 14	640 X 350	25.175	31.5	70	256KB	A,B,C
10	Planar	16	80 X 25	8 X 14	640 X 350	25.175	31.5	70	256KB	A,B,C
11	Planar	2	80 X 30	8 X 16	640 X 480	25.175	31.5	60	256KB	A,B,C
12	Planar	16	80 X 30	8 X 16	640 X 480	25.175	31.5	60	256KB	A,B,C
13	Packed Pixel	256	40 X 25	8 X 8	320 X 200	25.175	31.5	70	256KB	A,B,C

CRT Codes

A - PS/2 Fixed-frequency analog CRT or equivalent (31.5/35.5 Khz Horizontal Frequency Specification)
B - Multi-Frequency CRT Monitor (37.5 Khz minimum Horizontal Frequency Specification) (NEC MultiSync 3D or equivalent)
C - Multi-Frequency High-Performance CRT Monitor (48.5 KHZ minimum Horizontal Frequency Specification) MultiSyc 5D or equivalent

Extended Resolution Modes

Mode # (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Resolution	Dot Clock (MHz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)	Video Memory	CRT CODE
20	4-Bit Linear	16	80 X 30	8 X 16	640 X 480	25.175	31.5	60	512KB	A,B,C
22	4-Bit Linear	16	100 X 37	8 X 16	800 X 600	40.00	37.5	60	512KB	B,C
24	4-Bit Linear	16	128 X 48	8 X 16	1024 X 768	65.00	48.5	60	512KB	C
24I						44.90	35.5	43	512KB	B,C
30	8-Bit Linear	256	80 X 30	8 X 16	640 X 480	25.175	31.5	60	512K	A,B,C
32	8-Bit Linear	256	100 X 37	8 X 16	800 X 600	40.00	37.5	60	512KB	B,C
34	8-Bit Linear	256	128 X 48	8 X 16	1024 X 768	65.00	48.5	60	1MB	C
34I						44.90	35.5	43	1MB	B,C
40	16-Bit Linear	32K	80 X 30	8 X 16	640 X 480	50.350	31.5	60	1MB	A,B,C
41	16-Bit Linear	64K	80 X 30	8 X 16	640 X 480	50.350	31.5	60	1MB	A,B,C
50	24-Bit Linear	16M	80 X 30	8 X 16	640 X 480	65.00	27.1	51.6	1MB	B.C
60	Text	16	132 X 25	8 X 16	1056 X 400	40.00	30.5	68	256KB	A,B,C
61	Text	16	132 X 50	8 X 16	1056 X 400	40.00	30.5	68	256KB	A,B,C
6A,70	Planar	16	100 X 37	8 X 16	800 X 600	40.00	38.0	60	256KB	B,C
72,75	Planar	16	128 X 48	8 X 16	1024 X 768	65.00	48.5	60	512KB	C
72,75I						44.90	35.5	43	512KB	B,C
78	Packed Pixel	16	80 X 25	8 X 16	640 X 400	25.175	31.5	70	256KB	A,B,C
79	Packed Pixel	256	80 X 30	8 X 16	640 X 480	25.175	31.5	60	512KB	A,B,C
7C	Packed Pixel	256	100 X 37	8 X 16	800 X 600	40.00	37.5	60	512KB	B,C
7E	Packed Pixel	256	128 X 48	8 X 16	1024 X 768	65.00	48.5	60	1MB	C
7EI	Packed Pixel					44.90	35.5	43	1MB	B,C

Support for the modes above is included directly in the BIOS. The 'I' in the mode # column indicates "interlaced"

CRT Codes

A - PS/2 Fixed frequency analog CRT or equivalent (31.5/35.5 Khz Horizontal Frequency Specification)
B - Multi-Frequency CRT Monitor (37.5 Khz minimum Horizontal Frequency Specification) (NEC MultiSync 3D or equivalent)
C - Multi-Frequency High-Performance CRT Monitor (48.5 KHZ minimum Horizontal Frequency Specification) MultiSyc 5D or equivalent

High Refresh Modes

Mode # (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Resolution	Dot Clock (MHz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)	Video Memory	CRT CODE
12	Planar	16	80 X 30	8 X 16	640 X 480	31.50	37.5	75	256KB	B,C
30	8-Bit Linear	256	80 X 30	8 X 16	640 X 480	31.50	37.5	75	256KB	C
79	Packed Pixel	256	80 X 30	8 X 16	640 X 480	31.50	37.5	75	512KB	C
6A,70	Planar	16	100 X 37	8 X 16	800 X 600	49.50	46.9	75	512KB	C
32	8-Bit Linear	256	100 X 37	8 X 16	800 X 600	49.50	46.9	75	1MB	C
7C	Packed Pixel	256	100 X 37	8 X 16	800 X 600	49.50	46.9	75	1MB	C

Support for the modes above is included directly in the BIOS. The 'I' in the mode # column indicates "interlaced"

CRT Codes

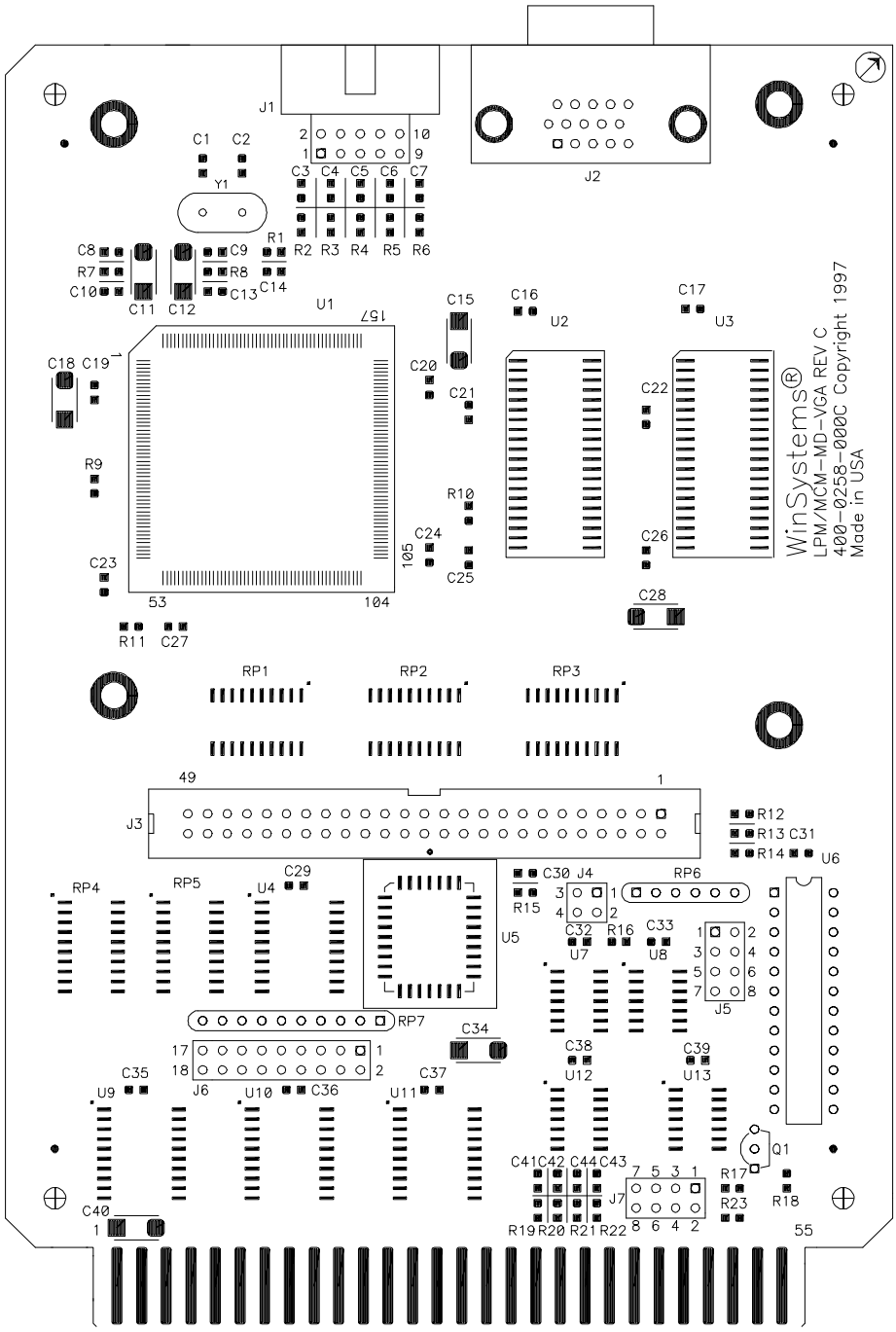
A - PS/2 Fixed frequency analog CRT or equivalent (31.5/35.5 Khz Horizontal Frequency Specification)
B - Multi-Frequency CRT Monitor (37.5 Khz minimum Horizontal Frequency Specification) (NEC MultiSync 3D or equivalent)
C - Multi-Frequency High-Performance CRT Monitor (48.5 KHZ minimum Horizontal Frequency Specification) MultiSyc 5D or equivalent

2.8 Connector/Jumper Summary

Connector/ Jumper	Description	Page Reference
J1	VGA output connector	2-5
J2	VGA output connector	2-5
J3	FPA-50 Panel Interface connector	2-6
J4	BIOS Size select jumper	2-4
J5	Board ID select jumper	2-3
J6	I/O Address select jumper	2-2
J7	Interrupt Routing select jumper	2-1

3 APPENDIX A

LPM/MCM-MDVGA Parts Placement Guide



4 APPENDIX B

LPM/MCM-MDVGA Parts List

ASSM ITEM FROM: LPM-MDVGA-1M ASSM ITEM THRU: LPM-MDVGA-1M
PARENT LOC FROM: <FIRST> DEFAULT COMPONENT LOCATION: ARLIN PARENT LOC THRU: <LAST>

LVL	ITEM KEY	ITEM DESCRIPTION	BOM COMMENT		ITEM TYPE	QTY REQUIRED
LPM-MDVGA-1M		CMOS STD BUS MULTIDISPLAY SVGA	CMOS STD BUS MULTIDISPLAY SVGA	CO	F	1.0
1	999-9999-001	SPECIAL NOTES	06-30-97 MEB (NEW-REV.C)		I	1.0
1	0258-130-0000C	ASSY MDVGA-1M REV.C			F	1.0
2	999-9999-001	SPECIAL NOTES	11-24-97 MEB ECO 97-114		I	1.0
2	999-9999-001	SPECIAL NOTES	05-08-97 MEB (REVC)		I	1.0
2	603-2207-403	CAP 22pF 50v 1% NPO 0805	C1-C7		I	7.0
2	603-1047-803	CAP .1uF 50v 20% CER 0805	C8-C10,C13,C14,C16,C17,C19-C27,C29-C33,		I	26.0
2	999-9999-001	SPECIAL NOTES	C35-C39		I	1.0
2	603-1065-82D	CAP 10uF 25v 20% TAN 6032	C11,C12,C15,C18,C28,C34,C40		I	7.0
2	603-4707-803	CAP 47pF 50v 20% CER 0805	C42-C44		I	3.0
2	201-0010-121	HDR 10 RA IDH-10LP-SR3-TR (1,200)	J1		I	1.0
2	201-0015-300	CON PC MT FE 15 MCRO D 302-122-106A I/OI	J2		I	1.0
2	201-0050-021	HDR 50 ST IDH-50LP-S3-TR (504)	J3		I	1.0
2	201-0072-120	HDR 2X36 UN TSW-136-07-G-D	J4=2X2 J7=2X4		I	.2
2	125-0001-000	TRANSISTOR PN2222 (TO92)	Q1		I	1.0
2	602-0220-523	RN 22 Oh, 5%, 20P, 10R, ISO	RP1-RP5		I	5.0
2	601-0103-503	RES 10K Ohm 5% 1/10W 0805	R1,R9,R12,R13-R16		I	7.0
2	601-0151-503	RES 150 Ohm 5% 1/10w 0805	R2-R4		I	3.0
2	601-0220-503	RES 22 Ohm 5% 1/10w 0805	R5,R6		I	2.0
2	601-0100-503	RES 10 Ohm 5% 1/10w 0805	R7,R8		I	2.0
2	601-0472-503	RES 4.7K Ohm 5% 1/10w 0805	R10		I	1.0
2	601-2670-303	RES 267 Ohm 1% 1/10w 0805	R11		I	1.0
2	601-0102-503	RES 1K Ohm 5% 1/10W 0805	R17,R18		I	2.0
2	601-0101-503	RES 100 Ohm 5% 1/10w 0805	R19-R22		I	4.0
2	601-0000-503	RES 0 Ohm 5% 1/10w 0805	R23		I	1.0
2	621-0011-016	IC, C&T F65545/B2-5 (24)	U1		I	1.0
2	631-0002-008	256k X 16 DRAM 70n	U2,U3		I	2.0
2	612-0245-002	IC, 74HCT245DW (SM)	U4		I	1.0
2	650-0032-002	SOCKET 32P AMP 822498-1 (28)	U5		I	1.0
2	612-0008-001	IC, 74HCT08 (SM)	U7		I	1.0
2	612-0004-001	IC, 74HCT04	U8		I	1.0
2	612-0373-002	IC, 74HCT373 (SM)	U9,U11		I	2.0
2	612-0074-001	IC, 74HCT74 (SM)	U12		I	1.0
2	612-0032-001	IC, 74HCT32	U13		I	1.0
2	220-0000-000	HC49 INSULATOR XTAL	Y1-INSTALL BEFORE XTAL		I	1.0
2	220-0032-001	XTAL-14.31818 (ABRACON) ABL-14.31818	Y1		I	1.0
2	400-0258-000C	PCB, MD-VGA REV.C			I	1.0
SUB-ASSEMBLY TOTAL: 0258-130-0000C		ARLIN - 34 Items				
1	0258-310-0000C	SUB ASSY MDVGA REV.C			F	1.0
2	999-9999-001	SPECIAL NOTES	05-08-97 MEB (NEW REVC)		I	1.0
2	201-0002-000	PLUG JUMPER 999-19-310-00-000000	J4=1-2		I	1.0
2	999-9999-001	SPECIAL NOTES	J7=OPEN		I	1.0
2	634-0002-015	IC, AT27C040-15JC [SM] (15)	U5 CS=4B00 \MDVGA\REL1218.BIN		I	1.0
2	500-0001-000	EJECTOR SCANBE S208-1 (W/O Roll pin)	STAMP: RED-MCM/BLUE-LPM 'MD-VGA'		I	1.0

ASSM ITEM FROM: LPM-MDVGA-1M ASSM ITEM THRU: LPM-MDVGA-1M
PARENT LOC FROM: <FIRST> DEFAULT COMPONENT LOCATION: ARLIN PARENT LOC THRU: <LAST>

LVL	ITEM KEY	ITEM DESCRIPTION	BOM COMMENT	ITEM TYPE	QTY REQUIRED
2	500-0002-000	ROLL PIN MS171492	ROLL PIN MS171492	I	1.0
SUB-ASSEMBLY TOTAL: 0258-310-0000C		ARLIN - 6 Items			
TOP ASSEMBLY TOTAL: LPM-MDVGA-1M		ARLIN - 3 Items			

REPORT RECAP

0 WARNING(S)

PARAMETER RECAP

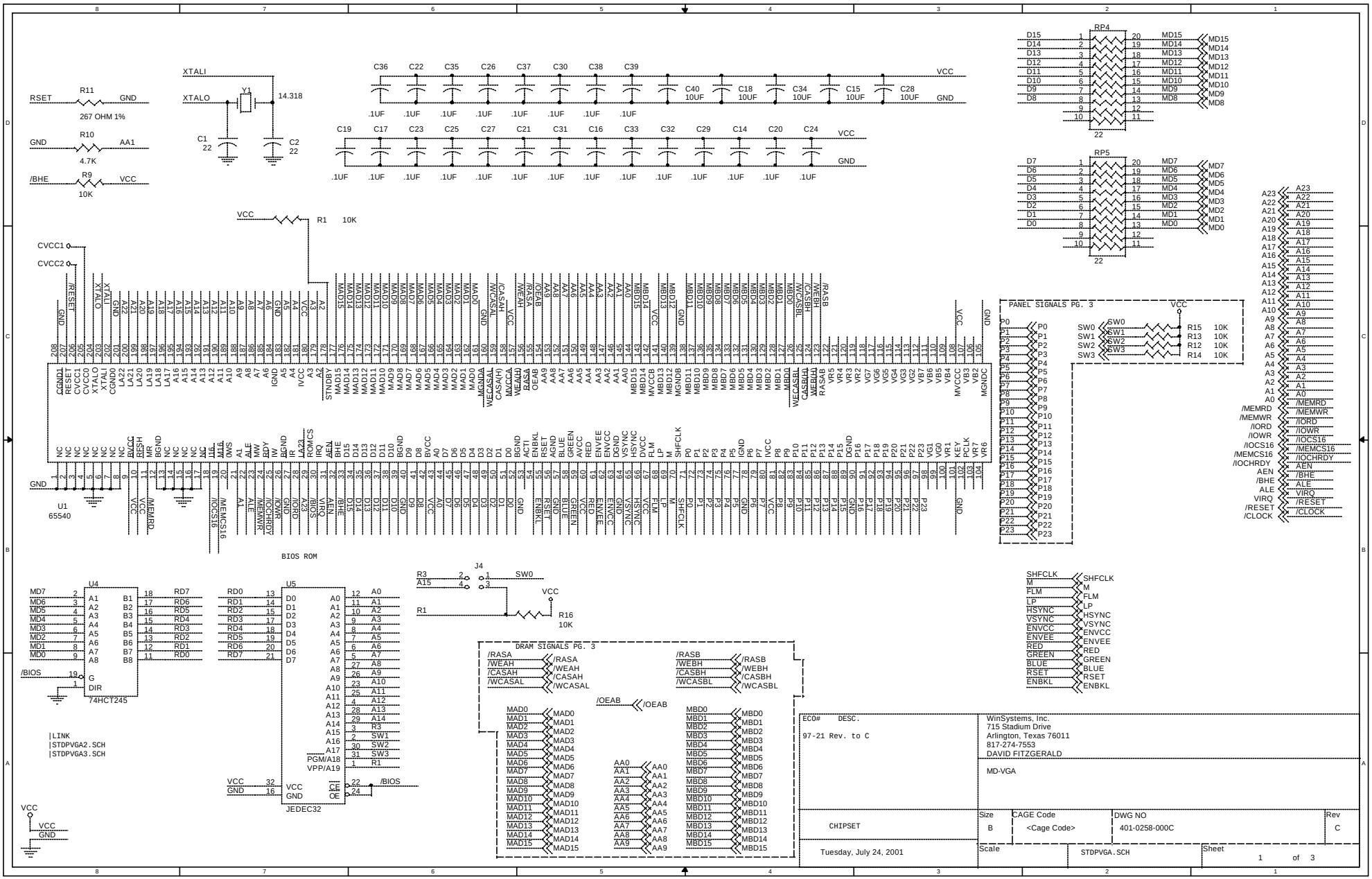
PARAMETER KEY : 10 BOM with Ref. Desc.
REPORT TITLE : BOM for Manuals

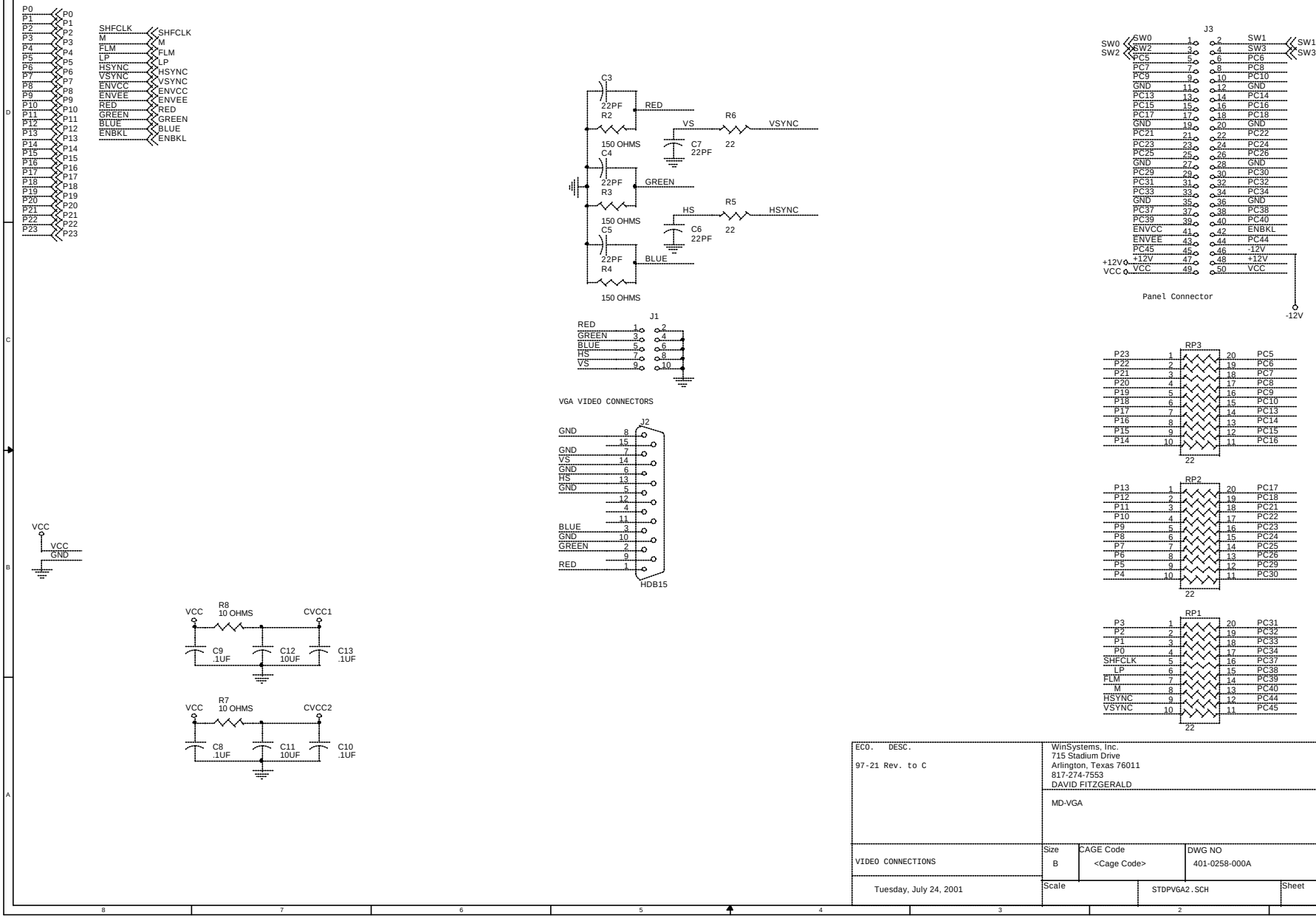
ASSM ITEM RANGE : LPM-MDVGA-1M THRU LPM-MDVGA-1M
PARENT LOC RANGE : <FIRST> THRU <LAST>
PRODUCT KEY RANGE : <FIRST> THRU <LAST>
COMMODITY KEY RANGE : <FIRST> THRU <LAST>
DEFAULT COMP LOC : ARLIN
BOM STATUS PRIORITY : A

COSTING METHOD : A
QUANTITY TO EXPLODE : 1
USE SCRAP FACTOR (Y/N) : N
UPDATE INV STD COST : N
NO. LEVELS TO EXPLODE : 999
COLUMNS OF DESC TEXT : 42
SHORT OR LONG (S/L) : S
PRINT ITEM DESC (Y/N) : Y

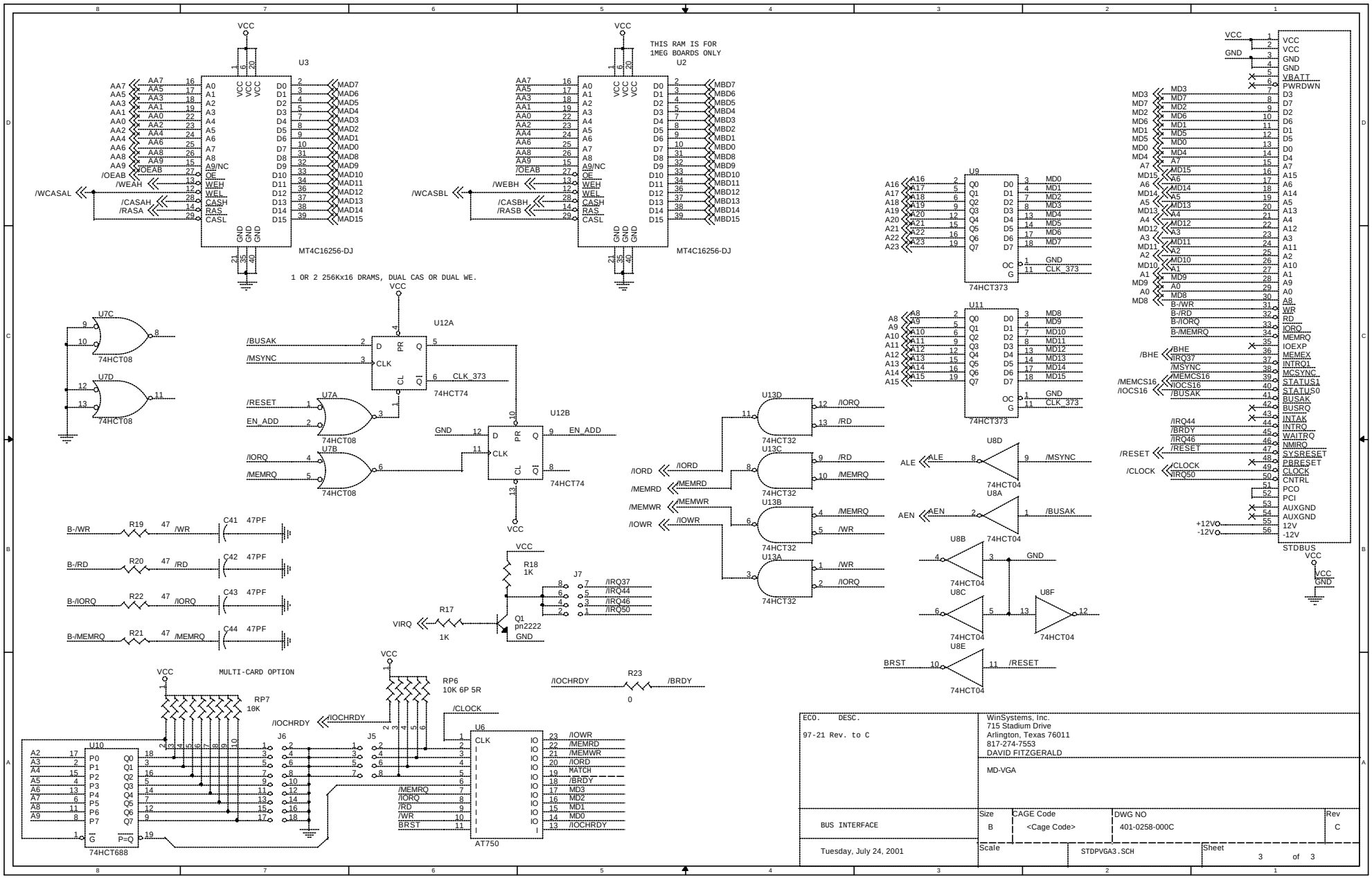
5 APPENDIX C

LPM/MCM-MDVGA Schematic Diagrams


RSET
R11
GND
267 OHM 1%
GND
R10
AA1
4.7K
/BHE
R9
VCC
10K
XTALI
XTALO
Y1
14.318
C1
22
C2
22
C36 C22 C35 C26 C37 C30 C38 C39
.1UF .1UF .1UF .1UF .1UF .1UF .1UF .1UF
C40 10UF
C18 10UF
C34 10UF
C15 10UF
C28 10UF
VCC
GND
C19 C17 C23 C25 C27 C21 C31 C16 C33 C32 C29 C14 C20 C24
.1UF .1UF .1UF .1UF .1UF .1UF .1UF .1UF .1UF .1UF .1UF .1UF .1UF .1UF
VCC
GND
RP4
RP5
22
R1 10K
CVCC1
CVCC2
U1
65540
BIOS ROM
PANEL SIGNALS PG. 3
SW0
SW1
SW2
SW3
R15 10K
R13 10K
R12 10K
R14 10K
U4
74HCT245
U5
JEDEC32
/BIOS
DIR
PGM/A18
VPP/A19
R3
R1
R16
10K
J4
|LINK
|STDPVGA2.SCH
|STDPVGA3.SCH
DRAM SIGNALS PG. 3
/RASA
/WEAH
/CASAH
/WCASAL
/RASB
/WEBH
/CASBH
/WCASBL
/OEAB
MAD0
MAD1
MAD2
MAD3
MAD4
MAD5
MAD6
MAD7
MAD8
MAD9
MAD10
MAD11
MAD12
MAD13
MAD14
MAD15
AA0
AA1
AA2
AA3
AA4
AA5
AA6
AA7
AA8
AA9
MBD0
MBD1
MBD2
MBD3
MBD4
MBD5
MBD6
MBD7
MBD8
MBD9
MBD10
MBD11
MBD12
MBD13
MBD14
MBD15
SHFCLK
M
FLM
LP
HSYNC
VSYNC
ENVCC
ENVEE
RED
GREEN
BLUE
RSET
ENBKL
ECO# DESC.
97-21 Rev. to C
WinSystems, Inc.
715 Stadium Drive
Arlington, Texas 76011
817-274-7553
DAVID FITZGERALD
MD-VGA
CHIPSET
Tuesday, July 24, 2001
Size B
CAGE Code <Cage Code>
DWG NO 401-0258-000C
Rev C
Scale
STDPVGA.SCH
Sheet 1 of 3



ECO. DESC. 97-21 Rev. to C	WinSystems, Inc. 715 Stadium Drive Arlington, Texas 76011 817-274-7553 DAVID FITZGERALD			
	MD-VGA			
VIDEO CONNECTIONS	Size: B	CAGE Code: <Cage Code>	DWG NO: 401-0258-000A	Rev: A
Tuesday, July 24, 2001	Scale:	STDPVGA2.SCH	Sheet: 2 of 3	


U3
MT4C16256-DJ
THIS RAM IS FOR
1MEG BOARDS ONLY
U2
MT4C16256-DJ
1 OR 2 256Kx16 DRAMS, DUAL CAS OR DUAL WE.
U9
74HCT373
U11
74HCT373
U7C
U7D
74HCT08
U12A
74HCT74
U12B
74HCT74
U7A
U7B
U13D
U13C
U13B
U13A
74HCT32
U8D
U8A
U8B
U8C
U8F
U8E
74HCT04
STDBUS
R18
1K
R17
1K
Q1
pn2222
J7
R19
R20
R22
R21
47
C41
C42
C43
C44
47PF
B-/WR
B-/RD
B-/IORQ
B-/MEMRQ
MULTI-CARD OPTION
RP7
10K
RP6
10K 6P 5R
R23
0
U10
74HCT688
J6
J5
U6
AT750
ECO. DESC.
97-21 Rev. to C
WinSystems, Inc.
715 Stadium Drive
Arlington, Texas 76011
817-274-7553
DAVID FITZGERALD
MD-VGA
BUS INTERFACE
Tuesday, July 24, 2001
Size B
CAGE Code <Cage Code>
DWG NO 401-0258-000C
Rev C
Scale
STDPVGA3.SCH
Sheet 3 of 3

Telephone: 817-274-7553 . . Fax: 817-548-1358
http://www.winsystems.com . . E-mail: info@winsystems.com

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All products returned to WinSystems must be assigned a Return Material Authorization (RMA) number. To obtain this number, please call or FAX WinSystems' factory in Arlington, Texas and provide the following information:

1. Description and quantity of the product(s) to be returned including its serial number.
2. Reason for the return.
3. Invoice number and date of purchase (if available), and original purchase order number.
4. Name, address, telephone and FAX number of the person making the request.
5. Do not debit WinSystems for the repair. WinSystems does not authorize debits.

After the RMA number is issued, please return the products promptly. Make sure the RMA number is visible on the outside of the shipping package.

The customer must send the product freight prepaid and insured. The product must be enclosed in an anti-static bag to protect it from damage caused by static electricity. Each bag must be completely sealed. Packing material must separate each unit returned and placed as a cushion between the unit(s) and the sides and top of the shipping container. WinSystems is not responsible for any damage to the product due to inadequate packaging or static electricity.