EPX-C380-S

Intel® ATOM™ EPIC Single Board Computer

PRODUCT MANUAL

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MANUAL REVISION HISTORY

P/N 400-0380-002

Revision Date Code	ECO Number
111219	Initial Release
120124	ECO 12-15
120307	
120507	
120703	
120815	
130304	
130723	
140206	ECO 14-06

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BEFORE YOU BEGIN

WinSystems offers best practice recommendations for using and handling WinSystems embedded PCs. These methods include valuable advice to provide an optimal user experience and to prevent damage to yourself and/or the product.

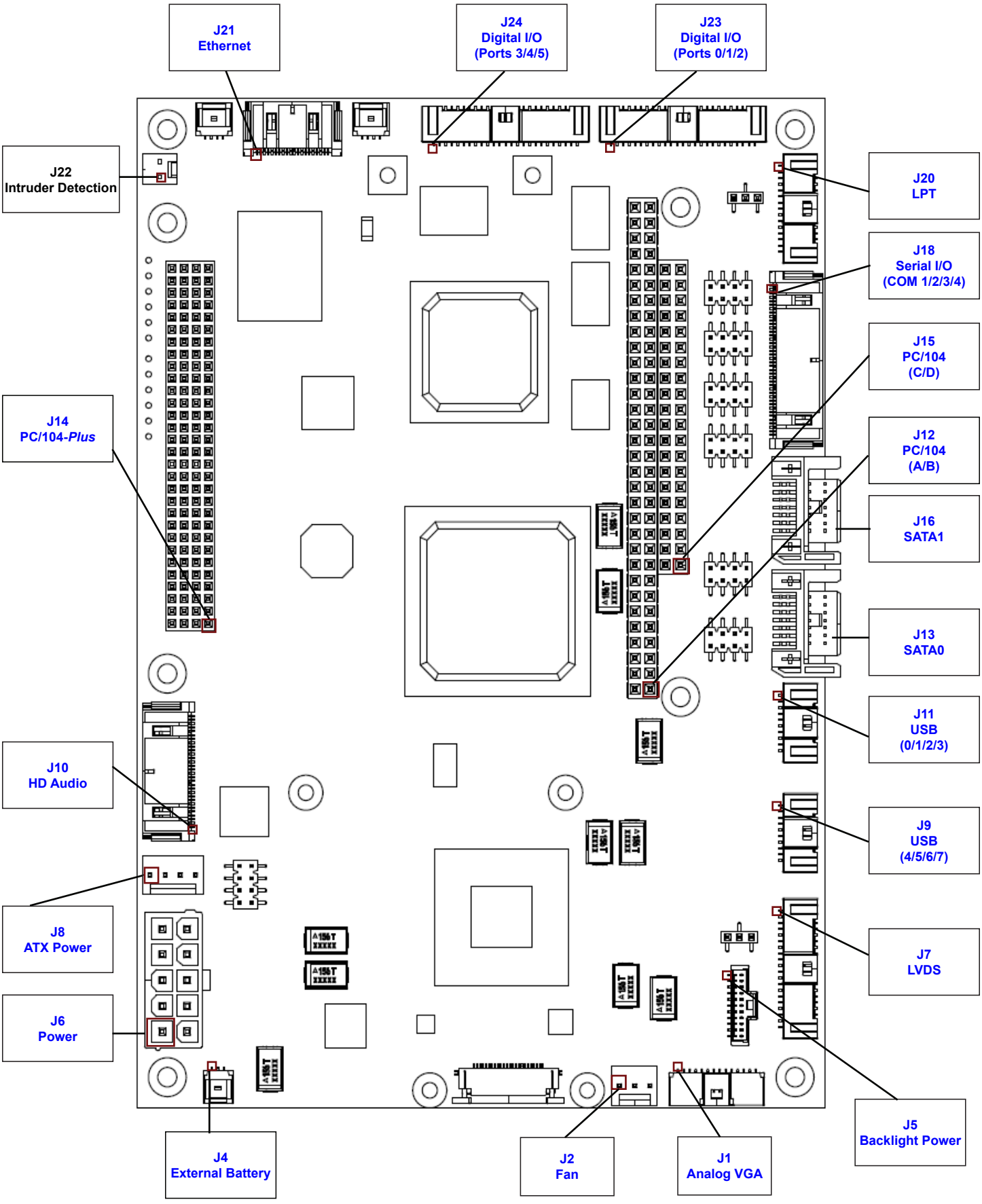
YOU MAY VOID YOUR WARRANTY AND/OR DAMAGE AN EMBEDDED PC BY FAILING TO COMPLY WITH THESE BEST PRACTICES.

Reference **Appendix - A** for **Best Practices**.

Please review these guidelines carefully and follow them to ensure you are successfully using your embedded PC.
This product ships with a heat sink. Product warranty is void if the heat sink is removed from the product.

For any questions you may have on WinSystems products, contact our Technical Support Group at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

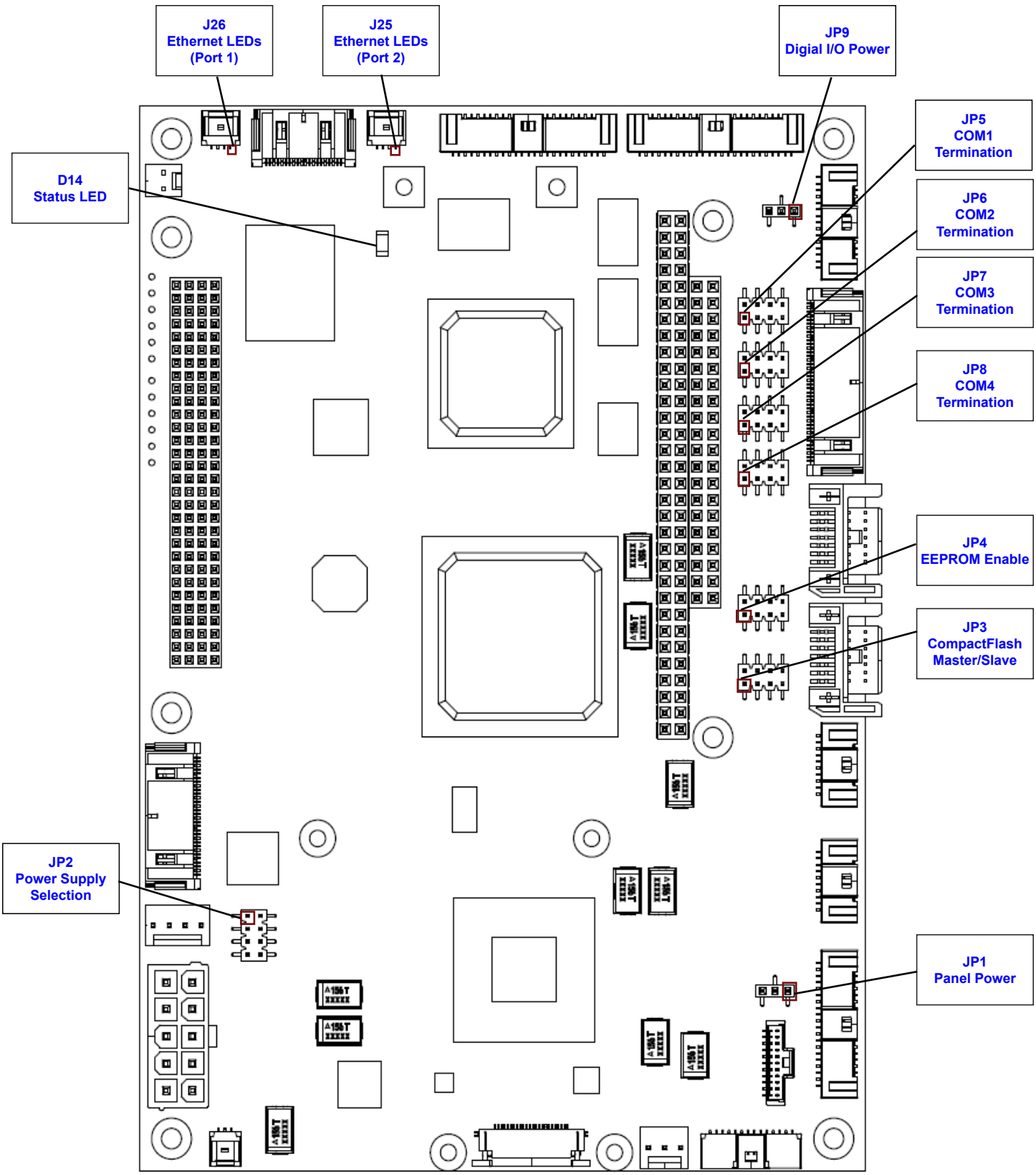
Visual Index - Top View (Connectors)



RESERVED - J3, J19, D12

NOTE: The reference line to each component part has been drawn to Pin 1, and is also highlighted with a square, where applicable.

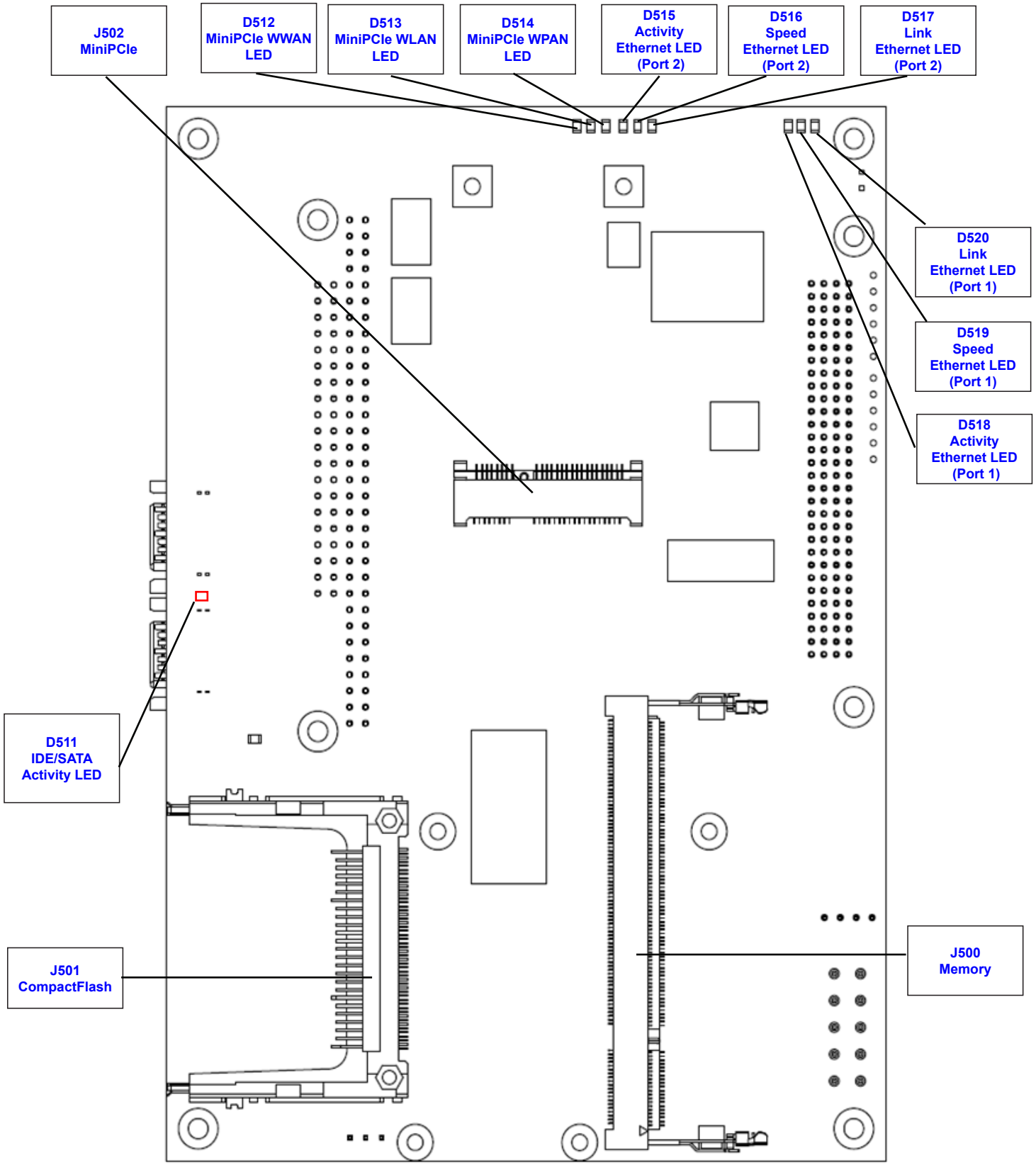
Visual Index - Top View (Jumpers & LEDs)



RESERVED - J3, J19, D12

NOTE: The reference line to each component part has been drawn to Pin 1, and is also highlighted with a square, where applicable.

Visual Index - Bottom View



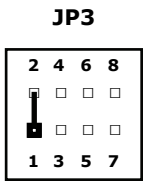
RESERVED - J3, J19, D12

NOTE: The reference line to each component part has been drawn to Pin 1, and is also highlighted with a square, where applicable.

Jumper Reference

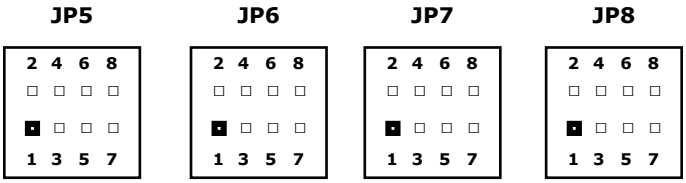
NOTE: Jumper Part# SAMTEC 2SN-BK-G is applicable to all jumpers. These are available in a ten piece kit from WinSystems (Part# KIT-JMP-G-200).

JP3 - CompactFlash / Solid State Disk / Ethernet



CompactFlash Master (default)	1-2
CompactFlash Slave	1 2
SSD Master	3-4
SSD Slave (default)	3 4
SSD Write Protect	5-6
SSD Program Enable (default)	5 6
Disable Ethernet Device 2	7-8
Enable Ethernet Device 2 (default)	7 8

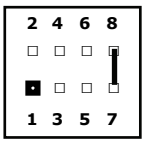
JP5 - COM1, JP6 - COM2, JP7 - COM3, JP8 - COM4



RS-422 Termination and Biasing Resistors		
TX (100): Places a 100Ω Resistor across the TX+/TX- pair		3-4
RX (100): Places a 100Ω Resistor across the RX+/RX- pair		7-8
TX(300):	Places a 100Ω Resistor from +5V to TX+	1-2
	Places a 100Ω Resistor between TX+ and TX-	3-4
	Places a 100Ω Resistor from Ground to TX-	5-6

RS-485 Termination and Biasing Resistors		
TX (100): Places a 100Ω Resistor across the TX/RX+/TX/RX- pair		3-4
TX/RX(300):	Places a 100Ω Resistor from +5V to TX/RX+	1-2
	Places a 100Ω Resistor between TX/RX+ and TX/RX-	3-4
	Places a 100Ω Resistor from Ground to TX/RX-	5-6

JP4 - EEPROM

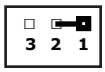


EEPROM Enable	
CMOS Register Reset (only in G3 power mode)	1-2
SPI BIOS Write Protect	3-4
SPI BIOS Program Enable	5-6
CMOS EEPROM Enable (default)	7-8
CMOS EEPROM Disable	7 8

Jumper Reference (cont'd)

JP1 - Panel Power

JP1

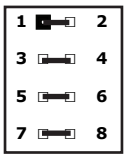


Avoid Simultaneous Jumpering of pins 1-2 and 2-3.
Misjumpering panel power causes damage to the board and/or the Flat Panel.

Panel Power	5V 3.3V (default)	2-3 1-2

JP2 - Power Supply Selection

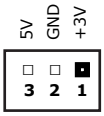
JP2



AT Power	1-2, 3-4, 5-6, 7-8 (default)
ATX Power	1 2, 3 4, 5 6, 7 8

JP9 - Digital I/O VCC

JP9



Avoid Simultaneous Jumpering of pins 1-2 and 2-3.
Misjumpering causes damage to the board.

+3.3V is provided at pin 49 of **J23/J24**	1-2
+5V is provided at pin 49 of **J23/J24**	2-3
No Power at Pin 49 of **J23/J24** (default)	OPEN

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INTRODUCTION

This manual is intended to provide the necessary information regarding configuration and usage of the EPX-C380 single board computer. WinSystems maintains a Technical Support Group to help answer questions not adequately addressed in this manual. Contact Technical Support at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

FEATURES

CPU
- Intel® ATOM™ N450 (1.66 GHz) single core or D510 (1.66 GHz) dual core

Compatible Operating Systems
- Linux, Windows, DOS, and other x86 compatible OS

Memory
- Up to 2 GB of DDR2 SODIMM (Socketed)

BIOS
- Phoenix

Video
- Analog VGA or Flat Panel (simultaneous operation supported)
- Analog VGA resolution up to SXGA 1400x1050
- Flat Panel resolution up to 1366x768 or 1280x800
- Up to 18-bits/pixel color panel support
- LVDS supported

Ethernet
- 2 Intel® 10/100/1000 Mbps controllers (one using PC82574 and one using ICH8M LAN)
  *Model EPX-C380-S1-0 includes one Ethernet controller for ICH8M.

Storage
- 2 SATA (2.0) channels
- 1 MB soldered-on SRAM with battery backup
- Optional 512 MB - 2 GB soldered-on flash SSD
- CompactFlash Types I and II memory socket supported

Digital I/O
- 48 GPIO Bidirectional lines (WS16C48)

Serial I/O
- 4 serial ports (RS-232/422/485) (2-RS232/422/285) (2-RS-232 for EPX-C380-S1-0).
  *RS-422/485 on COM3 and COM4 are not supported for model EPX-C380-S1-0.

Line Printer Port
- SPP/EPP supported

USB
- 8 USB 2.0 ports *USB(J11) is not applicable for model EPX-C380-S1-0.

Watchdog Timer
- Adjustable from 1 second to 255 minute reset

Audio
- HD Audio supported

Power
- +5V required, 2.5A typical

Bus Expansion
- PC/104
- PC/104-*Plus*
- MiniPCIe *MiniPCIe not applicable for model EPX-C380-S1-0.

Industrial Operating Temperature
- -40°C to 85°C

Mechanical
- EPIC-compliant
- Dimensions: 4.50” x 6.50” (115 mm x 165 mm)
- Weight: 9.6 oz (272.2g)

Additional Features
- RoHS compliant
- Backlight power supported
- Custom splash screen on start-up
- Real-time clock/calendar

System

The EPX-C380 is an Intel® ATOM™ Single Board Computer (SBC) which uses either a 1.66 GHz single core Intel N450 or 1.66 GHz dual core D510 processor paired with the ICH8M controller hub. This is an EPIC-compatible unit and incorporates two 10/100/1000 Mbps Ethernet controllers, two SATA channels, 48 lines of digital I/O, four serial RS-232/422/485 ports, watchdog timer, and LPT. The SBC also supports HD audio, USB ports, and is equipped with a CompactFlash socket and MiniPCIe card socket.

Memory

The EPX-C380 board supports up to 2 GB DDR2 SODIMM system memory via an on-board socket located at **J500**.

FUNCTIONALITY

I/O Port Map

Following is a list of I/O ports used on the EPX-C380.

NOTE: The EPX-C380 uses a PnP BIOS resource allocation. Care must be taken to avoid contention with resources allocated by the BIOS.

HEX Range	Usage
0000h-001Fh	DMA Controller 82C37
0020h-0021h	Interrupt Controller PIC 8259
0024h-0025h	Interrupt Controller
0028h-0029h	Interrupt Controller
002Ch-002Dh	Interrupt Controller
002Eh-002Fh	Forward to Super IO
0030h-0031h	Interrupt Controller
0034h-0035h	Interrupt Controller
0038h-0039h	Interrupt Controller
003Ch-003Dh	Interrupt Controller
0040h-0043h	Timer counter 8254
004Eh-004Fh	Forward to Super IO
0050h-0053h	Timer counter 8254
0060h	Keyboard data port
0061h	NMI controller
0062h	8051 download 4K address counter
0064h	Keyboard status port
0066h	8051 download 8-bit data port
0070h-0077h	RTC Controller
0080h-0091h	DMA Controller
0092h	Reset Generator
0093h-009Fh	DMA Controller
00A0h-00A1h	Interrupt Controller PIC 8259
00A4h-00A5h	Interrupt Controller
00A8h-00A9h	Interrupt Controller
0ACh-00ADh	Interrupt Controller
00B0h-00B1h	Interrupt Controller
00B2h-00B3h	Power Management
00B4h-00B5h	Interrupt Controller
00B8h-00B9h	Interrupt Controller
00C0h-00DFh	DMA Controller 82C37
00F0h	FERR#/IGNNE/Interrupt Controller
0120h-012Fh	Digital I/O (Default)
0140h-01FFh	Reserved *
0170h-0177h	IDE1 Controller
0180h-01FFh	Reserved
0210h-0213h	SRAM Control
0298h-029Bh	Reserved for Super I/O Configuration
029Ch	Interrupt Status Reigster
029Dh	Status LED Register
029Eh-029Fh	Watchdog Timer Control
02E8h-02EFh	COM4 (Default)
02F8h-02FFh	COM2 (Default)

HEX Range	Usage
0340h-03E7h	Reserved *
0376h	IDE1 Controller
0378h-037Bh	LPT (Default)
03E8h-03EFh	COM3 (Default)
03F0h-03F5h	Reserved
03F6h	IDE0 Controller
03F8h-03FFh	COM1 (Default)
04D0h-4D1h	Interrupt Controller
0564h-0568h	Advanced Watchdog
0CF9h	Reset Generator

This product utilizes a LPC to ISA Bridge to address the PC/104 bus. The majority of legacy PC/104 modules are I/O mapped and function as expected. However, neither DMA nor memory mapped PC/104 modules are supported with this product. The PC/104-*Plus* PCI signals are completely supported.

*** The ICH8M limits the LPC (ISA) decode ranges to four windows, two of which can be adjusted in the BIOS. For example, the 0300-033Fh range can be changed to 0600-06FFh so the full 256 bytes are available for PC/104 modules. Resources addressed internally may still exist in these ranges so please check the I/O map for availability.**

The advanced watchdog timer is the only on-board device affected by adjusting LPC (ISA) decode range. It will not be available if the 0564-0568h decode range is disabled.

The default is for the PC/104 decode ranges are shown below. Please contact an Applications Engineer if you have questions regarding the decode ranges.

0100-013Fh 64 Bytes (Fixed)

0200-02FFh 256 Bytes (Fixed)

0300-033Fh 64 Bytes (BIOS Selectable)

0500-05FFh 256 Bytes (BIOS Selectable)

Interrupt Map

Hardware Interrupts (IRQs) are supported for both PC/104 (ISA), PCI and PCIe devices. The user must reserve IRQs in the BIOS CMOS configuration for use by legacy devices. The PCIe/PnP BIOS will use unreserved IRQs when allocating resources during the boot process. The table below lists IRQ resources as used by the EPX-C380.

IRQ0	18.2 Hz heartbeat
IRQ1	Keyboard
IRQ2	Chained to Slave controller (IRQ9)
IRQ3	COM2 *
IRQ4	COM1 *
IRQ5	COM3 *
IRQ6	COM4 *
IRQ7	LPT *
IRQ8	Real Time Clock
IRQ9	FREE **
IRQ10	Digital I/O
IRQ11	PCI Interrupts
IRQ12	Mouse
IRQ13	Floating point processor
IRQ14	IDE
IRQ15	IDE

*	These IRQ references are default settings that can be changed by the user in the CMOS Settings utility. Reference the Super I/O Control section under Intel.
**	IRQ9 is commonly used by ACPI when enabled and may be unavailable (depending on operating system) for other uses.
***	IRQ15 is currently unavailable under the Windows operating systems.
Some IRQs can be freed for other uses if the hardware features they are assigned to are not being used. To free an interrupt, use the CMOS setup screens to disable any unused board features or their IRQ assignments.	

Interrupt Status Register - 29CH

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	N/A	N/A	N/A	COM4	COM3	COM2	COM1

Note: A **1** will be read for the device(s) with an interrupt pending.

WinSystems does not provide software support for implementing the Interrupt Status Register to share interrupts. Some operating systems, such as Windows XP and Linux, have support for sharing serial port interrupts and examples are available. The user will need to implement the appropriate software to share interrupts for the other devices.

PCI Devices and Functions

Bus:Device:Function	Function Description
Bus 0:Device 0:Fun: 0	Processor Host Bridge/DMI Controller
Bus 0:Device 2:Fun: 0	Processor Host Bridge/Graphics Controller
Bus 0:Device 2:Fun: 0	Processor Host Bridge/Graphics Controller
Bus 0:Device 25:Fun: 0	Internal GbE Controller
Bus 0:Device 26:Fun: 1	USB UHCI Controller
Bus 0:Device 26:Fun: 7	USB UHCI Controller
Bus 0:Device 26:Fun: 7	USB EHCI Controller
Bus 0:Device 27:Fun: 0	Intel High Definition Audio Controller
Bus 0:Device 28:Fun: 0	PCI Express Port 1
Bus 0:Device 28:Fun: 1	PCI Express Port 2
Bus 0:Device 29:Fun: 0	USB UHCI Controller
Bus 0:Device 29:Fun: 1	USB UHCI Controller
Bus 0:Device 29:Fun: 2	USB UHCI Controller
Bus 0:Device 29:Fun: 7	USB EHCI Controller
Bus 0:Device 30:Fun: 0	PCI-to-PCI Bridge
Bus 0:Device 31:Fun: 0	LPC Bridge
Bus0:Device 31:Fun: 0	IDE Controller
Bus 0:Device 31:Fun: 2	SATA Controller
Bus 0:Device 31:Fun: 3	SMBus Controller
Bus 0:Device 31:Fun: 6	ICH8M Thermal Subsystem
Bus 1:Device 0:Fun: 0	External GbE Controller
Bus 2:Device 0:Fun: 0	PCI Express MiniCard
Bus 3:Devicex:Fun: 0	PCI 2.0

DOS Legacy Memory Map

HEX Range	Usage
0000:0000-0009:FFFF	Main Memory (DOS area)
000A:0000-000B:FFFF	Legacy Video Area (SMM Memory)
000C:0000-000D:FFFF	Expansion Area
000E:0000-000E:FFFF	Extended System BIOS (Lower)
000F:0000-000F:FFFF	System BIOS (Upper)
0010:0000-TOM (Top of Memory)	Main Memory
FEC0:0000-FEC7:FFFF	IO APIC
FED0:x000-FED0:x3FF	High Precision Event Timers

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Watchdog Timer

The EPX-C380 features an advanced watchdog timer which can be used to guard against software lockups. Two interfaces are provided to the watchdog timer. The Advanced interface is the most flexible and recommended for new designs. The other interface option is provided for software compatibility with older WinSystems single board computers.

Advanced

The watchdog timer can be enabled in the BIOS Settings by entering a value for Watchdog Timeout on the Intel → Super I/O Control screen. Any non-zero value represents the number of minutes prior to reset during system boot. Once the operating system is loaded, the watchdog can be disabled or reconfigured in the application software.

NOTE: It is recommended that a long timeout be used if the watchdog is enabled when trying to boot any operating system.

The watchdog can be enabled, disabled or reset by writing the appropriate values to the configuration registers located at I/O addresses 565h and 566h. The watchdog is enabled by writing a timeout value other than zero to the I/O address 566h and disabled by writing **00h** to this I/O address. The watchdog timer is serviced by writing the desired timeout value to I/O port 566h. If the watchdog has not been serviced within the allotted time, the circuit resets the CPU.

The timeout value can be set from 1 second to 255 minutes. If port 565h bit 7 equals **0**, the timeout value written into I/O address 566h is in minutes. The timeout value written to address 566h is in seconds if port 565 bit 7 equals **1**.

Watchdog Timer Examples

Port Address	Port Bit 7 Value	Port Address	Value	Reset Interval
565H	x	566H	00h	DISABLED
565H	1	566H	03h	3 SECONDS
565H	1	566H	1Eh	30 SECONDS
565H	0	566H	04h	4 MINUTES
565H	0	566H	05h	5 MINUTES

Software watchdog timer PET = PORT 566H, write the timeout value.

Standard (requires changing the default I/O ranges within in the BIOS)

The watchdog can be enabled or disabled via software by writing an appropriate timeout value to I/O port 29EH. See the chart provided below.

Port Address	Value	Reset Interval
29EH	00h	DISABLED
	01h	3 SECONDS
	03h	30 SECONDS
	05h	300 SECONDS
29FH	ANY	RESET TIMER

Real-Time Clock/Calendar

A real-time clock is used as the AT-compatible clock/calendar. It supports a number of features including periodic and alarm interrupt capabilities. In addition to the time and date keeping functions, the system configuration is kept in CMOS RAM contained within the clock section. A battery must be enabled for the real-time clock to retain time and date during a power down.

STATUS LED

D14 - Status LED

Visual Index

A status LED is populated on the board at **D14**, which can be used for any application purpose. The LED is turned on during the boot process and can be turned off by writing a **0** to hex address 0x29D bit 0. The status LED can then be toggled on by writing a **1** and off by writing a **0** to the same address.

D14	--	GREEN	STATUS

CONNECTOR REFERENCE

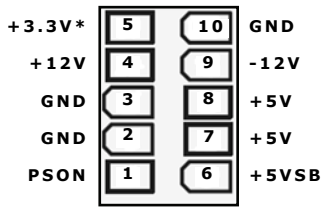
POWER

J6 - Power and Reset

Visual Index

PCB Connector: **MOLEX 87427-1043 (J6)**
Mating Connector: **MOLEX 39-01-2105 (Housing)**
MOLEX 39-00-0039 (Crimp)

J6



*** - only connects to the PC/104-*Plus* connector**

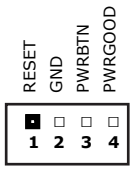
Power is applied to the EPX-C380 via the connector at **J6**. WinSystems offers the cable CBL-265-G-2-1.5 to simplify this connection.

J8 - ATX Signals

Visual Index

PCB Connector: **MOLEX 22-11-2042 (J8)**
Mating Connector: **MOLEX 22-01-3047 (Housing)**
MOLEX 08-55-0101 (Crimp)

J8



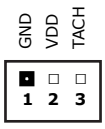
ATX signals for the power button, reset and power good are provided at **J8**. WinSystems offers the cable CBL-265-G-2-1.5 to simplify this connection.

J2 - Fan Power

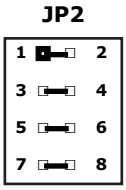
Visual Index

Mating Connector: **MOLEX 22-11-2032 (J2)**

J2



JP2 - Power Supply Selection



AT Power	1-2, 3-4, 5-6, 7-8 (default)
ATX Power	1 2, 3 4, 5 6, 7 8

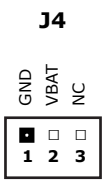
The EPX-C380 supports either AT (standard power supply) or ATX type power supplies. Zero load supplies are recommended. **JP2** specifies the style of supply connected to the single board computer (SBC). An AT power supply is a simple on/off supply with no interaction with the single board computer. Most embedded systems use this type of power supply and it is the default setting.

ATX type power supplies function with a “soft” on/off power button and a +5 VSB (standby). If an ATX compatible power supply is connected, **JP2** should be set accordingly and a power button (momentary contact) connected between pin 3 (power button) and pin 2 (ground) of **J8**. The +5 VSB signal provides the standby voltage to the EPX-C380 but does not power any other features of the board. When the power button is pressed, the EPX-C380 pulls PSON (Power Supply On) low and the power supply turns on all voltages to the single board computer. When the power button is pressed again, the BIOS signals the event so ACPI-compliant operating systems can be shutdown before the power is turned off. In ATX mode, if the power button is held for 4 seconds, the power supply is forced off, regardless of ACPI. Since this is software driven, it is possible that a software lockup could prevent the power button from functioning properly. For the BIOS to report the ATX supply to ACPI-compatible operating systems, **JP2** must be setup correctly.

J4 - External Battery

Visual Index

PCB Connector: **MOLEX 501953-0307 (J4)**
Mating Connector: **MOLEX 501939-0300 (Housing)**
MOLEX 501334-0100 or 501334-0000 (Crimp)



(For external battery. Provides battery backup to RTC and BIOS CMOS.)

WARNING: BAT-LTC-E-36-16-2 or BAT-LTC-E-36-27-2 must be connected at J4. Improper installation of the battery could result in explosive failure. Please be careful to note correct connection at location J4.

An optional external battery, connected at **J4**, supplies the EPX-C380 board with standby power for the real-time clock, CMOS setup RAM and SRAM (applicable models only). An extended temperature lithium battery is available from WinSystems, part number BAT-LTC-E-36-16-2 or BAT-LTC-E-36-27-2.

A power supervisory circuit contains the voltage sensing circuit and an internal power switch to route the battery or standby voltage to the circuits selected for backup. The battery automatically switches ON when the VCC of the systems drops below the battery voltage and back OFF again when VCC returns to normal.

J20 - LPT

Visual Index

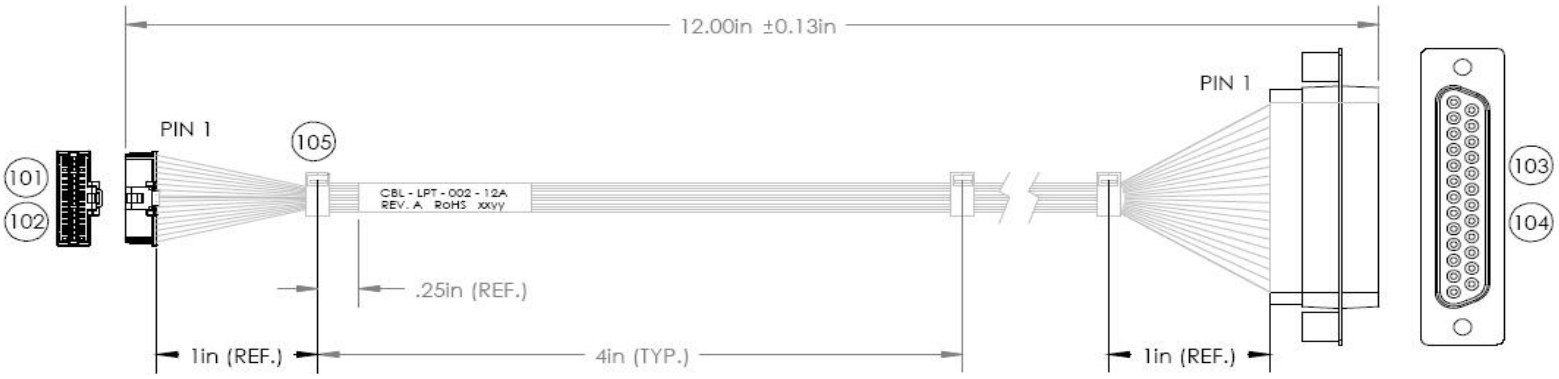
PCB Connector: **MOLEX 501571-3007 (J20)**
Mating Connector: **MOLEX 501189-3010 (Housing)**
MOLEX 501193-2000 (Crimp)

J20

GND	1	2	GND
STROBE	3	4	AUTOFEED
LPT DATA0	5	6	ERROR
LPT DATA1	7	8	PRNTER_INIT
LPT DATA2	9	10	SELECT
LPT DATA3	11	12	GND
LPT DATA4	13	14	GND
LPT DATA5	15	16	GND
LPT DATA6	17	18	GND
LPT DATA7	19	20	GND
ACK	21	22	GND
BUSY	23	24	GND
PAPER_END	25	26	GND
SELECT	27	28	GND
GND	29	30	GND

The LPT port , located at **J20**, is a multimode parallel printer port that supports the PS/2 Standard Bidirectional Parallel Port (SPP) and Enhanced Parallel Port (EPP) functionality. The output drivers support 8 mA per line.

The printer port can also be used as two additional general-purpose I/O ports if a printer is not required. The first port is configured as eight input or output only lines. The other port is configured as five input and three output lines.

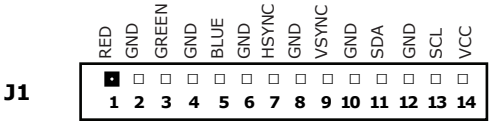


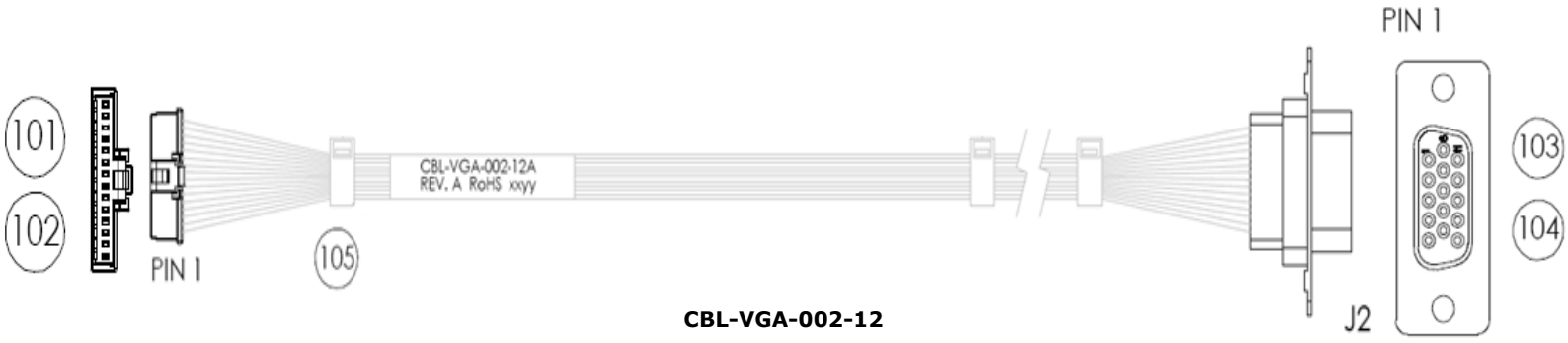
CBL-LPT-002-12

J1 - ANALOG VGA

Visual Index

PCB Connector: **MOLEX 501568-1407 (J1)**
Mating Connector: **MOLEX 501330-1400 (Housing)**
MOLEX 501334-0000 (Crimp)





CBL-VGA-002-12

J7 - LVDS

Visual Index

PCB Connector: MOLEX 501571-4007 (J7)
Mating Connector: MOLEX 501189-4010 (Housing)
MOLEX 501193-2000 (Crimp)

J7

SWVDD	1	2	GND
D0-	3	4	D0+
D1-	5	6	D1+
SWVDD	7	8	GND
D2-	9	10	D2+
NC	11	12	NC
SWVDD	13	14	GND
CLK-	15	16	CLK+
DDC_CLK	17	18	GND
DDC_DATA	19	20	GND
SWVDD	21	22	GND
NC	23	24	NC
NC	25	26	NC
SWVDD	27	28	GND
NC	29	30	NC
NC	31	32	NC
SWVDD	33	34	GND
NC	35	36	NC
NC	37	38	GND
NC	39	40	GND

J5 - Backlight Power

Visual Index

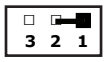
PCB Connector: MOLEX 501131-1107 (J5)
Mating Connector: MOLEX 99999-9999 (Housing)
MOLEX 99999-9999 (Crimp)

J5

VCC	1
ENABLE (Low)	2
ENABLE (High)	3
GND	4
+12V	5
BKLT_A	6
BKLT_A	7
BKLT_C	8
BKLT_C	9
LCTL_B DATA	10
LCTL_A CLK	11

HAZARD WARNING: **LCD panels can require a high voltage for the panel backlight. This high-frequency voltage can exceed 1000 volts and can present a shock hazard. Care should be taken when wiring and handling the inverter output. To avoid the danger of shock and to avoid the panel, make all connection changes with the power removed.**

JP1



Panel Power	5V 3.3V (default)	2-3 1-2

Avoid Simultaneous Jumpering of pins 1-2 and 2-3.
Misjumpering panel power causes damage to the board and/or the Flat Panel.

The EPX-C380 has an integrated display controller that interfaces to both Analog VGA and flat panel displays. The video output mode is selected in the CMOS setup. Simultaneous flat panel and Analog VGA mode is also supported. The Analog VGA connector is located at **J1**. WinSystems offers the cable CBL-VGA-002-12 to simplify the connection. The LVDS interface connector is located at **J7** to interface to flat panels. A backlight power connectors is located at **J5.** Panel power option selection is made at **JP1**.

Contact your WinSystems' Applications Engineer for information about available cable kits and supported panels.
This manual does not attempt to provide any information about how to connect to specific LCDs.

J10 - HD Audio

Visual Index

PCB Connector: **MOLEX 5020463070 (J10)**
Mating Connector: **MOLEX 5031103000 (Housing)**
MOLEX 501930-1100 (Crimp)

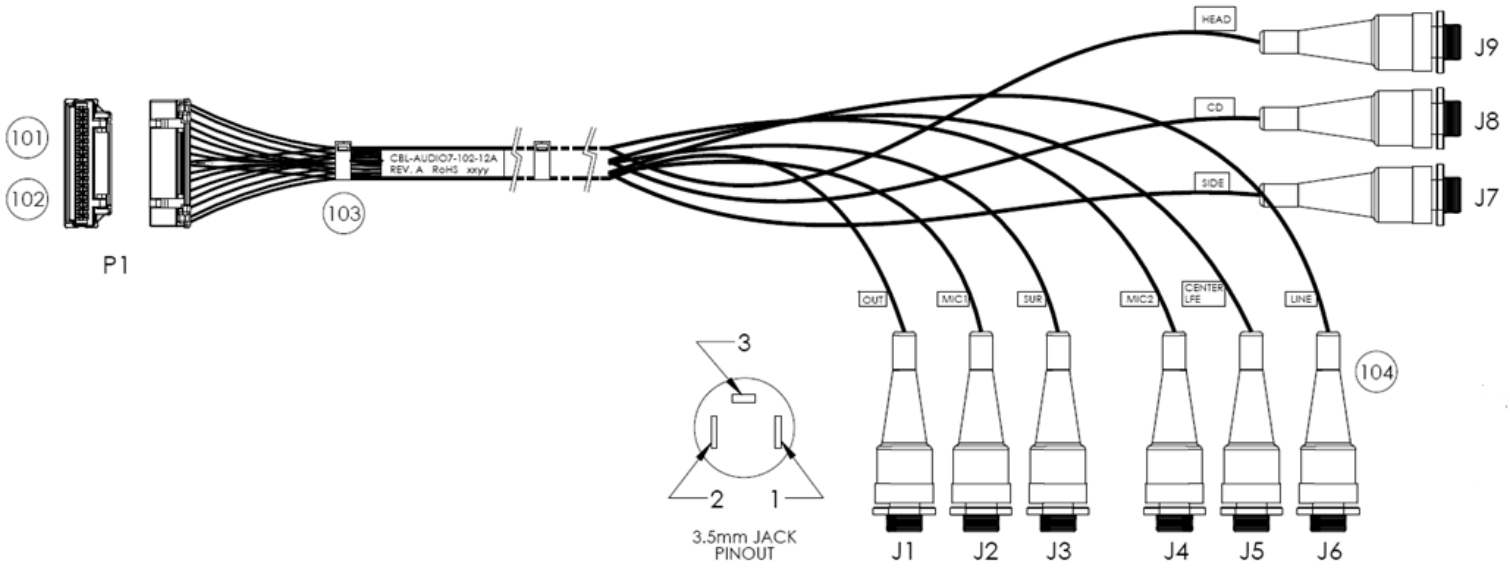
J10

ADGND	30	29	ADGND
ADGND	28	27	HEADPHONE-L
ADGND	26	25	HEADPHONE-R
CD-GND	24	23	ADGND
CD-L	22	21	SIDE-L
CD-R	20	19	SIDE-R
ADGND	18	17	ADGND
LINE-L	16	15	LFE
LINE-R	14	13	CENTER
ADGND	12	11	ADGND
MIC2-REAR-L	10	9	SUR-L
MIC2-REAR-R	8	7	SUR-R
ADGND	6	5	ADGND
MIC1-REAR-L	4	3	OUT-L
MIC1-REAR-R	2	1	OUT-R

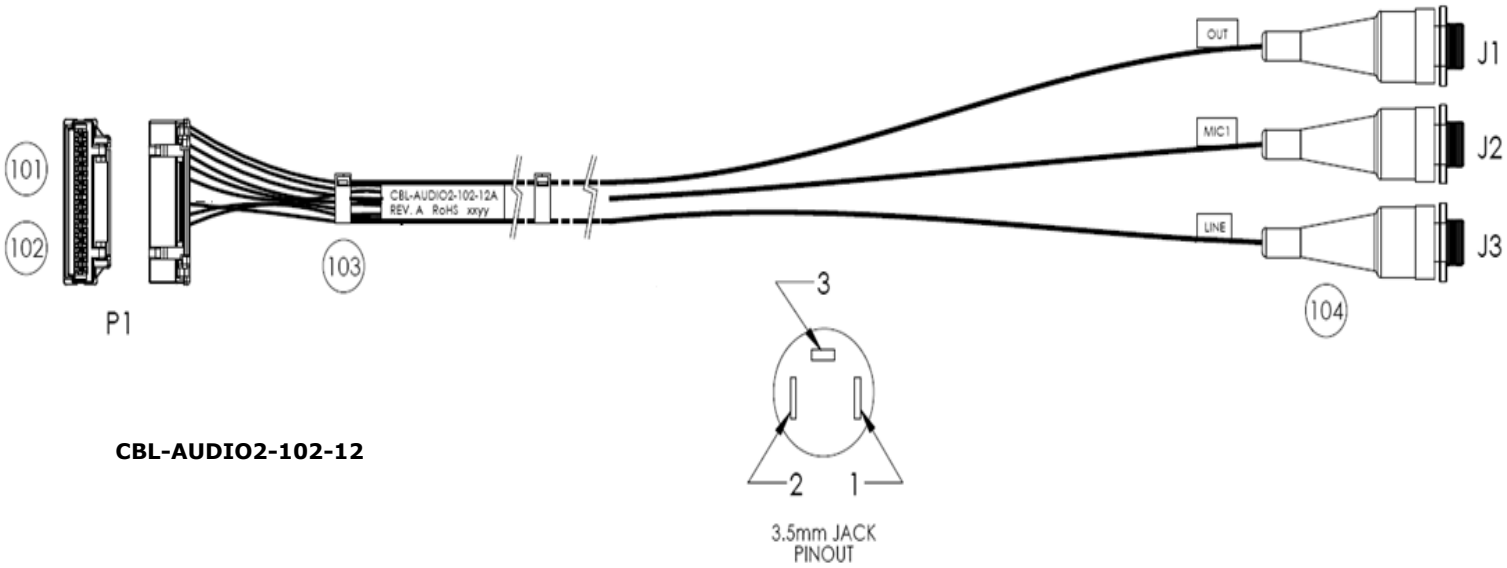
Audio External Connection

The Intel HD Audio controller is included with a VIA 1708B codec.

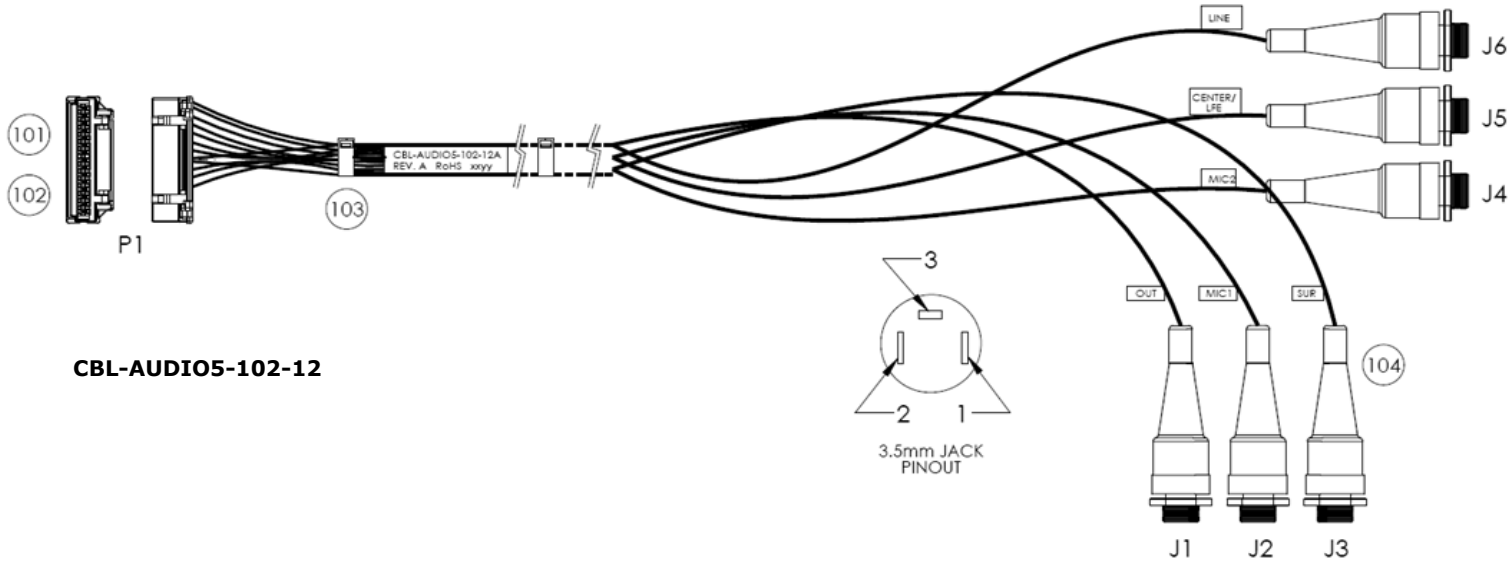
Audio connection is provided at **J10**. Three cables are available from WinSystems to adapt to this connector. CBL-AUDIO7-102-12 provides full 7.1 audio support. A simplified cable, CBL-AUDIO2-102-12, provides basic Line In, Line Out, and Microphone audio support and CBL-AUDIO5-102-12 provides 5.1 audio support.



CBL-AUDIO7-102-12



CBL-AUDIO2-102-12



CBL-AUDIO5-102-12

SP1 - Speaker

Speaker

An on-board speaker, **SP1**, is available for sound generation.

Beep Codes

Reference the chart Appendix-B section of this manual for the appropriate beep codes.

J18 - COM1, COM2, COM3, COM4

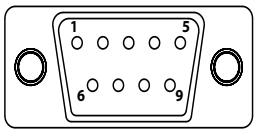
Visual Index

PCB Connector: MOLEX 502046-4070 (J18)
Mating Connector: MOLEX 503110-4000 (Housing)
MOLEX 501930-1100 (Crimp)

J18

DCD (COM1)	1	2	DSR (COM1)
RXD (COM1)	3	4	RTS (COM1)
TXD (COM1)	5	6	CTS (COM1)
DTR (COM1)	7	8	RI (COM1)
GND	9	10	GND
DCD (COM2)	11	12	DSR (COM2)
RXD (COM2)	13	14	RTS (COM2)
TXD (COM2)	15	16	CTS (COM2)
DTR (COM2)	17	18	RI (COM2)
GND	19	20	GND
DCD (COM3)	21	22	DSR (COM3)
RXD (COM3)	23	24	RTS (COM3)
TXD (COM3)	25	26	CTS (COM3)
DTR (COM3)	27	28	RI (COM3)
GND	29	30	GND
DCD (COM4)	31	32	DSR (COM4)
RXD (COM4)	33	34	RTS (COM4)
TXD (COM4)	35	36	CTS (COM4)
DTR (COM4)	37	38	RI (COM4)
GND	39	40	GND

COM1, COM2, COM3, COM4 [DB9 Male]



Pin	RS-232	RS-422	RS-485
1	DCD	N/A	N/A
2	RX	TX+	TX/RX+
3	TX	TX-	TX/RX-
4	DTR	N/A	N/A
5	GND	GND	GND
6	DSR	RX+	N/A
7	RTS	RX-	N/A
8	CTR	N/A	N/A
9	RI	N/A	N/A

All ports are configured as Data Terminal Equipment (DTE). Both the send and receive registers of each port have a 16-byte FIFO. All serial ports have 16C550-compatible UARTs. The RS-232 has a charge pump to generate the plus and minus voltages so the EPX-C380 only requires +5V to operate. An independent, software programmable baud rate generator is selectable from 50 through 115.2 kbps. Individual modem handshake control signals are supported for all ports.

COM1, COM2, COM3, COM4 Configuration Options in BIOS

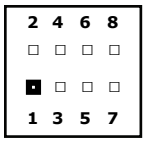
1. RS-232 Mode
2. RS-422 Mode with RTS transmitter enable
3. RS-422 Mode with auto transmitter enable
4. RS-485 Mode with RTS transmitter enable
5. RS-485 Mode with RTS transmitter enable and echo back
6. RS-485 Mode with auto transmitter enable
7. RS-485 Mode with auto transmitter enable and echo back

Mode(s)	Configuration Note
2, 4, 5	Require the RTS bit (MCR Bit 1) to be set in order to transmit.
3, 6, 7	Require TX/RX(300) termination on one node.
4	Requires the RTS (MCR Bit 1) be de-asserted in order to receive.
* Each of the RS-422/RS-485 modes allow for jumper selection of transmit and/or receive termination and biasing resistor(s). An 8-pin configuration jumper is provided for each port.	

Termination Resistors

COM1 = **JP5** COM3 = **JP7***

COM2 = **JP6** COM4 = **JP8***



*** COM3 and COM4 are RS-232 only for model EPX-C380-S1-0.**

RS-422 Termination and Biasing Resistors		
TX (100): Places a 100Ω Resistor across the TX+/TX- pair		3-4
RX (100): Places a 100Ω Resistor across the RX+/RX- pair		7-8
TX(300):	Places a 100Ω Resistor from +5V to TX+	1-2
	Places a 100Ω Resistor between TX+ and TX-	3-4
	Places a 100Ω Resistor from Ground to TX-	5-6

RS-485 Termination and Biasing Resistors		
TX (100): Places a 100Ω Resistor across the TX/RX+/TX/RX- pair		3-4
TX/RX(300):	Places a 100Ω Resistor from +5V to TX/RX+	1-2
	Places a 100Ω Resistor between TX/RX+ and TX/RX-	3-4
	Places a 100Ω Resistor from Ground to TX/RX-	5-6

J9, J11 - USB

Visual Index

PCB Connector: MOLEX 501571-2007 (J9, J11)
Mating Connector: MOLEX 501189-2010 (Housing)
MOLEX 501193-2000 (Crimp)

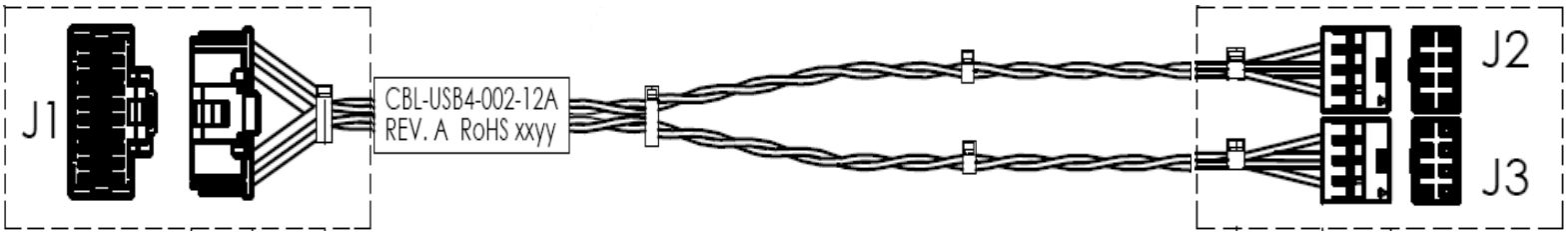
NOTE: USB (J9) is not applicable for model EPX-C380-S1-0.

J11
USB (0/1/2/3)

USBPWR0	1	2		USBPWR1
D0-	3	4		D1-
D0+	5	6		D1+
GND	7	8		GND
GND	9	10		GND
GND	11	12		GND
USBPWR2	13	14		USBPWR3
D2-	15	16		D3-
D2+	17	18		D3+
GND	19	20		GND

J9
USB (4/5/6/7)

USBPWR4	1	2		USBPWR5
D4-	3	4		D5-
D4+	5	6		D5+
GND	7	8		GND
GND	9	10		GND
GND	11	12		GND
USBPWR6	13	14		USBPWR7
D6-	15	16		D7-
D6+	17	18		D7+
GND	19	20		GND



CBL-USB4-002-12 with ADP-10-USB-001

Up to two USB cables may be attached to the EPX-C380 via the connectors for a total of eight USB 2.0 ports. These are terminated to 20-pin connector at **J9** and **J11**. An adapter cable CBL-USB4-002-12 is available from WinSystems for connection along with ADP-IO-USB-001.

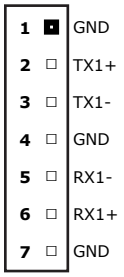
SERIAL ATA

J13, J16 - SATA

Visual Index

PCB Connector: **MOLEX 67490-1220 (J13, J16)**

J13, J16



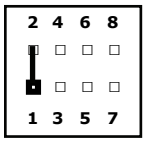
The EPX-C380 supports two SATA interfaces located at **J13** and **J16**.

COMPACTFLASH

J501 - CompactFlash

Visual Index

JP3



CompactFlash Master (default)	1-2
CompactFlash Slave	1 2

When using a CompactFlash device, Master/Slave selection is made using jumper field **JP3**. The EPX-C380 supports solid state CompactFlash storage devices for applications where the environment is too harsh for mechanical hard disks.

The CompactFlash socket at **J501** supports modules with TrueIDE support. WinSystems offers industrial grade CompactFlash modules that provide high performance and extended temperature operation (-40ºC to +85ºC). An activity LED is present at **D511**.

NOTE: SRAM is not applicable for model EPX-C380-S1-0.

The EPX-C380 board provides 1 MB of battery-backed user SRAM. The 1 MB SRAM is normally used as a solid state disk device by using the appropriate driver for your operating systems.

For example, the DOS driver **USSD.SYS** can be used to make the SRAM appear as a drive in the system by adding the following to **config.sys**.

Device = c:\ussd.sys /mod:u /pad:210 /dsz:1024

The base address for the SRAM is located at 0210h.

There are four I/O registers used for accessing the memory array. The register definition and usage is defined below.

OFFSET 0 - MSB Address Register
D7 - A23 of access address
D6 - A22 of access address
D5 - A21 of access address
D4 - A20 of access address
D3 - A19 of access address
D2 - A18 of access address
D1 - A17 of access address
D0 - A16 of access address

This register is write-only and holds the upper 8 bits of the 24-bit address used to access the 1 MB SRAM.

OFFSET 1 - NSB Address Register
D7 - A15 of access address
D6 - A14 of access address
D5 - A13 of access address
D4 - A12 of access address
D3 - A11 of access address
D2 - A10 of access address
D1 - A9 of access address
D0 - A8 of access address

This register is write-only and holds the middle 8 bits of address used to access the 1 MB memory array. Writing this register also clears the LSB address counter to 0.

OFFSET 2 - Data Access Register A
D7 - D7 of memory data
D6 - D6 of memory data
D5 - D5 of memory data
D4 - D4 of memory data
D3 - D3 of memory data
D2 - D2 of memory data
D1 - D1 of memory data
D0 - D0 of memory data

This read/write register is the primary window to the memory array. A value written to this port will be written to the address in the memory array specified by the MSB register, the NSB register, and the current LSB counter address. In like fashion, a read from this I/O address will result in the current memory array data at the address specified by the MSB register, the NSB register, and the LSB address counter. In either case, read or write, an access to this register results in the LSB address counter being incremented immediately following the access so that the next access will be at the next sequential address in the array. This incrementing process does **not** carry into the NSB or MSB register which must be rewritten every 256 bytes.

OFFSET 3 - Data Access Register B
D7 - D7 of memory data
D6 - D6 of memory data
D5 - D5 of memory data
D4 - D4 of memory data
D3 - D3 of memory data
D2 - D2 of memory data
D1 - D1 of memory data
D0 - D0 of memory data

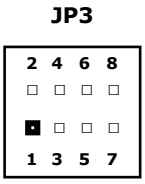
This read/write register is used to access the memory array when post incrementing of the LSB counter is not desired. The byte written or read will still be specified by the 24-bit combination of the MSB register, the NSB register, and the LSB counter. However, the LSB counter will **not** be altered following the access. It will then be necessary to do one more read from Data Access Register A in order to bump the address to the next byte.

OFFSET 4 - Write Protect Register
D7 - D6 - Reserved
D0 - Write Protect Bit, 0 = Protected, 1 = Writeable

This write-only register controls the write protect function of the 1 MB SRAM board. On power up, the write protect bit is cleared (disabling writes) and must be explicitly enabled by writing a **1** to the I/O port at the BASE address +4. To re-enable the write protection, write a **0** at this register. The **USSD.SYS** device will enable writing only during that time when a sector is being transferred, which contributes greatly to data safety and integrity.

OPTIONAL SSD

The EPX-C380 can be populated with an optional on-board Flash disk for rugged OEM applications where a removal device is not desirable. The Flash disk is connected to the PATA controller. Since the on-board Flash disk may co-exist with a CompactFlash device, it can be set as Master by installing a jumper at **JP3** pins 3-4 or Slave when the **JP3** pins 3 and 4 are open.



SSD Master	3-4
SSD Slave (default)	3 4
SSD Write Protect	5-6
SSD Program Enable (default)	5 6

A jumper at **JP3** 5-6 protects the on-board Flash disk. When **JP3** pins 5 and 6 are open, read/write access is available to the on-board Flash disk.

Please contact an Applications Engineer if you are interested in this optional feature.

J21 - Ethernet

Visual Index

PCB Connector: MOLEX 502046-2070 (J11)
Mating Connector: MOLEX 503110-2000 (Housing)
MOLEX 501930-1100 (Crimp)

J21

(G1) MX1+	1	2		(G1) MX1-
(G1) MX2+	3	4		(G1) MX2-
(G1) MX3+	5	6		(G1) MX3-
(G1) MX4+	7	8		(G1) MX4-
GND	9	10		GND
(G2) MX1+	11	12		(G2) MX1-
(G2) MX2+	13	14		(G2) MX2-
(G2) MX3+	15	16		(G2) MX3-
(G2) MX4+	17	18		(G2) MX4-
GND	19	20		GND

ADP-IO-ENET-001

Gigabit Ethernet Controllers

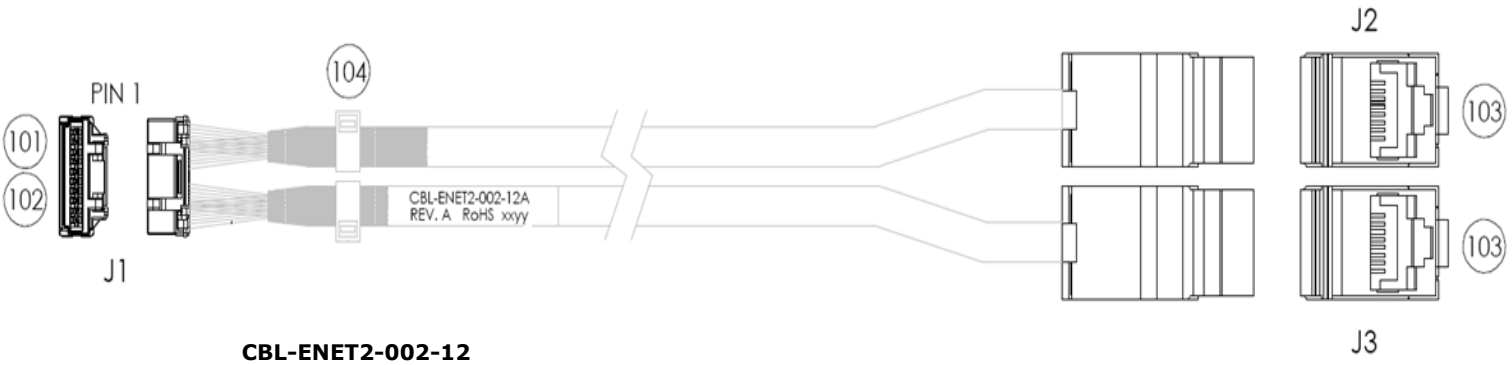
The EPX-C380 is equipped with two Intel Gigabit Ethernet controllers, one from ICH8 and one from 82574. Each of these provides a standard IEEE 802.3 Ethernet interface for 1000/100/10BASE-T networks. The connections for each Ethernet port are available at **J21**. WinSystems offers CBL-ENET2-002-12, to interfere to two RJ-45 jacks.

On-board Ethernet activity LEDs **D518-D520** are provided for Port 1. LEDs **D515-D517** are associated with Port 2. These activity signals are also available off-board for enclosures or other applications that have remote mounting requirements. The activity signals for Port 1 are provided at connector **J25**. The signals for Port 2 are provided at **J26**. See tables below for signal and pin definitions.

NOTE: Model EPX-C380-S1-0 only includes one Ethernet controller for ICH8.

CBL-ENET2-004-12

CBL-ENET2-003-12



CBL-ENET2-002-12

J25, J26 - Ethernet LEDs

Visual Index

PCB Connector: MOLEX 5019530407 (J25, J26)
Mating Connector: MOLEX 5019390400 (Housing)
MOLEX 501334-0100 or 501334-0000 (Crimp)

J26
(Ethernet Port 1)

Pin	LED	Color	Signal
1	D518	RED	ACTIVITY
2	D519	YELLOW	SPEED100
3	D520	GREEN	SPEED1000
4	-	-	+3V

J25
(Ethernet Port 2)

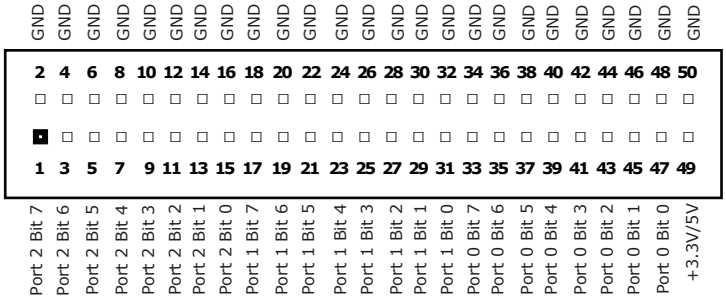
Pin	LED	Color	Signal
1	D515	RED	ACTIVITY
2	D516	YELLOW	SPEED100
3	D517	GREEN	SPEED1000
4	-	-	+3VSB

J23, J24 - Digital I/O

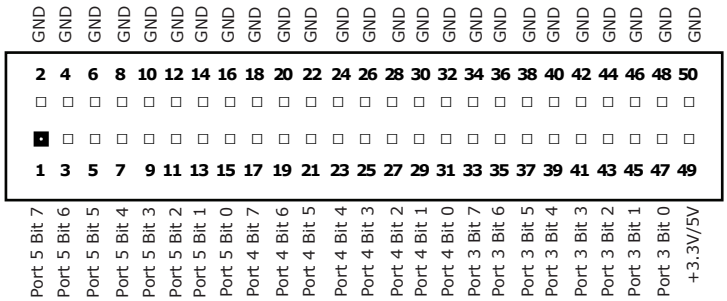
Visual Index

PCB Connector: **MOLEX 5015715007 (J23, J24)**
Mating Connector: **MOLEX 5011895010 (Housing)**
MOLEX 501193 (Crimp)

J23 (Ports 0/1/2)



J24 (Ports 3/4/5)



The EPX-C380 has 48 open collector digital I/O bits with a default base address of 120H. Each bit is configured as an open collector with a 10K pullup. Each bit is able to sink up to 8mA. The first 24 lines are capable of fully latched event sensing with polarity being software programmable.

Digital I/O Connectors

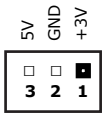
These 48 lines of digital I/O are terminated through two 50-pin connectors at **J23** and **J24**. The **J23** connector handles I/O ports 0 through 2 while **J24** handles ports 3 through 5.

JP9 - Digital I/O Power

Visual Index

The I/O connectors can provide +5V or +3.3V to an I/O rack for miscellaneous purposes by jumpering **JP9**. When J**P9** is jumpered (2-3), +5V is provided at pin 49 of **J23** and **J24**. If **JP9** is jumpered (1-2), then +3.3V is provided at pin 49 of **J23** and **J24**. It is the user's responsibility to limit current to a safe value (less than 400 mA) to avoid damaging the CPU board.

JP9



STOP

Avoid Simultaneous Jumpering of pins 1-2 and 2-3.
Misjumpering causes damage to the board.

+3.3V is provided at pin 49 of **J23/J24**	1-2
+5V is provided at pin 49 of **J23/J24**	2-3
No Power at Pin 49 of **J23/J24** (default)	OPEN

Register Definitions (WS16C48)

Visual Index

The EPX-C380 uses the WinSystems exclusive ASIC device, the WS16C48. This device provides 48 lines of digital I/O. There are 16 unique registers within the WS16C48. The following table summarizes the registers, and the text that follows provides details on each of the internal registers.

I/O Address Offset	Page 0	Page 1	Page 2	Page 3
00H	Port 0 I/O	Port 0 I/O	Port 0 I/O	Port 0 I/O
01H	Port 1 I/O	Port 1 I/O	Port 1 I/O	Port 1 I/O
02H	Port 2 I/O	Port 2 I/O	Port 2 I/O	Port 2 I/O
03H	Port 3 I/O	Port 3 I/O	Port 3 I/O	Port 3 I/O
04H	Port 4 I/O	Port 4 I/O	Port 4 I/O	Port 4 I/O
05H	Port 5 I/O	Port 5 I/O	Port 5 I/O	Port 5 I/O
06H	Int_Pending	Int_Pending	Int_Pending	Int_Pending
07H	Page/Lock	Page/Lock	Page/Lock	Page/Lock
08H	Reserved	Pol_0	Enab_0	Int_ID0
09H	Reserved	Pol_1	Enab_1	Int_ID1
0AH	Reserved	Pol_2	Enab_2	Int_ID2

Register Details

Port 0 through 5 I/O

Each I/O bit in each of the six ports can be individually programmed for input or output. Writing a **0** to a bit position causes the corresponding output pin to go to a high-impedance state (pulled high by external 10 KΩ resistors). This allows it to be used as an input. When used in the input mode, a read reflects the inverted state of the I/O pin, such that a high on the pin will read as a **0** in the register. Writing a **1** to a bit position causes that output pin to sink current (up to 12 mA), effectively pulling it low.

INT_PENDING

This read-only register reflects the combined state of the INT_ID0 through INT_ID2 registers. When any of the lower three bits are set, it indicates that an interrupt is pending on the I/O port corresponding to the bit position(s) that are set. Reading this register allows an Interrupt Service Routine to quickly determine if any interrupts are pending and which I/O port has a pending interrupt.

PAGE/LOCK

This register serves two purposes. The upper two bits select the register page in use as shown here:

D7	D6	Page
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

Bits 5-0 allow for locking the I/O ports. A **1** written to the I/O port position will prohibit further writes to the corresponding I/O port.

POL0 - POL2

These registers are accessible when Page 1 is selected. They allow interrupt polarity selection on a port–by–port and bit-by-bit basis. Writing a **1** to a bit position selects the rising edge detection interrupts while writing a **0** to a bit position selects falling edge detection interrupts.

ENAB0 - ENAB2

These registers are accessible when Page 2 is selected. They allow for port-by-port and bit-by-bit enabling of the edge detection interrupts. When set to a **1**, the edge detection interrupt is enabled for the corresponding port and bit. When cleared to **0**, the bit's edge detection interrupt is disabled. Note that this register can be used to individually clear a pending interrupt by disabling and re-enabling the pending interrupt.

INT_ID0 – INT_ID2

These registers are accessible when Page 3 is selected. They are used to identify currently pending edge interrupts. A bit when read as a **1** indicates that an edge of the polarity programmed into the corresponding polarity register has been recognized. Note that a write to this register (value ignored) clears ALL of the pending interrupts in this register.

J12, J15 - PC/104

Visual Index

PCB Connector: **TEKA PC232-A-1BD-M (J12)**
TEKA PC220-A-1BD-M (J15)

The PC/104 bus is electrically equivalent to the 16-bit ISA bus. Standard PC/104 I/O cards can be populated on EPX-C380's connectors, located at **J12** and **J15**. The interface does not support hot swap capability. The PC/104 bus connector pin definitions are provided below for reference. Refer to the PC/104 Bus Specification for specific signal and mechanical specifications.

J15 (C/D)

GND	D0		C0	GND
MEMCS16#	D1		C1	SBHE#
IOCS16#	D2		C2	LA23
IRQ10	D3		C3	LA22
IRQ11	D4		C4	LA21
IRQ12	D5		C5	LA20
IRQ15	D6		C6	LA19
IRQ14	D7		C7	LA18
DACK0#	D8		C8	LA17
DRQ0	D9		C9	MEMR#
DACK5#	D10		C10	MEMW#
DRQ5	D11		C11	SD8
DACK6#	D12		C12	SB9
DRQ6	D13		C13	SD10
DACK7#	D14		C14	SD11
DRQ7	D15		C15	SD12
+5V	D16		C16	SD13
MASTER#	D17		C17	SD14
GND	D18		C18	SD15
GND	D19		C19	KEY

J12 (A/B)

IOCHK#	A1		B1	GND
SD7	A2		B2	RESET
SD6	A3		B3	+5V
SD5	A4		B4	IRQ
SD4	A5		B5	-5V
SD3	A6		B6	DRQ2
SD2	A7		B7	-12V
SD1	A8		B8	SRDY#
SD0	A9		B9	+12V
IOCHRDY	A10		B10	KEY
AEN	A11		B11	SMEMW#
SA19	A12		B12	SMEMR#
SA18	A13		B13	IOW#
SA17	A14		B14	IOR#
SA16	A15		B15	DACK3#
SA15	A16		B16	DRQ3
SA14	A17		B17	DACK1#
SA13	A18		B18	DRQ1
SA12	A19		B19	REFRESH#
SA11	A20		B20	BCLK
SA10	A21		B21	IRQ7
SA9	A22		B22	IRQ6
SA8	A23		B23	IRQ5
SA7	A24		B24	IRQ4
SA6	A25		B25	IRQ3
SA5	A26		B26	DACK2#
SA4	A27		B27	TC
SA3	A28		B28	BALE
SA2	A29		B29	+5V
SA1	A30		B30	OSC
SA0	A31		B31	GND
GND	A32		B32	GND

= Active Low Signal

NOTES:

1. Rows C and D are not required on 8-bit modules.
2. B10 and C19 are key locations. WinSystems uses key pins as connections to GND.
3. Signal timing and function are as specified in ISA specification.
4. Signal source/sink current differ from ISA values.

J14 - PC/104-*Plus*

Visual Index

PCB Connector: **TEKA 2MR430-BDWM-368-00**

The PC/104-*Plus* is electrically equivalent to the 33 MHz PCI bus and is terminated to a 120-pin, nonstackthrough connector. The standard PC/104-*Plus* I/O modules can be populated on EPX-C380's PC104-*Plus* bus. The interface does not support hot swap capability. The PC/104-Plus bus connector is located at **J14**. Refer to the PC/104-*Plus* Bus Specification for specific signal and mechanical specifications. The pin definitions are:

PIN	A	B	C	D
1	GND	RESERVED	+5V	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD007	GND	AD06
5	GND	AD009	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1#	AD15	+3.3V
9	SERR#	GND	RESERVED	PAR
10	GND	PERR#	+3.3V	RESERVED
11	STOP#	+3.3V	LOCK#	GND
12	+3.3V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	+3.3V
14	GND	AD16	+3.3V	C/BE2#
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0#	GND	REQ1#	VI/O
24	GND	REQ2#	+5V	GNT0#
25	GNT1#	VI/O	GNT2#	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD#	+5V	RST#
29	+12V	INTA#	INTB#	INTC#
30	-12V	REQ3#	GNT3#	GND

J502 - MiniPCIe

Visual Index

PCB Connector: **MOLEX 0679105700 (J502)**

NOTE: MiniPCIe is not applicable for model EPX-C380-S1-0.

The EPX-C380 includes a MiniPCIe socket at **J502**. Though the socket can support other devices, it is most often used to add wireless Ethernet cards from Broadcom®, Foxconn®, (Atheros), or others.

Pin	Name	Pin	Name
2	3.3Vaux	**1**	WAKE#
4	GND	**3**	COEX1
6	1.5V	**5**	COEX2
8	UIM_PWR	**7**	CLKREQ#
10	UIM_DATA	**9**	GND
12	UIM_CLK	**11**	REFCLK-
14	UIM_RESET	**13**	REFCLK+
16	UIM_VPP	**15**	GND
Mechanical Key			
18	GND	**17**	Reserved (UIM_C8)
20	W_DISABLE#	**19**	Reserved (UIM_C4)
22	PERST#	**21**	GND
24	+3.3Vaux	**23**	PERn0
26	GND	**25**	PERp0
28	+1.5V	**27**	GND
30	SMB_CLK	**29**	GND
32	SMB_DATA	**31**	PETn0
34	GND	**33**	PETp0
36	USB_D-	**35**	GND
38	USB_D+	**37**	GND
40	GND	**39**	+3.3Vaux
42	LED_WWAN#	**41**	+3.3Vaux
44	LED_WLAN#	**43**	GND
46	LED_WPAN#	**45**	Reserved
48	+1.5V	**47**	Reserved
50	GND	**49**	Reserved
52	+3.3Vaux	**51**	Reserved

MiniPCIe LEDs

LED	Color	Signal
D512	RED	WWAN
D513	RED	WLAN
D514	RED	WPAN

General Information

The EPX-C380 includes BIOS from Phoenix Technologies to assure full compatibility with PC operating systems and software. The basic system configuration is stored in battery backed CMOS RAM within the clock/calendar. As an alternative, the CMOS configuration may be stored in EEPROM for operation without a battery. For more information of CMOS configuration, see the BIOS Settings Storage Options section of this manual. Access to this setup information is via the Setup Utility in the BIOS.

Entering Setup

To enter setup, power up the computer and press **F2** when either the splash screen is displayed or when the **Press F2 for Setup** message is displayed. It may take a few seconds before the main setup menu screen is displayed.

Navigation of the Menus

Use the **Up** and **Down** arrow keys to move among the selections and press **Enter** when a selection is highlighted to enter a sub-menu or to see a list of choices. Following are images of each menu screen in the default configuration along with a brief description of each option where applicable. Available options are listed in reference tables. Menu values shown in **bold** typeface are factory defaults.

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Main Menu	
System Time:	**09:40:34**
System Date:	**04/09/2010**
>IDE Primary/Master	**None**
>IDE Primary/Slave	**None**
>SATA Port 1	**None**
>SATA Port 2	**None**
System Memory:	633 KB
Extended Memory:	2085888 KB
Ethernet MAC Address 1:	xx:xx:xx:xx:xx:xx
Ethernet MAC Address 2:	xx:xx:xx:xx:xx:xx
CPU Temperature:	50 °C/132 °F
Ambient Temperature:	40 °C/104 °F

Each available option is listed in detail in the following sections.

Navigation to the screens is located at the top of each screen's layout.

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Depending on the Primary Master **Type**, various Primary Master options will be available. See the following screens.

Main Menu > **IDE Primary Master/Slave [None]**	
Type:	**Auto**
Multi-Sector Transfers:	**Disabled**
LBA Mode Control:	**Disabled**
32 Bit I/O:	**Disabled**
Options: Disabled Enabled	
Transfer Mode:	**FPIO 4 / DMA 2**
Ultra DMA Mode:	**Disabled | (Mode 2 for IDE Primary Slave only)**
SMART Monitoring	**Disabled**

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Depending on the Primary Master **Type**, various Primary Master options will be available. See the following screens.

Main Menu > **SATA Port 1**	
Type:	**Auto**
Multi-Sector Transfers:	**Disabled**
LBA Mode Control:	**Disabled**
32 Bit I/O:	**Disabled**
Options: Disabled Enabled	
Transfer Mode:	**Standard**
Ultra DMA Mode:	**Disabled**
SMART Monitoring	**Disabled**

Main Menu > **SATA Port 2**	
Type:	**Auto**
Multi-Sector Transfers:	**Disabled**
LBA Mode Control:	**Disabled**
32 Bit I/O:	**Disabled**
Options: Disabled Enabled	
Transfer Mode:	**Standard**
Ultra DMA Mode:	**Disabled**

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Advanced	
Installed O/S:	**Win95**
Options: Other Win95 Win98 WinMe Win2000	
Reset Configuration Data:	**No**
Options: No Yes	
Large Disk Access Mode:	**DOS**
Options: Other DOS	
Summary screen:	**Disabled**
Options: Disabled Enabled	
Boot-time Diagnostic Screen:	**Enabled**
Options: Disabled Enabled	
QuickBoot Mode:	**Enabled**
Options: Disabled Enabled	
Extended Memory Testing:	**None**
Options: Normal Just zero it None	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel
> CPU Control Sub-Menu
> Video (Intel IGD) Control Sub-Menu
> ICH Control Sub-Menu
> Super I/O Control Sub-Menu
> ACPI Control Sub-Menu

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > CPU Control Sub-Menu	
Hyperthreading:	**Enabled**
Options: Disabled Enabled	
Processor Power Management:	**Enabled**
Options: Disabled GV3 Only C-States Only Enabled	
Timestamp Counter Updates	**Enabled**
Options: Disabled Enabled	
> CPU Thermal Control Sub-Menu	
Set Max Ext CPUID = 3	**Disabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > CPU Control Sub-Menu > **CPU Thermal Control Sub-Menu**	
Thermal Control Circuit:	**Disabled**
Options: Disabled TM1	
DTS Enable:	**Disabled**
Options: Disabled Enabled	
Active Trip Point:	**55 C**
Options: Disabled 55 C 63 C 71 C 79 C 87 C 95 C 103 C 111 C 119 C	
Passive Cooling Trip Point:	**95 C**
Options: Disabled 55 C 63 C 71 C 79 C 87 C 95 C 103 C 111 C 119 C	
Passive TC1 Value:	**1**
Passive TC2 Value:	**5**
Options: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	
More CPU Thermal Control Sub-Menu options are continued on the next page.	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > CPU Control Sub-Menu > CPU Thermal Control Sub-Menu (continued)

Passive TSP Value:	**10**
Options: 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150	
Critical Trip Point:	**POR**
Options: POR 15 C 23 C 31 C 39 C 47 C 55 C 63 C 71 C 79 C 87 C 95 C 103 C 111 C 119 C 127 C	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > Video (Intel IGD) Control Sub-Menu	
IGD - VBIOS Boot Type:	**CRT**
Options: VBT Default CRT LFP CRT+LFP	
> IGD - LCD Control Sub-Menu	
DVMT 4.0 Mode:	**Auto**
Options: Fixed DVMT Auto	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > Video (Intel IGD) Control Sub-Menu > **IGD - LCD Control Sub-Menu**	
IGD - LCD Panel Type:	**3: 1024x768 LVDS**
Options: 1: 640x480 LVDS 2: 800x600 LVDS 3: 1024x768 LVDS 4: 1024x600 LVDS 5: 800x480 LVDS 6: Reserved 7: Reserved 8: 1280x768 LVDS 9: Reserved 10: Reserved 11: Reserved 12: Reserved 13: Reserved 14: 1280X800 LVDS 15: 1280X600 LVDS 16: Reserved	
IGD - Panel Scaling:	**Auto**
Options: Auto Force Scaling Off	
GMCH BLC Control:	**GMBus**
Options: Disabled PWM GMBus	
BIA Control	**Disabled**
Options: Automatic Disabled Level 1 Level 2 Level 3 Level 4 Level 5	
Spread Spectrum Clock Chip:	**Off**
Options: Off Hardware Software	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > ICH Control Sub-Menu	
> Integrated Device Control Sub-Menu	
Pop Up Mode Enable:	**Enabled**
Options: Disabled Enabled	
Pop Down Mode Enable:	**Enabled**
Options: Disabled Enabled	
LPC Decode Range 1 Base Address:	**300h**
LPC Decode Range 1 Size:	**64 Bytes**
Options: 64 Bytes 32 Bytes 16 Bytes 8 Bytes 4 Bytes	
LPC Decode Range 2 Base Address:	**500h**
LPC Decode Range 2 Size:	**256 Bytes**
Options: 256 Bytes 128 Bytes 64 Bytes 32 Bytes 16 Bytes 8 Bytes 4 Bytes	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > ICH Control Sub-Menu > **Integrated Device Control Sub-Menu**	
> PCI Express Control Sub-Menu	
> ICH USB Control Sub-Menu	
Azalia HD Audio Function:	**Auto**
Options: Disabled Auto	
SATA/PATA Configuration:	**Enhanced**
Options: Compatible Enhanced	
AHCI Configuration:	**Disabled**
Options: Disabled Enabled	
Disable Vacant Ports:	**Disabled**
Options: Disabled Enabled	
On-board LAN:	**Enabled**
Options: Disabled Enabled	
PXE OPROM:	**Disabled**

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > ICH Control Sub-Menu > Integrated Device Control Sub-Menu > **PCI Express Control Sub-Menu**	
PCI Express - Root Port 1:	**Enabled**
Options: Disabled Enabled Auto	
PCI Express - Root Port 2:	**Auto**
Options: Disabled Enabled Auto	
Root Port ASPM Support:	**Auto**
Options: Disabled Auto	
ASPM Latency Checking:	**Auto**
Options: Disabled Auto	
> PCI/PNP ISA IRQ Resource Exclusion	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > ICH Control Sub-Menu > Integrated Device Control Sub-Menu > PCI Express Control Sub-Menu **PCI/PNP ISA IRQResource Exclusion**	
IRQ 3:	**Available**
Options: Available Reserved	
IRQ 4:	**Available**
Options: Available Reserved	
IRQ 5:	**Available**
Options: Available Reserved	
IRQ 7:	**Available**
Options: Available Reserved	
IRQ 9:	**Available**
Options: Available Reserved	
IRQ 10:	**Reserved**
Options: Available Reserved	
IRQ 11:	**Available**
Options: Available Reserved	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > ICH Control Sub-Menu > Integrated Device Control Sub-Menu > **ICH USB Control Sub-Menu**	
Overcurrent Detection	**Enabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > Super I/O Control Sub-Menu

Serial port 1:	**Enabled**
Speed:	**Low**
Base I/O address:	**3F8**
Interrupt:	**IRQ 4**
Interface:	**RS232**

Options:

Port x:	**Speed:**	**Base I/O address:**	**Interrupt:**	**Interface:**
Disabled	Low	3F8	Disabled	RS232
Enabled	High	2F8	IRQ 3	RS422 RTS
		3E8	IRQ 4	RS422 Auto
		2E8	IRQ 5	RS485 RTS
			IRQ 6	RS485 RTS w/Echo
			IRQ 7	RS485 Auto
			IRQ 9	RS485 Auto w/Echo

Serial port 2:	**Enabled**
Speed:	**Low**
Base I/O address:	**2F8**
Interrupt:	**IRQ 3**
Interface:	**RS232**

Options:

Port x:	**Speed:**	**Base I/O address:**	**Interrupt:**	**Interface:**
Disabled	Low	3F8	Disabled	RS232
Enabled	High	2F8	IRQ 3	RS422 RTS
		3E8	IRQ 4	RS422 Auto
		2E8	IRQ 5	RS485 RTS
			IRQ 6	RS485 RTS w/Echo
			IRQ 7	RS485 Auto
			IRQ 9	RS485 Auto w/Echo

Serial port 3:	**Enabled**
Speed:	**Low**
Base I/O address:	**3E8**
Interrupt:	**IRQ 5**
Interface:	**RS232**

Options:

Port x:	**Speed:**	**Base I/O address:**	**Interrupt:**	**Interface:**
Disabled	Low	3F8	Disabled	RS232
Enabled	High	2F8	IRQ 3	RS422 RTS
		3E8	IRQ 4	RS422 Auto
		2E8	IRQ 5	RS485 RTS
			IRQ 6	RS485 RTS w/Echo
			IRQ 7	RS485 Auto
				RS485 Auto w/Echo

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > Super I/O Control Sub-Menu (continued)

Serial port 4:	**Enabled**
Speed:	**Low**
Base I/O address:	**2E8**
Interrupt:	**IRQ 6**
Interface:	**RS232**

Options:

Port x:	**Speed:**	**Base I/O address:**	**Interrupt:**	**Interface:**
Disabled	Low	3F8	Disabled	RS232
Enabled	High	2F8	IRQ 3	RS422 RTS
		3E8	IRQ 4	RS422 Auto
		2E8	IRQ 5	RS485 RTS
			IRQ 6	RS485 RTS w/Echo
			IRQ 7	RS485 Auto
				RS485 Auto w/Echo

Parallel port:	**Enabled**
Base I/O address:	**378**
Interrupt:	**IRQ 7**

Options:

Port x:	**Base I/O address:**	**Interrupt:**
Disabled	378	Disabled
Enabled	278	IRQ 3
		IRQ 4
		IRQ 5
		IRQ 6
		IRQ 7
		IRQ 9
		IRQ 10
		IRQ 12

Digital I/O port:	**Enabled**
DIO port address:	**120**
DIO IRQ:	**IRQ 10**

Options:

Digital I/O port:	**DIO port address:**	**DIO IRQ:**
Disabled	120	Disabled
Enabled	130	IRQ 3
	140	IRQ 4
		IRQ 5
		IRQ 6
		IRQ 7
		IRQ 9
		IRQ 10
		IRQ 12

Watchdog:	**0**

Options:
{Enter any value between 0-255 for seconds.}

SIO Firmware:	Rev 0006

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > **ACPI Control Sub-Menu**	
Active Trip Point:	**55 C**
Options: Disabled 55 C 63 C 71 C 79 C 87 C 95 C 103 C 111 C 119 C	
Passive Cooling Trip Point:	**95 C**
Options: Disabled 55 C 63 C 71 C 79 C 87 C 95 C 103 C 111 C 119 C	
Passive TC1 Value:	**1**
Passive TC2 Value:	**5**
Options: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	
Passive TSP Value:	**10**
Options: 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Intel > **ACPI Control Sub-Menu** (continued)	
Critical Trip Point:	**POR**
Options: POR 15 C 23 C 31 C 39 C 47 C 55 C 63 C 71 C 79 C 87 C 95 C 103 C 111 C 119 C 127 C	
FACP - RTC S4 Flag Value:	**Enabled**
Options: Disabled Enabled	
FACP - PM Timer Flag Value:	**Enabled**
Options: Disabled Enabled	
HPET Support:	**Disabled**
Options: Disabled Enabled	

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Security	
Supervisor Password Is:	Clear
User Password Is:	Clear
Set Supervisor Password:	**Enter**
Set User Password:	Enter
Virus check reminder:	**Disabled**
Options: Disabled Daily Weekly Monthly	
Password on boot:	Disabled

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Boot

Boot priority order:

1:
2:
3:
4:
5:
6:
7:
8:

Options:

Excluded from boot order:

Options:
All IDE HDD
All USB Floppy
All USB KEY
All USB HDD
All USB CDROM
All USB ZIP
All USB LS120
All PCI BEV
Bootable Add-in Cards

Note: Defaults are indicated in **bold** for BIOS properties. Default options that cannot be user-modified are indicated with grey text.

Exit
Exit Saving Changes
Exit Saving Changes to CMOS and EEPROM
Exit Discarding Changes
Load Setup Defaults
Discard Changes
Save Changes

BIOS SETTINGS STORAGE OPTIONS

CMOS Storage Locations

The EPX-C380's BIOS configuration is stored in three (3) locations:

(1) CMOS RAM (nonvolatile if battery backed)

(2) EEPROM (nonvolatile storage for user defaults)

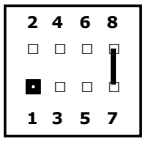
(3) FLASH PROM (nonvolatile storage for factory defaults)

Saving the CMOS Configuration

The Real-Time Clock and the CMOS RAM settings can be maintained by an optional battery when the board is powered off. A battery is always required to maintain time and date functions when the board is powered off.

The EEPROM feature allows the user to save CMOS configuration settings to nonvolatile storage that does not require a battery. This feature can be enabled/disabled using **JP4**. When enabled, the user's CMOS settings can be saved to EEPROM from the BIOS utility's Main Menu. If the board is powered off with no battery, the user's CMOS settings will be restored from EEPROM but time and date information will be lost and returned to default values.

JP4 - EEPROM



EEPROM Enable	
CMOS Register Reset	1-2
SPI BIOS Write Protect	3-4
SPI BIOS Program Enable	5-6
CMOS EEPROM Enable (default)	7-8
CMOS EEPROM Disable	7 8

At system boot, the BIOS first performs a checksum validation on the contents of the CMOS RAM. Invalid checksums usually occur due to a low or disabled battery. If the checksum is valid, the system boots using values stored in CMOS RAM. If a checksum error occurs, the BIOS attempts to load CMOS values from the EEPROM.

After a checksum validation, the BIOS configuration is loaded from the EEPROM and the boot process continues. If the EEPROM is disabled or the contents of the EEPROM fail the checksum validation, the system loads the factory default settings from the FLASH PROM and continues the boot sequence.

For applications where the battery is present, CMOS settings should be saved to both the CMOS RAM and to the EEPROM so the system can continue to function without user interaction.

Resetting CMOS to EEPROM defaults

If a battery is present, you can reset the CMOS RAM to the values stored in EEPROM by turning the system off and removing the external battery. Replace the battery and reboot. When power is applied to the board, the system will boot with the CMOS settings that were stored in EEPROM.

Resetting EEPROM to Factory Defaults

The EPX-C380 can normally be returned to the factory default BIOS configuration by selecting option Load Setup Defaults on the BIOS Exit menu.

If you have saved EEPROM values that prevent you from accessing BIOS menus, the board can be reset to factory defaults as follows:

1) Turn the system off.
2) Remove the jumper from pins 7-8 on **JP4**.
3) Turn the system on and enter the BIOS Main Menu using the **F2** key.
4) Select Load Defaults from the Exit menu.
5) Install the jumper on pins 7-8 on **JP4**.
6) Save the restored defaults to CMOS and EEPROM.

Updating the BIOS FLASH PROM

The most recent EPX-C380 BIOS is available on the WinSystems website. However, it is highly recommended that an Applications Engineer be consulted prior to any BIOS FLASH PROM update. If the BIOS PROM is updated, the steps described above must be followed to reset the CMOS and EEPROM to the newly loaded factory defaults and to clear the data from the previous BIOS version.

CABLES

Part Number	Description
CBL-SET-380-2	Cable set for EPX-C380 includes:
CBL-265-G-2-1.5	DC Harness, EPX, Unterminated
ADP-IO-G-EBC0364	Breakout PCB, Dual RJ-45 and 4 USB
CBL-USB4-002-12	4x USB ports with two, 8-pin, 2-mm connectors
CBL-ENET2-004-12	Ethernet 2x10 1.25-mm. to 2EA 2x6 2-mm. 12”
CBL-VGA-002-12	Video 1x14 1-mm. to DB15, 12”
CBL-SER4-002-12	Serial Cable 2x20, 1.25-mm. to 4EA DB9 12”
BAT-LTC-E-36-16-2	External 3.6V, 1650 mAH battery with plug-in connector
Additional Cables	
ADP-IO-G-EBC0364	Breakout PCB-Dual RJ-45 and 4 USB
ADP-IO-ENET-001	Dual 12-pin, 2-mm. to Dual RJ-45
ADP-IO-USB-001	Dual 8-pin, 2-mm. 4 USB ports
CBL-265-G-2-1.5	DC Harness, EPX, Unterminated
CBL-AUDIO2-102-12	Audio 2x15, 1.25-mm. to Jack, 12” Stereo Audio, UL1429
CBL-AUDIO5-102-12	Audio 2x15, 1.25-mm. to Jack, 12” 5.1 Audio, UL1429
CBL-AUDIO7-000-14	Audio 2x15, 1.25-mm. Unterminated, 14”
CBL-AUDIO7-102-12	Audio 2x15, 1.25-mm. to Jack, 12” 7.1 Audio, UL1429
CBL-BKLT-000-14	Backlight 1x11 1-mm., Unterminated Pico-Clasp
CBL-DIO24-001-12	DIO 2x25 1-mm. to 2x25 1-mm. 12”
CBL-DIO24-002-12	DIO Cable 2x25 1-mm. to 2x25 .1 CNTRS 12”
CBL-ENET2-001-12	Ethernet 2x10, 1.25-mm. to 2x10 1.25-mm. 12”
CBL-ENET2-002-12	Ethernet 2x10, 1.25-mm. to 2 x RJ-45 Female/Jack 12”
CBL-ENET2-003-12	Ethernet 2x10, 1.25-mm. to 2 x RJ-45 Males/Plug 12”
CBL-ENET2-004-12	Ethernet 2X10, 1.25-mm. to 2EA 2x6 2-mm. 12”
CBL-LED3-000-14	LED, Ethernet 1x4, 1-mm. Unterminated, 14”
CBL-LED3-001-12	LED, Ethernet 1x4, 1-mm. to 1x4 1-mm.
CBL-LPT-002-12	LPT Cable 2x15, 1-mm. to DB25 12”
CBL-LVDS24-000-14	LVDS 2x20, 1-mm. to Unterminated 14”
CBL-PWR-600-14	Power ATX and Reset, .1 Molex, 14” Unterminated
CBL-SER4-000-14	Serial Cable 2x20, 1.25-mm. Unterminated 14”
CBL-SER4-001-12	Serial Cable 2x20, 1.25-mm. to 2x20 1.25-mm. 12”
CBL-SER4-002-12	Serial Cable 2x20, 1.25-mm. to 4EA DB9 12”
CBL-USB4-000-14	USB 2x10, 1-mm. Unterminated 14”
CBL-USB4-001-12	USB 2 of 2x10-mm., Pico Clasp 12”
CBL-USB4-002-12	4x USB ports with two, 8-pin, 2-mm. connectors
CBL-VGA-002-12	Video 1x14, 1-mm. to DB15, 12”
External Batteries	
BAT-LTC-E-36-16-2	External 3.6V, 1600 mAH battery with plug-in connector
BAT-LTC-E-36-27-2	External 3.6V, 2700 mAH battery with plug-in connector

SOFTWARE DRIVERS

See WinSystems website.

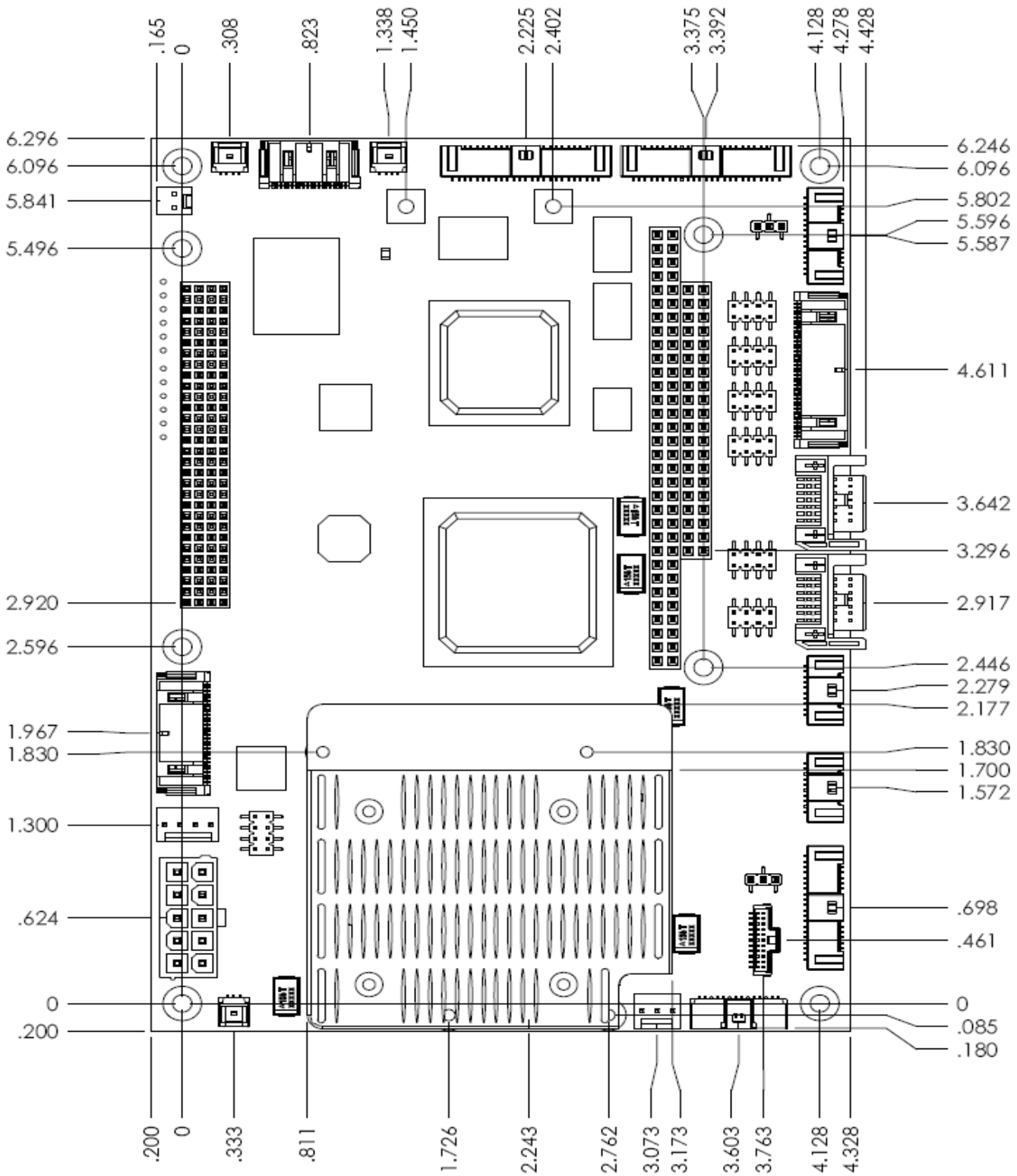
SPECIFICATIONS

Electrical		
VCC	+5V ±5% required, 2.5A typical	
	MODEL EPX-C380-S2-0	
Power	Typical	2.5A
	Maximum	2.94A
	Standby (S3)	268 mA
Mechanical		
Dimensions	4.50” x 6.50” (115 mm x 165 mm)	
Weight	9.6 oz (272.2g)	
Environmental		
Operating Temperature	-40°C to 85°C *	
Random Vibration	MIL-STD-202G, Method 214A, Condition D .1g/Hz (11.95g rms), 20 minutes per axis, 3 axis	
Mechanical Shock	MIL-STD-202G, Method 213B, Condition A 50g half-sine, 11 ms duration per axis, 3 axis	

* - Thermal profiles can also vary greatly depending on the operating system and applications being used. WinSystems uses the Intel TAT (Thermal Analysis Tool) for testing with Intel processors. This program heavily loads the system and creates a worst case scenario for the single board computer. Specific real world applications will rarely tax the system as heavily and may allow for extending the fanless operational range. WinSystems conducts temperature verification with PassMark BurnInTest to provide a more realistic real world example. The PassMark BurnInTest is performed with all internal tests operating at 50% duty cycle.

Thermal Qualification Testing						
SBC	**Test Application**	**Air Flow (linear ft/min)**	**Low Temp (Celsius)**	**High Temp (Celsius)**	**CPU Freq. (GHz)**	**CPU Throttling**
EPX-C380-S2-0	PassMark BurnInTest	150	-40	85	1.66	No
EPX-C380-S2-0	Intel TAT	150	-40	80	1.66	No
EPX-C380-S2-0	PassMark BurnInTest	0	-40	85	1.66	No
EPX-C380-S2-0	Intel TAT	0	-40	70	1.66	No
EPX-C380-D2-1	PassMark BurnInTest	Onboard Fan	-40	75	1.66	No
EPX-C380-D2-1	Intel TAT	Onboard Fan	-40	75	1.66	No

MECHANICAL DRAWING



EPX-C380 (TOP VIEW)

MECHANICAL DIMENSIONS ARE IN INCHES AND FOR REFERENCES ONLY

APPENDIX - A

BEST PRACTICES

POWER SUPPLY

The power supply and how it is connected to the Single Board Computer (SBC) is very important.

Avoid Electrostatic Discharge (ESD)
Only handle the SBC and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

Power Supply Budget
Evaluate your power supply budget. It is usually good practice to budget 2X the typical power requirement for all of your devices.

Zero-Load Power Supply
Use a zero-load power supply whenever possible. A zero-load power supply does not require a minimum power load to regulate. If a zero-load power supply is not appropriate for your application, then verify that the single board computer's typical load is not lower than the power supply's minimum load. If the single board computer does not draw enough power to meet the power supply's minimum load, then the power supply will not regulate properly and can cause damage to the SBC.

Use Proper Power Connections (Voltage)
When verifying the voltage, you should always measure it at the power connector on the SBC. Measuring at the power supply does not account for voltage drop through the wire and connectors.

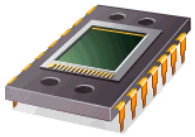
The single board computer requires +5V (±5%) to operate. Verify the power connections. Incorrect voltages can cause catastrophic damage.

Populate all of the +5V and ground connections. Most single board computers will have multiple power and ground pins, and all of them should be populated. The more copper connecting the power supply to the single board computer the better.

Adjusting Voltage
If you have a power supply that will allow you to adjust the voltage, it is a good idea to set the voltage at the power connector of the SBC to 5.1V. The SBC can tolerate up to 5.25V, so setting your power supply to provide 5.1V is safe and allows for a small amount of voltage drop that will occur over time as the power supply ages and the connector contacts oxidize.

Power Harness
Minimize the length of the power harness. This will reduce the amount of voltage drop between the power supply and the single board computer.

Gauge Wire
Use the largest gauge wire that you can. Most connector manufacturers have a maximum gauge wire they recommend for their pins. Try going one size larger; it usually works and the extra copper will help your system perform properly over time.



Contact Points
WinSystems' boards mostly use connectors with gold finish contacts. Gold finish contacts are used exclusively on high speed connections. Power and lower speed peripheral connectors may use a tin finish as an alternative contact surface. It is critical that the contact material in the mating connectors is matched properly (gold to gold and tin to tin). Contact areas made with dissimilar metals can cause oxidation/corrosion resulting in unreliable connections.

Pin Contacts
Often the pin contacts used in cabling are not given enough attention. The ideal choice for a pin contact would include a design similar to Molex's or Trifurcons' design, which provides three distinct points to maximize the contact area and improve connection integrity in high shock and vibration applications.

POWER DOWN

Make sure the system is **completely off/powered down** before connecting anything.

Power Supply OFF
The power supply should always be off before it is connected to the single board computer.

I/O Connections OFF
I/O Connections should also be off before connecting them to the single board computer or any I/O cards. Connecting hot signals can cause damage whether the single board computer is powered or not.

MOUNTING AND PROTECTING THE SINGLE BOARD COMPUTER

Do Not Bend or Flex the SBC
Never bend or flex the single board computer. Bending or flexing can cause irreparable damage. Single board computers are especially sensitive to flexing or bending around Ball-Grid-Array (BGA) devices. BGA devices are extremely rigid by design and flexing or bending the single board computer can cause the BGA to tear away from the printed circuit board.

Mounting Holes
The mounting holes are plated on the top, bottom and through the barrel of the hole and are connected to the single board computer's ground plane. Traces are often routed in the inner layers right below, above or around the mounting holes.

Never use a drill or any other tool in an attempt to make the holes larger.

Never use screws with oversized heads. The head could come in contact with nearby components causing a short or physical damage.

Never use self-tapping screws; they will compromise the walls of the mounting hole.

Never use oversized screws that cut into the walls of the mounting holes.

Always use all of the mounting holes. By using all of the mounting holes you will provide the support the single board computer needs to prevent bending or flexing.

Plug or Unplug Connectors Only on Fully Mounted Boards
Never plug or unplug connectors on a board that is not fully mounted. Many of the connectors fit rather tightly and the force needed to plug or unplug them could cause the single board computer to be flexed.

Avoid cutting of the SBC
Never use star washers or any fastening hardware that will cut into the single board computer.

Avoid Overtightening of Mounting Hardware
Causing the area around the mounting holes to compress could damage interlayer traces around the mouting holes.

Use Appropriate Tools
Always use tools that are appropriate for working with small hardware. Large tools can damage components around the mounting holes.

Placing the SBC on Mounting Standoffs
Be careful when placing the single board computer on the mounting standoffs. Sliding the board around until the standoffs are visible from the top can cause component damage on the bottom of the single board computer.

Avoid Conductive Surfaces
Never allow the single board computer to be placed on a conductive surface. Almost all single board computers use a battery to backup the clock-calendar and CMOS memory. A conductive surface such as a metal bench can short the battery causing premature failure.

ADDING PC/104 BOARDS TO YOUR STACK

Be careful when adding PC/104 boards to your stack.

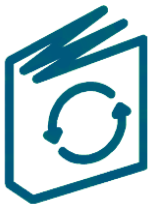
Never allow the power to be turned on when a PC/104 board has been improperly plugged onto the stack. It is possible to misalign the PC/104 card and leave a row of pins on the end or down the long side hanging out of the connector. If power is applied with these pins misaligned, it will cause the I/O board to be damaged beyond repair.

CONFORMAL COATING

Applying conformal coating to a WinSystems product will not in itself void the product warranty, if it is properly removed prior to return. Coating may change thermal characteristics and impedes our ability to test, diagnose, and repair products. Any coated product sent to WinSystems for repair will be returned at customer expense and no service will be performed.

OPERATIONS / PRODUCT MANUALS

Every single board computer has an Operations manual or Product manual.



Manual Updates
Operations/Product manuals are updated often. Periodicially check the WinSystems website (http://www.winsystems.com) for revisions.

Check Pinouts
Always check the pinout and connector locations in the manual before plugging in a cable. Many single board computers will have identical headers for different functions and plugging a cable into the wrong header can have disastrous results.

Contact an Applications Engineer with questions
If a diagram or chart in a manual does not seem to match your board, or if you have additional questions, contact your Applications Engineer.

APPENDIX - B

POST CODES

If the system hangs before the BIOS can process the error, the value displayed at the I/O port I/O address 80h is the last test that performed. In this case, the screen does not display an error code.

The following is a list of the checkpoint codes written at the start of each test and their corresponding audio beep codes issued for terminal errors.

Code	Beeps	Location	Description
01h			IPMI initialization
02h			Verify real mode
03h			Disable non-maskable interrupt (NMI)
04h			Get CPU type
06h			Hardware initialization
07h			Chipset BIOS deshadow
08h			Chipset initialization
09h			Set IN POST flag
0Ah			CPU initialization
0Bh			CPU cache on
0Ch			Cache initialization
0Eh			I/O initialization
0Fh			FDISK initialization
10h			Power management initialization
11h			Register initialization
12h			Restore CR0
13h			PCI bus master reset
14h			8742 initialization (keyboard/embedded controller)
16h	1-2-2-3	Checksum BIOS ROM	
17h			Pre-size RAM (initialize cache before memory auto size)
18h			Timer initialization (8254 CTC)
1Ah			DMA initialization (8237 DMAC)
1Ch			Reset PIC (8259 PIC)
20h	1-3-1-1	Test DRAM refresh	
22h	1-3-1-3		Test 8742 Keyboard Controller
24h			Set huge ES (segment register to 4 GB)
26h			Enable A20
28h			Auto size DRAM
29h			POST memory manager (PMM) initialization
2Ah			Zero base (clear 512 KB base RAM)
2Bh			Enhanced CMOS initialization
2Ch	1-3-4-1	Address test (RAM failure on address line **xxxx***)	
2Eh	1-3-4-3	Base RAM Low (RAM failure on data bits **xxxx*** of low byte)	
2Fh			Pre-sys shadow (Enable cache before system BIOS shadow)
30h			Base RAM High (RAM failure on data bits **xxxx*** of high byte)
32h			Compute speed (test CPU bus-clock frequency)
33h			Post Dispatch Manager (PDM) initialization
34h			CMOS test
35h			Register re-initialization
36h			Check shutdown (perform warm restart)

Code	Beeps	Location	Description
37h			Chipset re-initialization
38h			System shadow (shadow BIOS ROM)
39h			Cache re-initialization
3Ah			Cache auto-size
3Bh			Debug server initialization
3Ch			Advanced chipset initialization
3Dh			Advanced register configuration
3Eh			Read hardware
3Fh			RomPilot memory initialization
40h			Speed
41h			RomPilot initialization
42h			Interrupt vectors initialization
44h			Set BIOS interrupt
45h			Device initialization
46h	2-1-2-3	Check ROM copyright	
48h			Config (Check video configuration against CMOS)
49h			PCI initialization
4Ah			Video initialization (Initialize all video adapters)
4Bh			QuietBoot start
4Ch			Video shadow (Shadow video BIOS)
4Eh			Copyright display
4Fh			MultiBoot-XP initialization
50h			CPU type display
51h			EISA initialization
52h			Keyboard test
54h			Set key click (if enabled)
55h			USB initialization
56h			Enabled keyboard
57h			1394 Firewire initialization
58h	2-2-3-1	HOT (Test for unexpected interrupts)	
59h			POST display service (PDS) initialization
5Ah			Display prompt **Press F2 to enter SETUP**
5Bh			CPU cache off
5Ch			Test RAM between 512 KB to 640 KB
60h			Test extended memory
62h			Test extended memory address
64h			Jumper to UserPatch1
66h			Configure advanced cache registers
67h			Initialize Multi Processor APIC
68h			Cache configuration (enable internal and external caches)
69h			PM setup System Management Mode (SMM)
6Ah			Display external L2 cache size
6Bh			Load custom defaults (optional)
6Ch			Display shadow-area messages
70h			Display error messages
72h			Check for configuration errors

Code	Beeps	Location	Description
74h			RTC test
76h			Keyboard test
7Ah			Key lock
7Ch			Hardware interrupts
7Dh			Intelligent System Monitoring (ISM) initialization
7Eh			Coprocessor initialization (if present)
80h			I/O initialization (before)
81h			Late device initialization
82h			RS-232 initialization
83h			FDISK config IDE
84h			LPT initialization
85h			PCI PCC initialization (PC-compatible PnP ISA devices)
86h			I/O initialization (after)
87h			Motherboard Configurable Devices (MCD) initialization
88h			BIOS data-area initialization (BDA)
89h			Enable Non-Maskable Interrupt (NMI)
8Ah			Extended BIOS Extended Data Area (EBDA)
8Bh			Mouse initialization
8Ch			Floppy initialization
8Fh			FDISK fast pre-initialization
90h			FDISK initialization
91h			FDISK fast initialization
92h			Jump to UserPatch2
93h			Build MPTABLE for multi-processor boards
95h			CDROM initialization
96h			Clear huge ES
97h			MultiProcessor table fix-up
98h	1-2		Option ROM scan
99h			FDISK check SMART
9Ah			Miscellaneous shadow (shadow option ROMs)
9Bh			PM CPU speed
9Ch			Power Management (PM) setup
9Dh			Intialize security engine
9Eh			IRQS
9Fh			FDISK fast initialization #2
A0h			Time of day - set
A2h			Keylock test
A4h			Key rate initialization (typematic rate)
A8h			Erase F2 prompt
AAh			Scan for F2 keystroke
ACh			Setup check
AEh			Clear bootflag
B0h			Error check
B1h			RomPilot unload
B2h			POST done - prepare to boot operating system
B4h	1		One beep (before boot)

Code	Beeps	Location	Description
B5h			Terminate QuietBoot
B6h			Check password
B7h			ACPI initialization
B8h			System initialization
B9h			Prepare to boot
BAh			DMI - SMBIOS initialization
BBh			BCV (Boot Connection Vectors) initialization
BCh			Parity - clear parity checkers
BDh			MultiBoot-XP boot menu display
BEh			Clear screen
BFh			Check reminders (virus and backup)
C0h			INT19 - boot
C1h			POST Error Manager (PEM) - Initialization
C2h			POST Error Manager (PEM) - Logging initialization
C3h			POST Error Manager (PEM) - Initialize error display function
C4h			POST Error Manager (PEM) - Initialize system error handler
C5h			PNP'ed dual CMOS
C6h			Initialize note dock
C7h			Initialize note dock late
C8h			Force check
C9h			Extended checksum

Embedded Extensions	
Code	**Description**
CAh	TP_SERIAL_KEY - Redirect INT15h to serial keyboard
CBh	TP_ROMRAM - Redirect INT13h to Memory Technologies Devices Such as ROM, RAM, PCMCIA, and serial disk
CCh	TP_SERIAL_VID - Redirect INT10h to enable remote serial video
CDh	TP_PCMATA - Re-map I/O and memory for PCMCIA
CEh	TP_PEN_INIT - Initialize digitizer and display message
CFh	TP_XBDA_FAIL - Extended BIOS Data Area (XBDA) failure

More Post Codes	
Code	**Description**
D1h	TP_BIOS_STACK_INIT
D3h	TP_SETUP_WAD
D4h	TP_CPU_GET_STRING
D5h	TP_SWITCH_POST_TABLES
D6h	TP_PCCARD_INIT
D7h	TP_FIRSTWARE_CHECK
D8h	TP_ASF_INIT
D9H	TP_IPMI_INIT_LATE
DAh	TP_PCIE_INIT
DBh	TP_SROM_TEST
DCh	TP_UPD_ERROR
DDh	TP_REMOTE_FLASH
DEh	TP_UNDI_INIT
DFh	TP_UNDI_SHUTDOWN
E0h	TP_EFI_NV_INIT
E1h	TP_PERIODIC_TIMER

Boot Block	
Code	**Description**
80h	TP_BB_CS_INIT - Chipset Init
81h	TP_BB_BRIDGE_INIT - Bridge Init
82h	TP_BB_CPU_UNIT - CPU Init
83h	TP_BB_TIMER_INIT - System timer Init
84h	TP_BB_IO_INIT - System I/O Init
85h	TP_BB_FORCE - Check force recovery boot
86h	TP_BB_CHKSUM - Check BIOS Checksum
87H	TP_BB_GOTOBIOS - Go to BIOS
88h	TP_BB_MP_INIT - Init Multi Processor
89h	TP_BB_SET_HUGE - Set Huge Seg
8Ah	TP_BB_OEM_INIT - OEM Special Init
8Bh	TP_BB_HW_INIT - Init PIC and DMA
8Ch	TP_BB_MEM_TYPE - Init Memory Type
8Dh	TP_BB_MEM_SIZE - Init Memory Size
8Eh	TP_BB_SHADOW - Shadow Boot Block
8Fh	TP_BB_SMM_INIT - Init SMM
90h	TP_BB_RAMTEST - System Memory Test
91h	TP_BB_VECS_INIT - Init Interrupt Vectors
92h	TP_BB_RTC_INIT - Init RTC
93h	TP_BB_VIDEO_INIT - Init Video
94h	TP_BB_OUT_INIT - Init Beeper
95h	TP_BB_BOOT_INIT - Init Boot
96h	TP_BB_CLEAR_HUGE - Clear Huge Seg
97h	TP_BB_BOOT_OS - Boot to OS
98h	TP_BB_USB_INIT - Intialize the USB Controller
99h	TP_BB_SECUR_INIT - Init Security

***** If the BIOS detects error 2C, 2E, or 30 (base 512 KB RAM error), it displays an additional word-bitmap (**xxxx**) indicating the address line or bits that failed.

For example, “2C 0002” means address line 1 (bit one set) has failed. “2E 1020” means data bits 12 and 5 (bits 12 and 5 set) have failed in the lower 16 bits. Note that error 30 cannot occur on 386SX systems because they have a 16 rather than 32-bit bus. The BIOS also sends the bitmap to the port-80h LED display. It first displays the checkpoint code, followed by a delay, the high-order byte, another delay, and then the low-order byte of the error. It repeats this sequence continuously.

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(http://www.winsystems.com/warranty.cfm)

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