WINSYSTEMS®

SBC35-CC405

Industrial Intel® Atom™ SFF Computer with Expansion

Product Manual

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Revision History

Document Version	Last Updated Date	Brief Description of Change
v1.0	12/2016	Initial release
v1.1	7/29/2025	Updated Conformal Coating, added Warranty link, updated all links

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Table of Contents

1. Before You Begin

Review the warnings (in this section) and the best practice recommendations (see “Best Practices” on page 49) when using and handling the WinSystems SBC35-CC405. Adherence to these recommendations provides an optimal user experience and prevents damage. Read through this document and become familiar with the SBC35-CC405 before proceeding.

APPLYING CONFORMAL COATING AFTER PURCHASE WILL VOID YOUR WARRANTY. FAILING TO COMPLY WITH THESE BEST PRACTICES MAY DAMAGE THE PRODUCT AND VOID YOUR WARRANTY.

1.1 Warnings

Only qualified personnel should configure and install the SBC35-CC405. While observing the best practices, pay particular attention to the following:

Avoid Electrostatic Discharge (ESD)
Only handle the circuit board and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

Warning
Do not reverse the positive and negative terminals when you connect power to the unit. This will void the warranty and damage the board.

2. Introduction

This manual provides configuration and usage information for the SBC35-CC405. If you still have questions, contact Technical Support at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

Refer to the WinSystems website for other accessories (including cable drawings and pinouts) that can be used with your SBC35-CC405.

3. Functionality

The SBC35-CC405 is a high-performance, industrial, small form factor (SFF) Single Board Computer (SBC) capable of operating at high temperatures without a fan or heat-pipe. The processor for the unit is an Intel® E3800 series Atom™, integrated into the SBC35-CC405 using a Type 6 COM Express module. The low-profile thermal solution provides a rugged platform base that protects the PCB assembly and offers convenient four-point mounting. Information to configure and operate the SBC35-CC405 for most

applications is included in this User Manual or on our website at www.winsystems.com.

NOTE WinSystems can provide custom configurations for Original Equipment Manufacturer (OEM) clients. For details, please contact an Application Engineer through Technical Support (see contact information in the Introduction section on page 1).

4. Features

This section describes the features that are included with the SBC35-CC405.

Single Board Computer

- Single Board Computer
  - IO60 expansion connector
  - Stackable expansion
- Intel E3800 series Atom processor:

	SBC35-CC405-3815	SBC35-CC405-3827	SBC35-CC405-3845
Processor	Intel Atom E3815	Intel Atom E3827	Intel Atom E3845
Core Speed	1.46 GHz	1.75 GHz	1.91 GHz
Number of Cores	1	2	4
L2 Cache	512 KB	1 MB	2 MB

Operating Systems (compatibility)

- Microsoft Windows
- Linux
- Other x86-compatible systems

Memory

- 2 GB, 4 GB, or 8 GB DDR3L SDRAM

BIOS

- Phoenix SecureCore™

Video Interfaces

- Up to two active displays
- VGA up to 2560x1536 at 24 bits per pixel (bpp)
- Display port 1.1
- LVDS 18 or 24 bpp

Ethernet

- Two Intel® I210 Gigabit Ethernet (1 gigabit per second, GbE) controllers

Storage (Bootable)

- One SATA (2.0) channel
- One CFAST socket (on back of the board)
- One mSATA socket (MiniPCIe socket)

Serial Interface

- Two serial ports (RS-232/422/485)
- One USB 3.0 port
- Three USB 2.0 ports

Bus Expansion

- Two MiniPCIe (one supports mSATA, one supports USB 2.0)
- IO60 (SPI, I2C, PWM)

Audio

The SBC35-CC405 Intel® Atom E3800 family processor uses the Realtek ALC888S-VD codec controller that provides both Digital and Analog channels. The controller has three jack detection pins and a built-in beep generator. The SBC35-CC405 supports the following audio interfaces: one digital (Display Port 1.1), two analog (Stereo Audio, Line-In/Line-Out/Microphone), and one HD Audio (7.1 Surround). The Display Port 1.1 interface located at J15 also delivers video capability.

- HD Audio supported
- Interfaces: Display Port 1.1, Line Out, Line In, Mic to 3.5 mm, and 7.1 Surround

Power

- SBC35-CC405-3815: +10 to 50 V DC input (7 W typical, 9 W maximum)
- SBC35-CC405-3827: +10 to 50 V DC input (7.5 W typical, 10 W maximum)
- SBC35-CC405-3845: +10 to 50 V DC input (8.75 W typical, 12 W maximum)

Additional Features

- Watchdog timer from 1 second to 255 minutes (15,300 seconds) reset

Temperature

- Operating temperature: Fanless -40 °C to +85 °C (-40 °F to +185 °F); SBC35-CC405-3845 requires a minimum airflow of 200 LFPM above 80 °C (176 °F) if input voltage (V_{CC}) is above 24 V DC.
- Storage temperature: -50 °C to +95 °C (-58 °F to +203 °F)

5. Specifications

The SBC35-CC405 adheres to the following specifications and requirements.

SBC35-CC405 Specifications

Electrical	
V_{CC}	10 to 50 V DC ±5%, 15 Watts (maximum)
MTBF	14.5 Years
Battery: CR-2032	Chemical System: Li/MnO_2 Nominal Voltage: 3 V Rated Capacity: 225 mAh
Mechanical	
Dimensions	4 x 6.125 x 2.3 inches (102 x 165 x 58 mm)
Weight	1.40 lbs. (635 g) with heat sink
PCB thickness	0.078 inch
Environmental	
Temperature	-40 °C to +85 °C (-40 °F to +185 °F)
Humidity (RH)	5% to 95% non-condensing
Mechanical Shock Testing	MIL-STD-202G, Method 213B, Condition A 50g half-sine, 11 ms duration per axis, 3 axis
Random Vibration Testing	MIL-STD-202G, Method 214A, Condition D .1g/Hz (11.95g rms), 20 minutes per axis, 3 axis
RoHS Compliant	Yes
Operating Systems	
Runs 32/64-bit Windows, Linux, and other x86-compatible operating systems.	

5.1 Additional Accessories

A standoff kit part number, KIT-IO60-STANDOFF-2, is included for use with the SBC35-CC405. The kit contains the following items:

Component	Description	Qty
Standoff	Aluminum, 5 mm HEX,12 mm Long, 3.5 mm thread, Male/Female	2
Hex Nut	Zinc Finish, M3-0.5 DIN	2
Screw	Stainless Steel, M3 x 0.5 mm x 6 mm PPH	2

6. Setup

Use the information in Section 7 to help locate and identify the connectors outlined in the following steps.

6.1 Installation and Connections

1. Connect a compatible monitor to the VGA output at J21, the Display port at J15, or the LVDS and Backlight connector at J12, depending on your preference and capabilities.

NOTE If you are using a flat panel display, make sure the jumper for Backlight Power at JP7 is installed as required. See “Backlight Power (JP7)” on page 28 for specific requirements.

NOTE If you are using a flat panel display (connector J12), configure the panel orientation, LVDS configuration, and bits per pixel to your preferences/requirements. For more information, see “Panel Orientation (JP6)” on page 28; “LVDS Configuration (JP5)” on page 27; and “Bits Per Pixel (JP4)” on page 27.

2. Connect a USB keyboard to any one of the four USB ports at J11 or J13.
3. Plug in the boot media of your preference. The options are:
   - CFAST (J103 – on the back of the board)
   - MSATA (J9)
   - External SATA (J3)
   - USB (J11 or J13)
   - Ethernet (LAN boot – requires special CMOS settings)
4. Set the jumper at JP3 (Battery Select) for the type of battery backup to be used (optional).
   - Internal battery backup (Default) (jumper pins 2 & 3)
   - No battery backup (no jumper installed)
   - Optional external battery backup (jumper pins 1 & 2)
5. If using an external battery backup, connect the battery to J7.
6. Connect an Ethernet cable to either of the ports at J11 or J13.

6.2 Power up

Plug in a compatible +10 to +50 V DC power source at J5. The first time power is applied, the SBC35-CC405 will boot automatically, bypassing the power button (SW1). After initial startup, briefly press the power button to turn the SBC35-CC405 on and off.

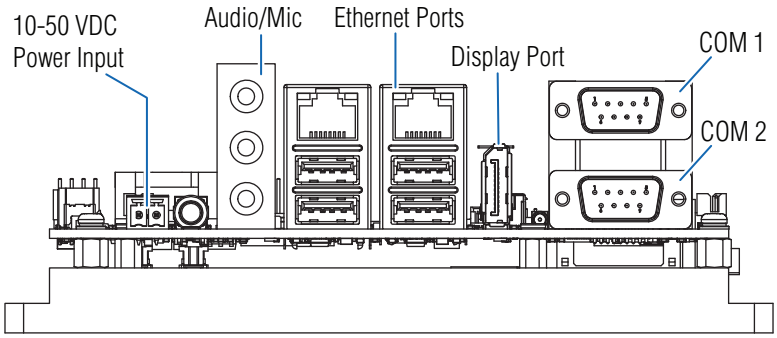
7. Configuration

This section describes the SBC35-CC405 components and configuration.

7.1 Component Layout

The SBC35-CC405 provides components on the edge, top, and bottom of the board. Edge connections provide common external connections.

7.1.1 Edge Connections



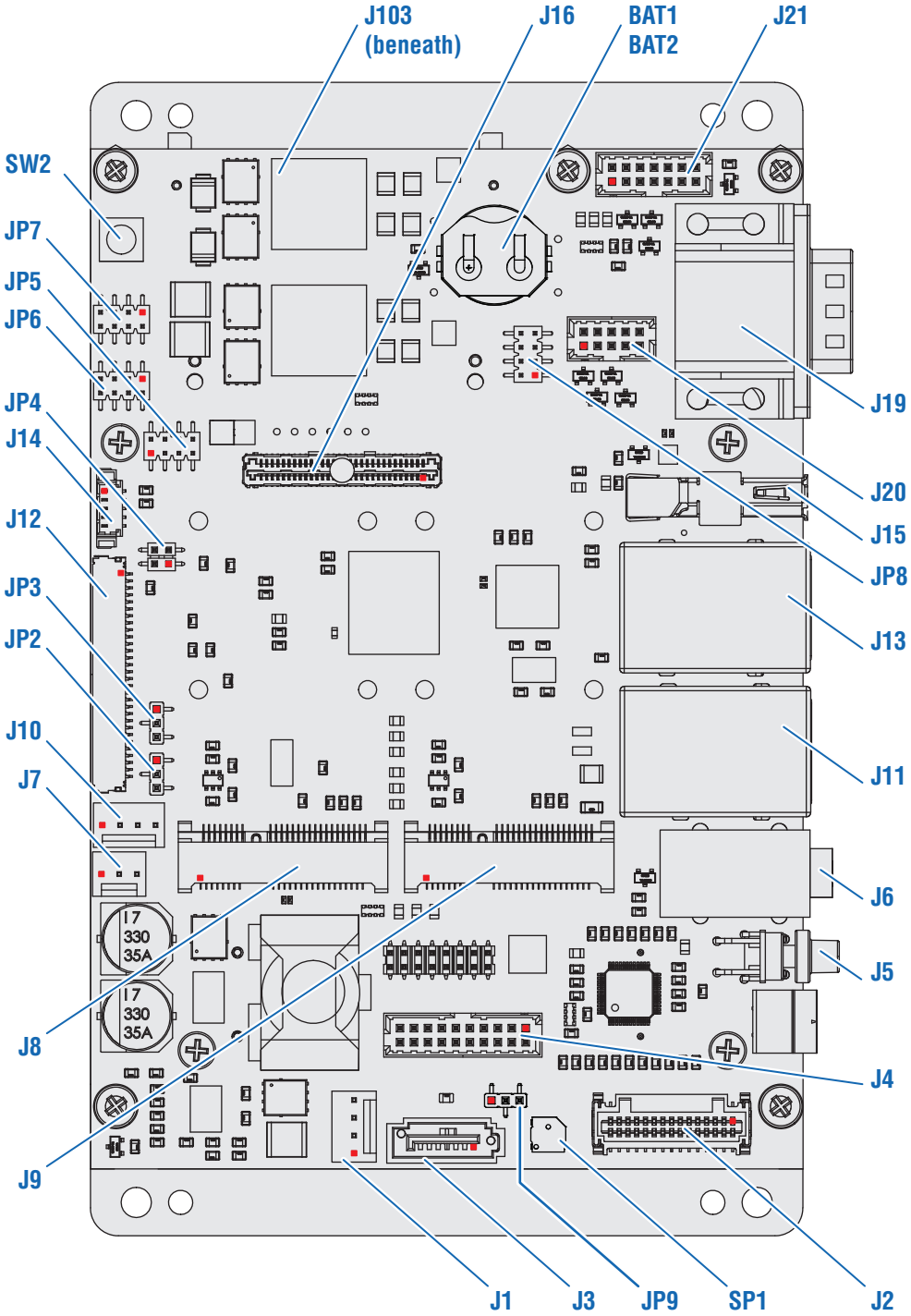
Edge Connections:

Connection	Reference
Power Input (J5)	page 15
Stereo Audio: Line-In, Line-Out, and Microphone (J6)	page 16
Ethernet (Top Half of Connectors J11 and J13)	page 19
USB Channels 1 and 3 (J11) and Channels 2 and 4 (J13)	page 21
Display Port 1.1 (J15)	page 22
COM 1 and COM 2 (J19A and J19B)	page 24

7.1.2 Top View Components

The following figure illustrates the location of each connector, jumper, and switch on the top of the SBC35-CC405. (Connector J103 is on the bottom of the board.)

Pin 1 of each connector or jumper is indicated by a red square in the figure.



Top View Connectors

The following table provides connector descriptions and references for the figure on page 7 (“Top View Components”).

Item	Description	Reference
J1	SATA Power	page 12
J2	HD Audio 7.1 Surround	page 13
J3	Serial ATA	page 14
J4	System Management	page 14
J5	Power Input	page 15
J6	Stereo Audio: Line-In, Line-Out, and Microphone	page 16
J7	External Battery Connector	page 16
J8	MiniPCIe	page 17
J9	MiniPCIe/MSATA	page 17
J10	External Fan Connector	page 19
J11	Ethernet (top half of connector)	page 19
J11	USB Channels 1 and 3 (bottom half of connector)	page 20
J12	LVDS and Backlight	page 21
J13	Ethernet (top half of connector)	page 19
J13	USB Channels 2 and 4 (bottom half of connector)	page 20
J14	USB Touchscreen	page 21
J15	Display Port 1.1	page 22
J16	IO60 Expansion	page 23
J19	COM 1 and COM 2	page 24
J20	Ethernet GPIO Controller	page 24
J21	Analog VGA	page 25
J103	CFAST (bottom of board)	page 25

Top View Jumpers

The following table provides jumper descriptions and references for the figure on page 7 (“Top View Components”).

Item	Description	Reference
JP2	Fan Voltage Output	page 26
JP3	Battery Select	page 27
JP4	Bits Per Pixel	page 27
JP5	LVDS Configuration	page 27
JP6	Panel Orientation	page 28
JP7	Backlight Power	page 28
JP8	Ethernet GPIO Reference Voltage Selection	page 29
JP9	Basic Input/Output System (BIOS) Programming Defaults	page 29

Top View Switches

The following table provides switch descriptions and references for the figure on page 7 (“Top View Components”).

Item	Description	Reference
SW1	Power Button	page 29
SW2	Reset Button	page 30

BAT1/BAT2

The SBC35-CC405 uses a single CR-2032 or CR-2025 battery. The nominal voltage of either battery is 3.0 V. This battery, or alternatively an external battery connected to the SBC35-CC405 board, provides standby power for the real-time clock and optional GPS. See “Battery Select (JP3)” on page 27 and “External Battery Connector (J7) (Optional)” on page 16 for more information.

7.2 Power

The SBC35-CC405 draws power through the J5 connector (see “Power Input (J5)” on page 15). The main supply to the board is +10-50 V DC.

7.3 Watchdog Timer

The SBC35-CC405 features an advanced watchdog timer (WDT) that can be used to guard against software lockups. The timer is programmable from 1 second to 255 minutes.

NOTE Use a long timeout if the watchdog is enabled when trying to boot any operating system.

The watchdog can be enabled, disabled, or reset by writing the appropriate values to the configuration registers. The WDT is part of the embedded controller, which uses the following command sequence:

CMD Register: 0x66

Read Command: 0x80

Write Command: 0x81

Sync Command: 0x82

DATA Register: 0x62

The watchdog timer initialization requires that the CMD register be cleared and then configured to write the command, and then the data written. Example code for C and Basic are provided following the tables.

Watchdog Timer Control Register	
Offset Address: 0x06, Attribute: R/W, Size: 8 bit	
Bit	Description
7	Reserved
6	WDT event reset Software writes a 1 to this bit to clear the WDT event.
5:4	Watchdog Timer Output Modes. 00: Generating an internal reset and WDT pin is driven high until the unit resets. 01: Driving WDT pin high until cleared by software.
3:2	Reserved.
1	Select WDT count mode. 0: Second Mode. 1: Minute Mode.
0	Disable / Enable the WDT function. 0: Disable 1: Enable

Watchdog Timer Control Register for Minutes	
Offset Address: 0x07, Attribute: R/W, Size: 8 bit	
Bit	Description
7:0	Timer Counter Register (Minutes) Watchdog timer time-out value in minutes (Default value = 0x00)

Watchdog Timer Control Register for Seconds	
Offset Address: 0x08, Attribute: R/W, Size: 8 bit	
Bit	Description
7:0	Timer Counter Register (Seconds) Watchdog timer time-out value in minutes (Default value = 0x00)

7.3.1 Example code (C WDT)

The following code example for the watchdog timer is written in C:

```
Offset = [Register]
Value = [Data]

VOID  Write_EC_SRAM(UINT8 Offset,UINT8 Value){
       UINT8  tmp,count;
       count=100;
       do{
              IoWrite8(0x66,0x82);
              pBS->Stall(1000); //uint=1us
              tmp=IoRead8(0x62);
              count--;
       }while (((tmp&0x10)==0) & (count>0));

       IoWrite8(0x66,0x81);
       Delay1MS(1);
       IoWrite8(0x62,Offset);
       Delay1MS(1);
       IoWrite8(0x62,Value);
}

int  Read_EC_SRAM(UINT8 Offset){
       UINT8  tmp,count;
       count=100;
       do{
              IoWrite8(0x66,0x82);
              pBS->Stall(1000); //uint=1us
              tmp=IoRead8(0x62);
              count--;
       }while (((tmp&0x10)==0) & (count>0));

       IoWrite8(0x66,0x80);
       Delay1MS(1);
       IoWrite8(0x62,Offset);
       Delay1MS(1);
       IoRead8(0x62,Value);
       return Value;
}
```

7.3.2 Example Code: Basic

The following code example for the watchdog timer is written in Basic:

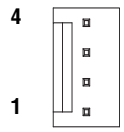
```
3 PRINT TIME$;" ";DATE$
4 O=VAL(RIGHT$(TIME$,2))
5 C=&H66:D=&H62:W=&H81:R=&H80:TRON
6 P=INP(C): IF (P=0) THEN GOTO 10 ELSE IF (P=1) THEN PRINT INP(D) ELSE
IF (P=8) THEN  OUT D,6: GOTO 200
7 GOTO 6
9 REM write reg 08 with 05
10 TROFF
11 IF (INP(C)=0) THEN OUT C,W ELSE GOTO 11
20 IF (INP(C)=8) THEN OUT D,8 ELSE GOTO 20
30 IF (INP(C)=0) THEN OUT D,O ELSE GOTO 30
39 REM enable dog
40 IF (INP(C)=0) THEN OUT C,W ELSE GOTO 40
50 IF (INP(C)=8) THEN OUT D,6 ELSE GOTO 50
60 IF (INP(C)=0) THEN OUT D,1 ELSE GOTO 60
69 REM read counter
70 IF (INP(C)=0) THEN OUT C,R ELSE GOTO 70
80 IF (INP(C)=8) THEN OUT D,8 ELSE GOTO 80
90 IF (INP(C)=1) THEN T=INP(D) ELSE GOTO 90
100 IF (T<>T2) THEN PRINT T;: T2=T
110 FOR X=1 TO 10000: NEXT: GOTO 70
200 IF (INP(C)=1) THEN PRINT INP(D);"*" ELSE GOTO 200
210 GOTO 10
```

7.4 Connectors

7.4.1 SATA Power (J1)

Power is supplied to the SATA device via the connector at J1.

Layout and Pin Reference:



Pin	Name
1	+5 V
2	GND
3	GND
4	+12 V

WinSystems cable CBL-PWR-117-12 simplifies this connection to the board.

Additional Information

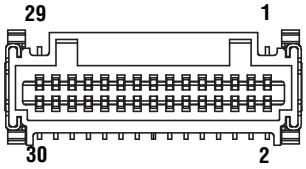
This connection is a Molex 22-11-2042.

7.4.2 HD Audio 7.1 Surround (J2)

The HD Audio connection delivers audio output depending on the cable used:

- WinSystems Cable CBL-AUDIO7-102-12: delivers 7.1 (surround sound) audio
- WinSystems Cable CBL-AUDIO5-102-12: delivers 5.1 audio
- WinSystems Cable CBL-AUDIO3-102-12: delivers stereo audio

Layout and Pin Reference:



Pin	Name	Pin	Name
1	OUT-R	2	MIC1-REAR-R
3	OUT-L	4	MIC1-REAR-L
5	ADGND	6	ADGND
7	SUR-R	8	MIC2-REAR-R
9	SUR-L	10	MIC2-REAR-L
11	ADGND	12	ADGND
13	CENTER	14	LINE-R
15	LFE	16	LINE-L
17	ADGND	18	ADGND
19	SIDE-R	20	CD-R
21	SIDE-L	22	CD-L
23	ADGND	24	CDGND
25	HEADPHONE-R	26	ADGND
27	HEADPHONE-L	28	ADGND
29	ADGND	30	ADGND

Additional Information

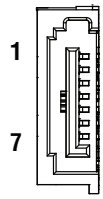
This connection is a Molex 501931-3070.

7.4.3 Serial ATA (J3)

The bootable SATA (2.0) interface is located at J3. WinSystems offers CBL-SATA-701-20 for this connector.

NOTE J3 cannot be used when J9 mSATA is present.

Layout and Pin Reference:



Pin	Name
1	GND
2	RX1+
3	RX1-
4	GND
5	TX1-
6	TX1+
7	GND

7.4.4 System Management (J4)

System management functions and events use J4 for connectivity from the SBC and CPU to the rest of the system. This enables the SBC and System to properly notify and respond to Power, Sleep/Wake, Thermal, and Security events.

The SPI and I2C interfaces on this connector can also be used for additional system connectivity such as enclosure management, SMBus, or PMBus connectivity.

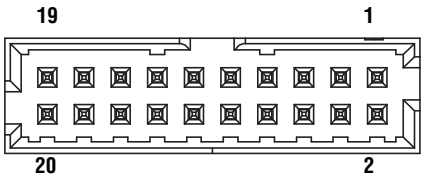
Pin 2 (LID#) indicates whether the system is on/off or opened/closed, and can be used for an intruder alert. If this bit is set, you can wire it to your system to initiate a system shutdown.

Optionally, you can use J4 to initiate sleep mode via Pin 3.

Pin 4 indicates thermal trip status. You can be notified of a thermal trip, and action (such as a system shutdown) is taken in response to the system overheating. More information regarding thermal protection signaling is provided in the table below.

Thermal Protection	Pin	Power Rail	Description
THRM#	6	3.3 V / 3.3 V	Input from off-Module temp sensor indicating an over-temp situation.
THRMTRIP#	4	3.3 V / 3.3 V	Active low output indicating that the CPU has entered thermal shutdown.

Layout and Pin Reference:



Pin	Name	Pin	Name
1	PWRBTN	2	LID#
3	SLEEP	4	THRMTRIP#
5	I^2C_CLK	6	THRM#
7	I^2C_DAT	8	WAKE
9	SYS_RESET	10	NC
11	SPI_PWR	12	VCC_5V
13	SPI_MISO	14	VCC_3.3V
15	SPI_CLK	16	GND
17	SPI_MOSI	18	GND
19	SPI_CS5	20	GND

7.4.5 Power Input (J5)

The SBC35-CC405 is capable of operating from +10 to +50 VDC (+/-5%). The green power input connector (J5) is located next to the power button on the edge of the board.

Warning
Do not reverse the positive and negative terminals when you connect power to the unit. This will void the warranty and damage the board.

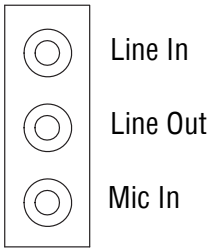
Power Connector (J5)	Power Button (SW1)
	

Additional Information

This connection is a Phoenix 1803277.

7.4.6 Stereo Audio: Line-In, Line-Out, and Microphone (J6)

The SBC35-CC405 uses 3.5 mm stereo line-in, line-out, and microphone jacks at J6.



7.4.7 External Battery Connector (J7) (Optional)

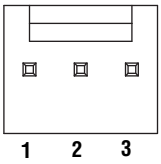
An external battery connected to the SBC35-CC405 board provides standby power for the real-time clock, CMOS, and optional GPS.

Extended temperature lithium batteries are available from WinSystems, part numbers:

- BAT-LTC-E-36-16-1
- BAT-LTC-E-36-27-1

The on-board battery is the default configuration on this product. The external battery is optional.

Layout and Pin Reference:

	Pin	Name
	1	GND
	2	VBAT
	3	GND

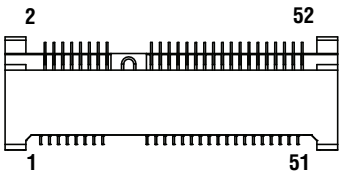
Additional Information

This connection is a Molex 22-11-2032.

7.4.8 MiniPCIe (J8)

The SBC35-CC405 includes a MiniPCIe socket at J8.

Layout and Pin Reference:

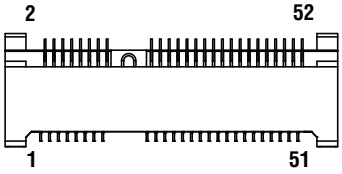


Pin	Name	Pin	Name
1	WAKE#	2	3.3Vaux
3	NC	4	GND
5	NC	6	1.5V
7	CLKREQ#	8	NC
9	GND	10	NC
11	REFCLK-	12	NC
13	REFCLK+	14	NC
15	GND	16	NC
Mechanical Key			
17	NC	18	GND
19	NC	20	W_DISABLE#
21	GND	22	PERST#
23	PERn0	24	+3.3Vaux
25	PERp0	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PETn0	32	SMB_DATA
33	PETp0	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	+3.3Vaux	40	GND
41	+3.3Vaux	42	LED_WWAN#
43	GND	44	LED_WLAN#
45	NC	46	LED_WPAN#
47	NC	48	+1.5V
49	NC	50	GND
51	NC	52	+3.3Vaux
NC = Not Connected			

7.4.9 MiniPCIe with SATA Support (J9)

The SBC35-CC405 includes a MiniPCIe socket at J9. The socket automatically detects mSATA, providing a bootable media and storage interface.

Layout and Pin Reference:



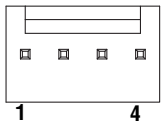
Pin	Name	Pin	Name
1	WAKE#	2	3.3Vaux
3	NC	4	GND
5	NC	6	1.5V
7	CLKREQ#	8	NC
9	GND	10	NC
11	REFCLK-	12	NC
13	REFCLK+	14	NC
15	GND	16	NC
Mechanical Key			
17	NC	18	GND
19	NC	20	W_DISABLE#
21	GND	22	PERST#
23	PERn0	24	+3.3Vaux
25	PERp0	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PETn0	32	SMB_DATA
33	PETp0	34	GND
35	GND	36	NC
37	GND	38	NC
39	+3.3Vaux	40	GND
41	+3.3Vaux	42	LED_WWAN#
43	GND	44	LED_WLAN#
45	NC	46	LED_WPAN#
47	NC	48	+1.5V
49	NC	50	GND
51	mSATA_DET	52	+3.3Vaux
NC = Not Connected			

7.4.10 External Fan Connector (J10)

The fan voltage output of this connector is determined by the jumper configuration on JP2.

NOTE A fan is not provided with the SBC35-CC405.

Layout and Pin Reference:



Pin	Name
1	FAN_PWM
2	FAN_TACH
3	FAN_VCC
4	GND

Additional Information

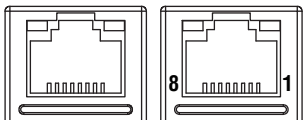
This connection is a Molex 22-11-2042.

7.4.11 Ethernet (Top Half of Connectors J11 and J13)

Two Intel I210 Gigabit Ethernet controllers provide standard IEEE 1588 and 802.1AS protocol timestamping. Each Ethernet interface includes 10/100/1000 MP/s multispeed, full, and half-duplex operation.

The pinout below describes both of the standard RJ45 Ethernet connectors.

Layout and Pin Reference:



Pin	Function	Description
1	TX_D1+	Transceive Data+
2	TX_D1-	Transceive Data-
3	RX_D2+	Receive Data+
4	BI_D3+	Bi-Directional Data+
5	BI_D3-	Bi-Directional Data-
6	RX_D2-	Receive Data-
7	BI_D4+	Bi-Directional Data+
8	BI_D4-	Bi-Directional Data-

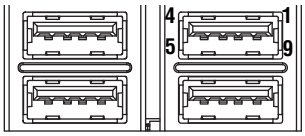
On-board Ethernet activity LEDs are built into the connectors at J11 & J13. There is one green LED (left) and one bi-color green/yellow LED (right).

LED	Activity	Ethernet Status
Left	Off	No Link
	Flashing (green)	Linked
Right	Off	No Link
	Off	Linked at 10 MB
	On (yellow)	Linked at 100 MB
	On (green)	Linked at 1 GB

7.4.12 USB Channels 1 and 3 (J11) and Channels 2 and 4 (J13)

J11 provides USB 3.0 on the bottom port (CH3) and USB 2.0 on the top port (CH1). J13 provides USB 2.0 on both ports (CH2 & CH4).

Pin Reference:

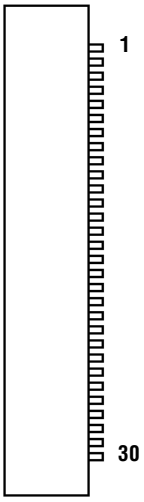


Pin	USB 3.0	USB 2.0
1	USBVCC	
2	D-	
3	D+	
4	GND	
5	RX-	Not Present
6	RX+	
7	GND	
8	TX-	
9	TX+	

7.4.13 LVDS and Backlight (J12)

The SBC35-CC405 supports LVDS flat panel displays with resolutions up to 1920x1200 at 24 bpp.

Layout and Pin Reference:



Pin	Name	Pin	Name
1	3.3 V	2	3.3 V
3	GND	4	SEL68
5	D0-	6	D0+
7	GND	8	D1-
9	D1+	10	GND
11	D2-	12	D2+
13	GND	14	CLK-
15	CLK+	16	GND
17	U/D	18	L/R
19	D3-	20	D3+
21	I^2C_CLK	22	I^2C_DATA
23	GND	24	GND
25	BLK_CLK	26	BLK_DATA
27	BLKEN	28	BLKPWM
29	BKLVCC	30	BKLVCC
Non-shaded cells designate LVDS interface.			
Shaded cells designate Backlight Interface.			

Additional Information

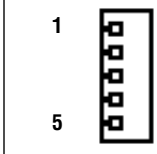
WinSystems cables simplify connections from supported displays to the board:

Display	WinSystems Cable
7” 800x480 AMPIRE AM-800480R3TMQW-TA1H	CBL-LVDSB-203-24A
12.1” 1024x768 AUO G121XN01 V0	CBL-LVDSB-202-24A

7.4.14 USB Touchscreen (J14)

J14 (USB 5) provides Plug-and-Play support for a USB Touchscreen. Aside from a simpler and faster interface, it also provides power within the USB cable, eliminating the need for a separate, dedicated cable to power the touchscreen.

Layout and Pin Reference:



Pin	Name
1	Ground
2	VCC5_SB
3	USB5_P
4	USB5_N
5	Ground

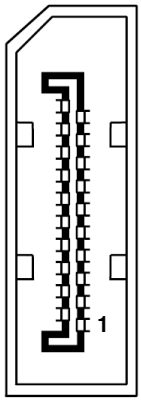
Additional Information

This connection is a Molex 53398-0571.

7.4.15 Display Port 1.1 (J15)

The Display Port 1.1 connector supplies both video and high definition (HD) audio. See the (XREF: Audio) section for more information.

Layout and Pin Reference:

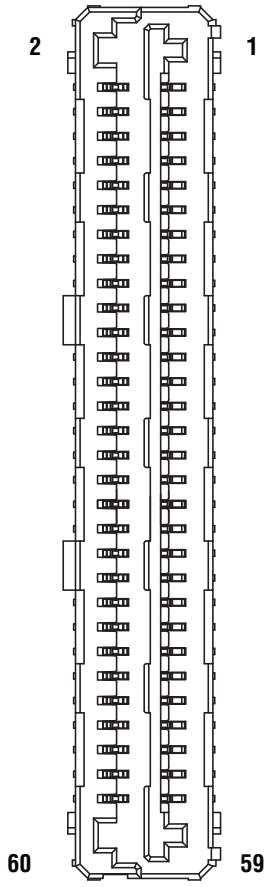


PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	ML_Lane 0 (p)	Lane 0 (positive)	2	GND	Ground
3	ML_Lane 0 (n)	Lane 0 (negative)	4	ML_Lane 1 (p)	Lane 1 (positive)
5	GND	Ground	6	ML_Lane 1 (n)	Lane 1 (negative)
7	ML_Lane 2 (p)	Lane 2 (positive)	8	GND	Ground
9	ML_Lane 2 (p)	Lane 2 (negative)	10	ML_Lane 3 (p)	Lane 3 (positive)
11	GND	Ground	12	ML_Lane 3 (n)	Lane 3 (negative)
13	CONFIG1	CONFIG1	14	CONFIG2	CONFIG2
15	AUX_CH (p)	Auxiliary Channel (positive)	16	GND	Ground
17	AUX_CH (n)	Auxiliary Channel (negative)	18	Hot Plug	Hot Plug Detect
19	RETURN	Return for Power	20	DP_PWR	Power for connector (3.3 V 500 mA)

7.4.16 IO60 Expansion (J16)

The expansion bus allows mezzanine cards to provide additional functionality.

Layout and Pin Reference:



Pin	Name	Pin	Name
1	VCC5	2	VCC5
3	VCC5	4	VCC5
5	UART_TX	6	UART_RX
7	UART_RTS	8	UART_CTS
9	GND	10	UART-MUX_CTL
11	SPI_CLK	12	SPI_MISO
13	SPI_C0	14	SPI_MOSI
15	SPI_CS1	16	SPI_CS2
17	SPI_CS3	18	SPI_RDY
19	GND	20	GND
21	I2C_SCL	22	I2C_SDA
23	GND	24	GND
25	PWM	26	EPIT1
27	GND	28	GND
29	POR	30	GPIO_0
31	GPIO_1	32	GPIO_2
33	GPIO_3	34	GPIO_4
35	GPIO_5	36	GPIO_6
37	GPIO_7	38	GPIO_8
39	GND	40	GND
41	RSVD1	42	RSVD2
43	RSVD3	44	RSVD4
45	GND	46	GND
47	RSVD5	48	RSVD6
49	RSVD7	50	RSVD8
51	GND	52	GND
53	RSVD9	54	RSVD10
55	RSVD11	56	RSVD12
57	VCC3.3	58	VCC3.3
59	VCC3.3	60	VCC3.3

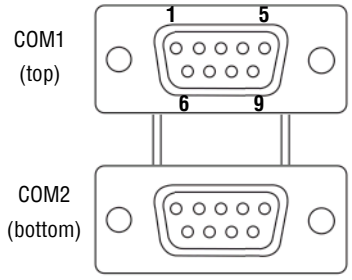
Additional Information

This connection is a SAMTEC LSEM-130-06.0-L-DV-A-N-K-TR.

7.4.17 COM 1 and COM 2 (J19A and J19B)

The SBC35-CC405 is equipped with two on-board serial ports (RS-232/422/485) at J19. Both serial channels use the advanced EXAR SP339E multiprotocol transceiver. Both ports are configured in the BIOS and include options for 120-ohm receiver termination, slew rate, and protocol.

Layout and Pin Reference:

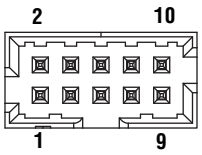


Pin	RS-232	RS-422	RS-485
1	DCD	N/A	N/A
2	RX	TX+	TX/RX+
3	TX	RX+	N/A
4	DTR	N/A	N/A
5	GND	GND	GND
6	DSR	TX-	TX/RX-
7	RTS	RX-	N/A
8	CTR	N/A	N/A
9	RI	N/A	N/A

7.4.18 Ethernet GPIO Controller (J20)

The SBC35-CC405 is equipped with an Ethernet GPIO connector at J20 that is associated with Ethernet port 2 at J13. Reference power to J20 is controlled by jumper settings on JP8.

Layout and Pin Reference:



Pin	Function
1	GPIO0
2	GND
3	GPIO1
4	GND
5	GPIO2
6	GND
7	GPIO3
8	GND
9	VDD IO
10	GND

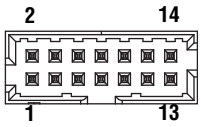
Additional Information

This connection is a Molex 87832-1021.

7.4.19 Analog VGA (J21)

The SBC35-CC405 supports analog VGA. The required cable is available from WinSystems, part number CBL-234-G-1-1.375C.

Layout and Pin Reference:



Pin	Name	Pin	Name
1	Red	2	Ground
3	Green	4	Ground
5	Blue	6	Ground
7	HSYNC	8	Ground
9	VSYNC	10	Ground
11	DDCDATA	12	Ground
13	DDCCLK	14	VCC

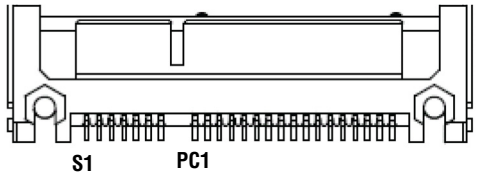
Additional Information

This connection is a Molex 87832-1420.

7.4.20 CFAST (SATA SSD) (J103)

The SBC35-CC405 supports CFAST storage at J103 located on the back of the board. CFAST is a small form factor SATA SSD.

Layout and Pin Reference:



PIN	CFAST	DESCRIPTION	PIN	CFAST	DESCRIPTION
S1	SGND	Signal Ground	PC5	NC	No Connect
S2	A+	SATA Pair A	PC6	NC	No Connect
S3	A-		PC7	GND	Ground
S4	SGND	Signal Ground	PC8	LED1	LED Output
S5	B-	SATA Pair B	PC9	LED2	LED Output
S6	B+		PC10	IO1	Reserved
S7	SGND	Signal Ground	PC11	IO2	Reserved
Key			PC12	IO3	Reserved
Key			PC13	3.3 V	Power
PC1	CDI	Card Detect In	PC14	3.3 V	Power
PC2	GND	Ground	PC15	GND	Ground
PC3	NC	No Connect	PC16	GND	Ground
PC4	NC	No Connect	PC17	GND	Card Detect Out

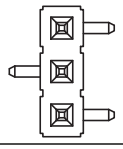
7.5 Jumpers

7.5.1 Fan Voltage Output (JP2)

The presence and position of a jumper at JP2 specifies the voltage for external fan connector J10. The default position is open (no jumper), indicating that no power is provided to an external fan. In position **1-2**, +5 VDC is selected. In position **2-3,** +12 VDC is selected.

Purpose: Determining voltage for an external fan connected at J10.

Jumper Pin Reference:

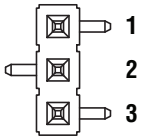
	Jumper	Voltage output
	1-2	5 VDC
	2-3	12 VDC
	open	No power

7.5.2 Battery Select (JP3)

The presence and position of a jumper at JP3 specifies whether a battery is connected at J7 and whether it is an external or internal battery. The default position is **2-3**, an internal battery is connected. In position **1-2**, an external battery is connected. The open position (no jumper) indicates that no battery is connected.

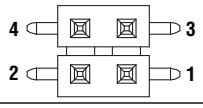
Purpose: Determining the presence and type of battery connected at J7.

Jumper Pin Reference:

	Jumper	Battery type
	1-2	External battery connected
	2-3	Internal battery connected
	open	No battery connected

7.5.3 Bits Per Pixel (JP4)

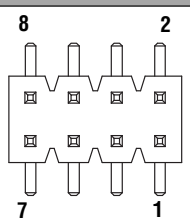
Select the appropriate number of bits per pixel (6 or 8 bpp) for the flat panel display connected to J12. This is a panel-dependent feature.

	Jumper	Pin 4 on J12 Setting
	1-2	Pin 4 on J12 is set to HIGH
	3-4	Pin 4 on J12 is set to LOW

Warning
Do not jumper more than one set of pins on JP4 simultaneously. This will damage the board.

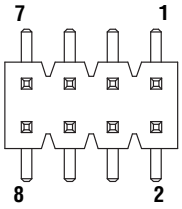
7.5.4 LVDS Configuration (JP5)

The graphics engine supports two independent interfaces. Use JP5 to configure the LVDS base address, clock frequency, and LVDS output swing for I^2C.

	Jumper	Setting	Options
	1-2	Base Address	Open: Dual I^2C 0xC0 Closed: Single I^2C 0x40
	3-4	Reserved	N/A
	5-6	Clock Frequency	Open: 0.5% Spread Closed: 0% Spread
	7-8	Output Voltage Swing	Open: 300 mV out Closed: 400 mV out

7.5.5 Panel Orientation (JP6)

Select the appropriate up/down and left/right panel orientation for the display connected to J12. This is a panel-dependent feature.

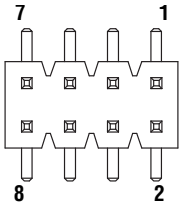
	Jumper	Setting
	1-2	Horizontal (left/right) Orientation: J12 Pin 18 set to HIGH
	3-4	Horizontal (left/right) Orientation: J12 Pin 18 set to LOW
	5-6	Vertical (up/down) Orientation: J12 Pin 17 set to HIGH
	7-8	Vertical (up/down) Orientation: J12 Pin 17 set to LOW

Warning
JP6 supports one jumper for the horizontal orientation setting and one jumper for the vertical orientation setting. Do not jumper more than one set of pins for each setting simultaneously. This will damage the board.

NOTE Not all panels support customizable left/right orientation.

7.5.6 Backlight Power (JP7)

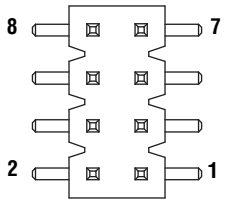
Select the appropriate backlight enable and power settings for the backlight.

	Jumper	Setting
	1-2	Backlight Enable: Active High
	3-4	Backlight Enable: Active Low
	5-6	Backlight Power: +5 VDC
	7-8	Backlight Power: +12 VDC

Warning
JP7 supports one jumper for the backlight enable setting and one jumper for the backlight power setting. Do not jumper more than one set of pins for each setting simultaneously. This will damage the board.

7.5.7 Ethernet GPIO Reference Voltage Selection (JP8)

The SBC35-CC405 supports voltages of 3.3 V, 5 V, and 12 V.



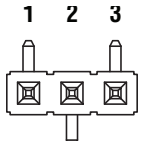
Jumper	Voltage
1-2	3.3 V
3-4	5.0 V
5-6	12.0 V

7.5.8 Basic Input/Output System (BIOS) Programming Defaults (JP9)

If you have saved EEPROM values that prevent you from accessing BIOS menus, the board can be reset to factory defaults as follows:

1. Turn the system off.
2. Install a jumper on **JP9** pins 2-3.
3. Turn the system on and enter the BIOS Main Menu by pressing the **F2** key. Factory defaults will be loaded at this point.
4. Remove the jumper from **JP9**.
5. Select **Exit Saving Changes** from the **Exit Menu**.

Jumper Pin Reference:



Jumper	Description
1-2	Normal operation
2-3	Reset EEPROM to factory default values
open	Normal operation (alternate)

7.6 Switches

7.6.1 Power Button (SW1)

The Power Button (SW1), located on the lower right edge of the board next to the audio line in/line out/microphone input, controls power to the SBC35-CC405. The first time you connect power to J5, the power button is bypassed and the board powers up automatically.

After the initial power up, press SW1 briefly to power the unit on or off, depending on the present state.

If the unit accidentally locks up and is unresponsive, press and hold SW1 for four (4) seconds to perform a hard restart.

7.6.2 Reset Button (SW2)

The Reset Button is a hardware reset. Press SW2 to reset the system. It grounds SYS_RESET# for a full system reset and is used to restart the system after a crash.

8. BIOS Settings

8.1 General Information

The SBC35-CC405 includes a BIOS from Phoenix Technologies to assure full compatibility with PC operating systems and software. The basic system configuration is stored in battery backed CMOS RAM within the clock/calendar. As an alternative, the CMOS configuration may be stored in EEPROM for operation without a battery. For more information of CMOS configuration, see the BIOS Settings Storage Options section of this manual. Access to this setup information is via the Setup Utility in the BIOS.

8.2 Entering Setup

To enter setup, power up the computer and press **F2** when either the splash screen is displayed or when the **Press F2 for Setup** message is displayed. It may take a few seconds before the main setup menu screen is displayed.

8.3 Navigation of the Menus

Use the up and down arrow keys to move among the selections and press **Enter** when a selection is highlighted to enter a sub-menu or to see a list of choices. See “BIOS Screens” on page 31. for available options.

8.4 BIOS Splash Screen

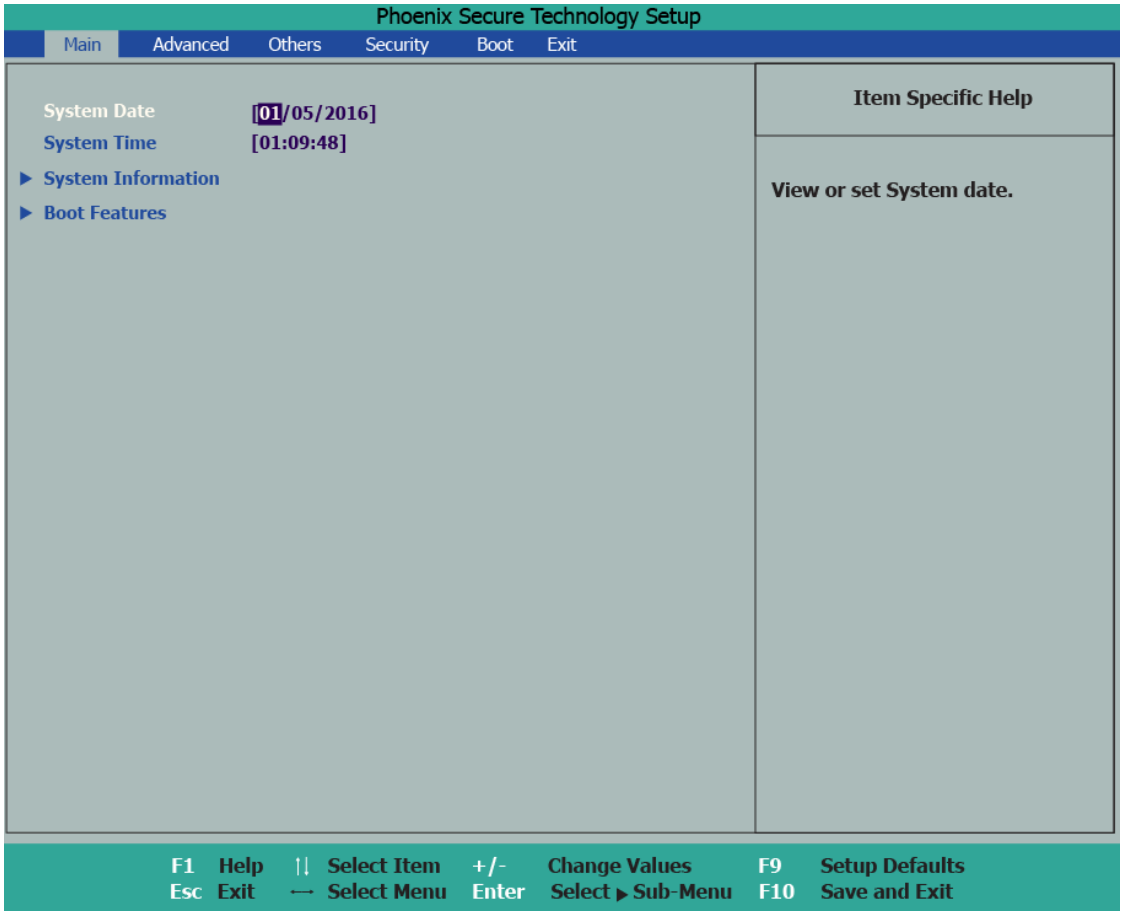
Custom BIOS Splash Screens can be accommodated for OEM customers. For details, please contact an Application Engineer through Technical Support (see contact information in the Introduction section on page 1).

8.5 BIOS Screens

The following BIOS screens contain the options and sample settings for the SBC35-CC405. Your actual configuration may differ from the screens shown here.

NOTE Use care when modifying BIOS settings.

Main Menu



System Date

Displays the current date in MM/DD/YYYY format. To set or change the date, highlight the row using the up/down arrow keys, then highlight the month, day, or year by pressing the Enter key until the desired value is highlighted with a square block. Use the +/- keys to change the highlighted value, or enter the time using the number keys.

System Time

Displays the current time in HH/MM/SS format. To set or change the time, highlight the row using the up/down arrow keys, then highlight the hour, minute, or second by pressing the Enter key until the desired value is highlighted with a square block. Use the +/- keys to change the highlighted value.

System Information

System Information parameters provide information and vary with BIOS version and the specific modules used. The typical format of the information is provided instead of the actual Default Setting or Value.

BIOS Version

Default Setting/Value: CC405yymmdd

BIOS Build Date

Default Setting/Value: mm/dd/yyyy

EC Version

Default Setting/Value: ymmddTXX

EC Build Date

Default Setting/Value: mm/dd/yyyy

Processor Type

Default Setting/Value: Intel® Atom™ CPU E3800 series

System Memory Speed

Default Setting/Value: 1066 MHz or 1333 MHz

L2 Cache Speed

Default Setting/Value: 512 KB per Core

Total Memory

Default Setting/Value: Up to 8192 MB

SODIMM Information

- MAC Address Port 1 (Module)
  Default Setting/Value: 00:90:FB:XX:XX:XX
- MAC Address Port 2 (Carrier)
  Default Setting/Value: 00:01:45:XX:XX:XX

Boot Features

NumLock

Selects the default state for NumLock during power up.

Default Setting/Value: On

Timeout

Number of seconds that Power On Self Test (POST) will wait for user input before booting.

Default Setting/Value: 2

CSM Support

Compatibility Support Module that provides backward compatibility services for legacy BIOS devices, such as int10/int13, dependent OS.

Default Setting/Value: Yes

Quick Boot

Enables/disables quick boot.

Default Setting/Value: Disable

Diagnostic Splash Screen

Enables/disables the diagnostic splash screen during boot.

Default Setting/Value: Disable

Diagnostic Summary Screen

Displays the Diagnostic Summary screen during boot.

Default Setting/Value: Disable

BIOS Level USB

Enables/disables all BIOS support for USB (boot time is reduced if USB support is not needed and disabled).

NOTE This will prevent using a USB keyboard in Setup or a USB biometric scanner such as a finger print reader to control access to setup, but does not prevent the operating system from supporting such hardware.

Default Setting/Value: Enable

Console Redirection

Enables/disables Universal Console Redirection

Default Setting/Value: Disable

Allow Hotkey in S4 Resume

Enables/disables hotkey detection when the system resumes from the Hibernate state.

Default Setting/Value: Enable

UEFI Boot

Enables the Unified Extensible Firmware Interface (UEFI). The UEFI interfaces between the OS and firmware.

Default Setting/Value: Enable

Legacy Boot

Enables Legacy boot (USB floppy emulation).

Default Setting/Value: Enable

Boot in Legacy Video Mode

When enabled, the display adapter is forced to switch from video mode to Text Mode 3 at the end of BIOS POST for non-UEFI boot mode (legacy boot). Some legacy software, such as DUET, requires BIOS to enter text video mode on boot.

Default Setting/Value: Disable

Load OPROM

Loads all OPROMs or on demand, according to the boot device.

Default Setting/Value: On Demand

Advanced Menu

The **Advanced** menu contains a variety of complex Items and submenus for CPU and other types of configuration.

Warning
Assigning incorrect values to items on the following screen menus may cause system malfunction.

CPU Configuration

Active Processor Cores

Number of cores to enable in each processor package.

Default Setting/Value: All

Execute Disable Bit

Prevents certain classes of malicious buffer overflow attacks when combined with a supporting Operating System (OS).

Default Setting/Value: Enable

Limit CPUI Maximum

Disabled for Windows XP.

Default Setting/Value: Disable

Bi-directional PROCHOT#

When a processor thermal sensor trips (either core), the PROCHOT# will be driven. If bi-direction is enabled, external agents can drive PROCHOT# to throttle the processor.

Default Setting/Value: Enable

VTX-2

Enables or disables the VTX-2 Mode support.

Default Setting/Value: Enable

TM1

Enables or disables TM1, which is a thermal monitor based on clock throttling.

Default Setting/Value: Enable

DTS

Enables or disables the digital thermal sensor, which protects the processor from overheating.

Default Setting/Value: Enable

CPU Power Management

This subset of the CPU Configuration menu provides CPU power management options.

- Intel® SpeedStep™: Enables or disables the processor's performance states (P-States)
  Default Setting/Value: Enable
- Boot Performance Mode: Selects the performance state that the BIOS will set before OS handoff.
  Default Setting/Value: Max Performance
- Intel Turbo Boost Technology: Enable to allow processor cores to run faster than the base operating frequency if it is operating below power, current, and temperature specification limits.
  Default Setting/Value: Enable
- C-States: Enables or disables C-States
  Default Setting/Value: Disable

Uncore Configuration

GOP Driver

Enable or disable the GOP Driver. Enabling will unload VBIOS; Disabling will load VBIOS.

Default Setting/Value: Enable

Integrated Graphics Device

Enables or disables the Integrated Graphics Device (IGD).

Default Setting/Value: Enable

Primary Display

Selects which of the IGD/PCI Graphics devices should be the primary display, or select SG for Switchable/Hybrid GFX.

Default Setting/Value: Auto

RC6 (Render Standby)

Enables or disables render standby support.

Default Setting/Value: Enable

PAVC

Enables or disables protected audio/video control.

Default Setting/Value: Lite Mode

GTT Size

Selects the GTT size.

Default Setting/Value: 2 MB

Aperture Size

Selects the aperture size.

Default Setting/Value: 256 MB

DVMT Pre-Allocated

Selects the DVMT 5.0 pre-allocated (Fixed) graphics memory size used by the internal graphics device.

Default Setting/Value: 64 MB

IGD Turbo

Selects the IGD Turbo feature, if Auto is selected. IGD Turbo will only be enabled when SOC stepping is 80 or above.

Default Setting/Value: Auto

Spread Spectrum Clock

Enables or disables the clock chip spread spectrum feature.

Default Setting/Value: Disable

Force Lid Status

For test: forces lid status to on or off.

Default Setting/Value: ON

BIA

When Auto is selected, GMCH uses the VBIOS default. When Level n is selected, GMCH is enabled with the selected Aggressiveness Level.

Default Setting/Value: Auto

IGD Boot Type

Selects preference for Integrated Graphics Device (IGD) display interface used upon system boot.

Default Setting/Value: Auto

Panel Scaling

Selects the LCD panel scaling option used by the internal graphics device.

Default Setting/Value: Auto

LCD Configuration

- LCD Panel Type: Selects the LCD panel type.
  Default Setting/Value: 1024 x 768 NXP Generic
- Bpp Select: Selects the bpp type.
  Default Setting/Value: 24 Bpp

South Cluster Configuration

PCI Express Configuration

This subset of the South Cluster Configuration menu provides PCI Express configuration options.

- PCIe 0 Speed: Configures PCIe 0 speed.
  Default Setting/Value: Auto
- PCIe 1 Speed: Configures PCIe 1 speed.
  Default Setting/Value: Auto
- PCIe 2 Speed: Configures PCIe 2 speed.
  Default Setting/Value: Auto
- PCIe 3 Speed: Configures PCIe 3 speed.
  Default Setting/Value: Auto
- PCI Express Root Port 1: Controls the PCI Express Root Port 1 (MiniPCIe)
  Default Setting/Value: Enable
- PCI Express Root Port 2: Controls the PCI Express Root Port 2 (MiniPCIe)
  Default Setting/Value: Enable
- PCI Express Root Port 3: Controls the PCI Express Root Port 3 (Ethernet, Carrier)
  Default Setting/Value: Enable
- PCI Express Root Port 4: Controls the PCI Express Root Port 4 (Ethernet, Carrier)
  Default Setting/Value: Enable

USB Configuration

This subset of the South Cluster Configuration menu provides USB configuration options.

- XHCI Link Power Management: Enables or disables XHCI link power management (USB 3.0).
  Default Setting/Value: Enable
- EHCI Controller: Controls the USB EHCI 9USB 2.0) functions. One EHCI controller must always be enabled.
  Default Setting/Value: Enable
- USB Per-Port Control: Allows USB ports 0-3 individual power control.
  Default Setting/Value: Enable
- USB Port #0: Enables or disables the USB port.
  Default Setting/Value: Enable
- USB Port #1: Enables or disables the USB port.
  Default Setting/Value: Enable
- USB Port #2: Enables or disables the USB port.
  Default Setting/Value: Enable
- USB Port #3: Enables or disables the USB port.
  Default Setting/Value: Enable

Audio Configuration

This subset of the South Cluster Configuration menu provides audio configuration options.

LPE Audio Support: Selects LPE Audio ACPI mode or PCI mode.
Default Setting/Value: Disable

Audio Controller: Controls detection of the Azalia device. When disabled, Azalia is unconditionally disabled; when enabled, Azalia is unconditionally enabled.
Default Setting/Value: Enable

SATA Drives

This subset of the South Cluster Configuration menu provides SATA drive options.

- Chipset SATA: Enables or disables the chipset SATA controller. The chipset SATA controller supports both internal SATA ports (up to 3Gb/s supported per channel)
  Default Setting/Value: Enable
- SATA Test Mode: Enables or disables test mode.
  Default Setting/Value: Disable
- Chipset SATA Mode: When IDE is selected, compatibility mode disables AHCI. When AHCI is selected, advanced SATA features such as Native Command Queuing are supported.
  Default Setting/Value: AHCI

Warning
OS may not boot if this setting is changed after OS install.

LAN Configuration

This subset of the South Cluster Configuration menu provides LAN configuration options.

- PXE ROM: Enables or disables PXE Option ROM execution for onboard LAN.
  Default Setting/Value: Disable

Miscellaneous Configuration

This subset of the South Cluster Configuration menu provides miscellaneous configuration options.

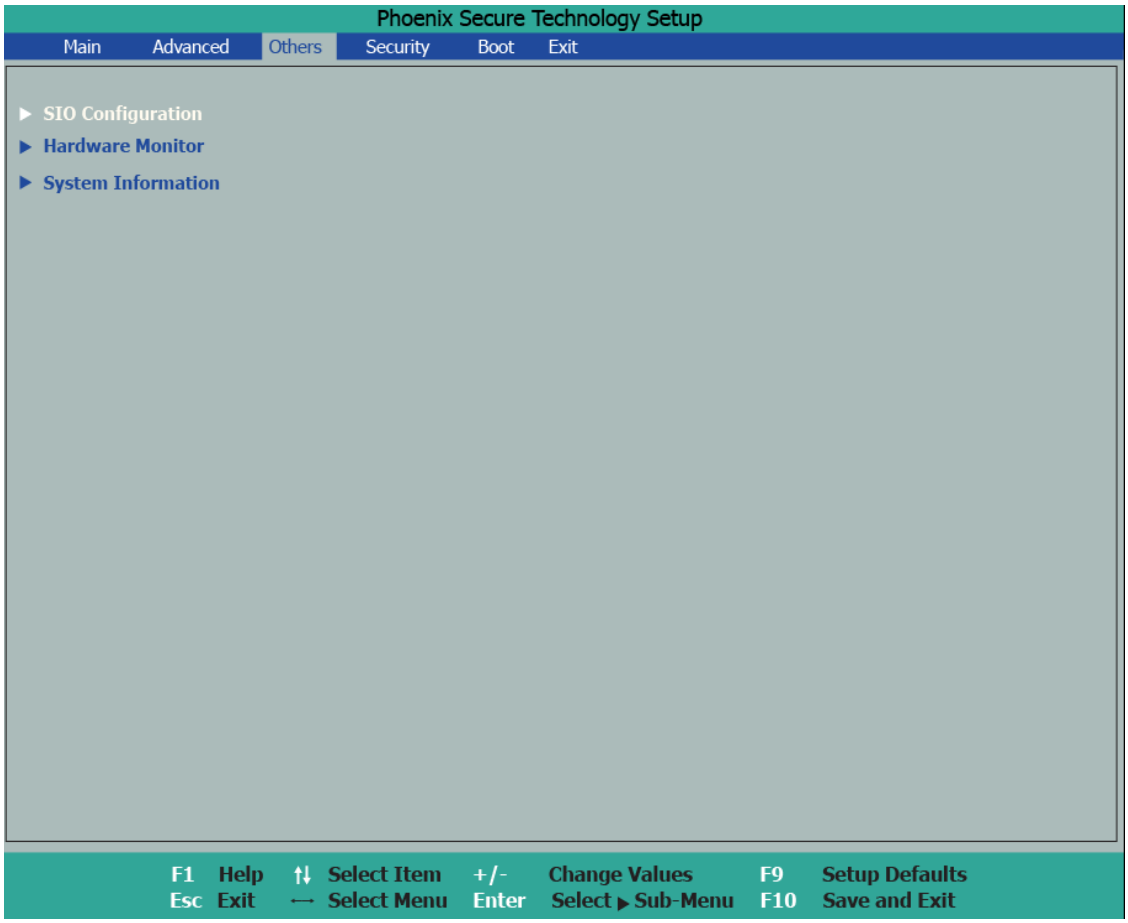
- State After G3: Specifies in which state to begin when power is re-applied after a power failure (G3 state).
  Default Setting/Value: SO State
- SMM Lock: Enables or disables the SMM Lock feature. This locks the SMRAM and disables the SMM driver.
  Default Setting/Value: Enable
- PCI MMIO Size: Sets the PCIO MMIO size.
  Default Setting/Value: 2 GB

Security Configuration

TXE FW Version (Read Only)

Default Setting/Value: 1.0.2.1067

Others



SIO Configuration

Serial 1

- I/O Address: Modifies the input serial 1 I/O address range from 0x100 to 0xFFF8.
  Default Setting/Value: 3F0
- IRQ: Modifies the input serial 1 IRQ range from 1 to 15.
  Default Setting/Value: 4
- Mode: Selects the Serial 1 mode. Available modes are RS232, RS422, RS485, and Loopback.
- Termination: Selects the UART termination. Not available in RS232 mode.
  Default Setting/Value: No Termination

- SLEW: Selects the Serial 1 SLEW.
  Default Setting/Value: not Limited
- BRG: Selects the Serial 1 BRG. High = 33.333 MHz; Normal = 1.8432 MHz.
  Default Setting/Value: Normal

Serial 2

- I/O Address: Modifies the input serial 2 I/O address range from 0x100 to 0xFFF8.
  Default Setting/Value: 2F8
- IRQ: Modifies the input serial 2 IRQ range from 1 to 15.
  Default Setting/Value: 3
- Mode: Selects the Serial 2 mode. Available modes are RS232, RS422, RS485, and Loopback.
- Termination: Selects the UART termination. Not available in RS232 mode.
  Default Setting/Value: No Termination
- SLEW: Selects the Serial 2 SLEW.
  Default Setting/Value: not Limited
- BRG: Selects the Serial 2 BRG. High = 33.333 MHz; Normal = 1.8432 MHz.
  Default Setting/Value: Normal

IO60

- I/O Address: Modifies the input serial 3 I/O address range from 0x100 to 0xFFF8.
  Default Setting/Value: 3E8
- IRQ: Modifies the input serial 3 IRQ range from 1 to 15.
  Default Setting/Value: 6

GPS

- I/O Address: Modifies the input serial 4 I/O address range from 0x100 to 0xFFF8.
  Default Setting/Value: 2E8
- IRQ: Modifies the input serial 4 IRQ range from 1 to 15.
  Default Setting/Value: 7

Watch Dog Timer

- Watch Dog Timer: Enables or disables the watch dog timer.
  Default Setting/Value: Disable
- Timer Unit: Select whether the timer value is expressed in seconds or minutes.
  Default Setting/Value: Second
- Timer Value: 255 seconds or 255 minutes, depending upon the choice of timer unit.
  Default Setting/Value: 255

Hardware Monitor

CPU Temp

Displays the temperature of the CPU in Celsius.

CPU Fan

N/A if no external an is connected.

APM Configuration

Power On By RTC Alarm

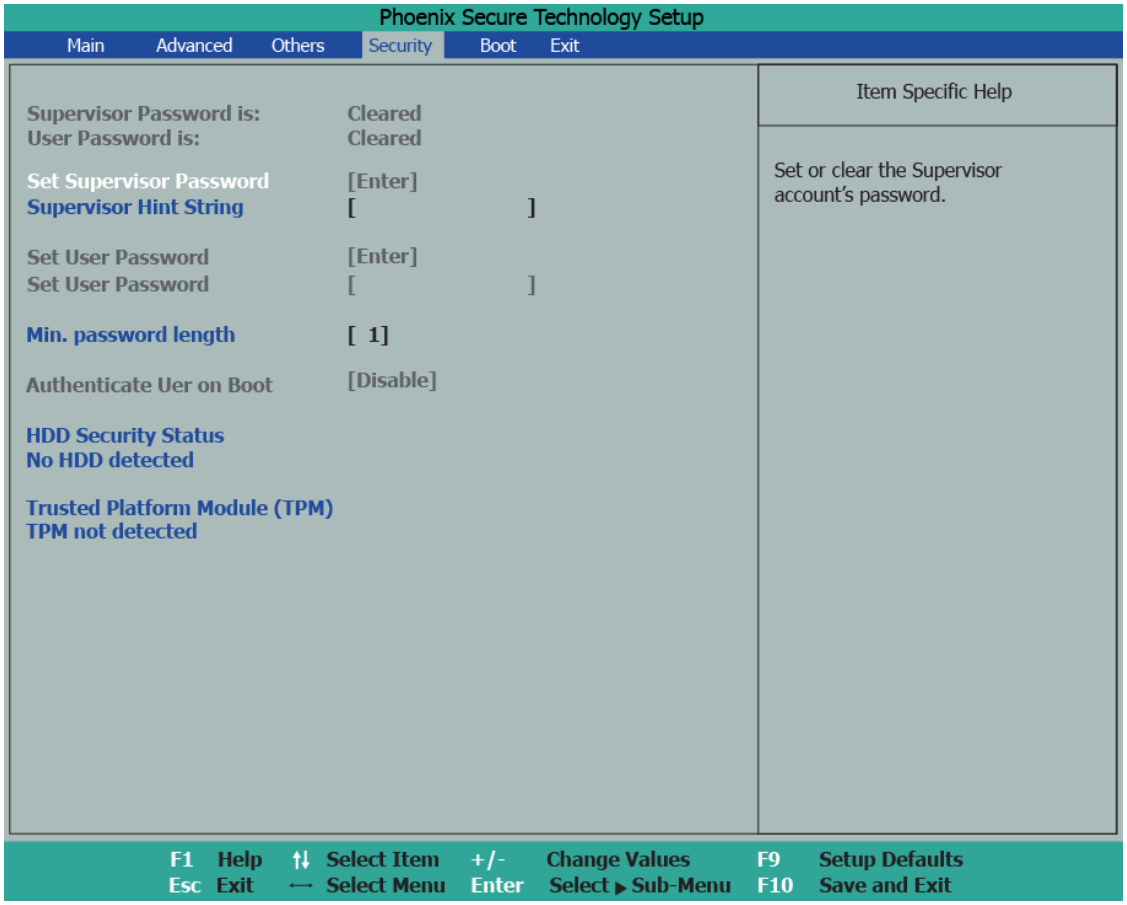
If enabled, allows the SBC to be powered on by an RTC alarm.

Default Setting/Value: Disable

Wake On LAN1

Default Setting/Value: Enable

Security



Supervisor Password is (Read Only)

Default Setting/Value: Cleared

User Password is (Read Only)

Default Setting/Value: Cleared

Set Supervisor Password

Press **Enter** to set or clear the supervisor account's password. Press **Esc** to exit without making changes.

Supervisor Hint String

Press **Enter** to type a hint for the Supervisor password. If you forget your password, the answer to your hint will help you recover the password.

Set User Password

Press **Enter** to set or clear the user password. Press **Esc** to exit without making changes.

User Hint String

Press **Enter** to type a hint for the User password. If you forget your password, the answer to your hint will help you recover the password.

Min. password length

Sets the minimum number of characters for your password (1-20).

Default Setting/Value: 1

Authenticate User on Boot

Enables or disables user authentication prompt on boot.

Default Setting/Value: Disable

HDD Security Status

If no hard disk drive is detected, this is blank.

No HDD Detected

This is displayed when no hard disk drive is detected.

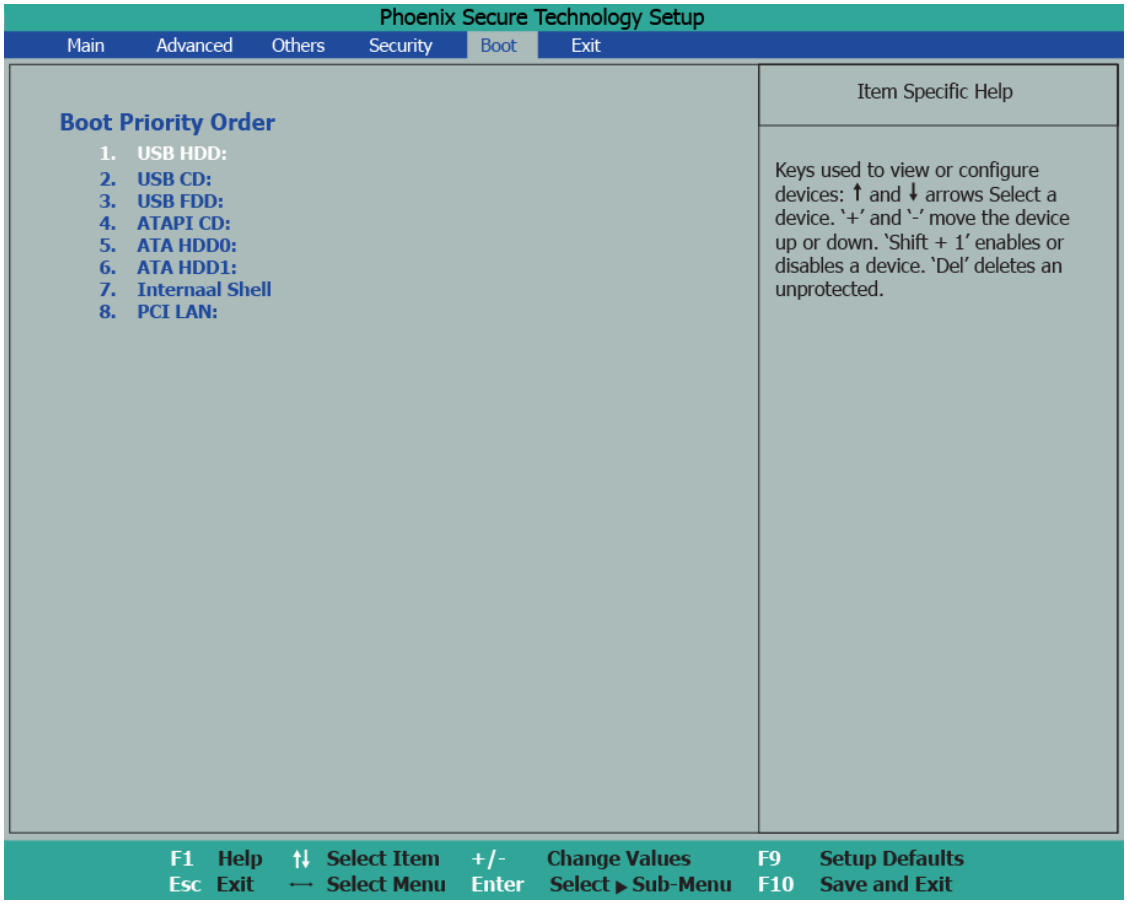
Trusted Platform Module (TPM)

This is the name of the next variable.

TPM Not Detected

This is the TPM variable current state.

Boot



Boot Priority Order

Once selected, use the + or – key to change the order in which the selected device boots.

Keys used to view or configure devices: Up and down arrows select a device. '+' and '-' move the device up or down. 'Shift + 1' enables or disables a device. 'Del' deletes an unprotected device.

Exit

Exit Saving Changes

Saves all changes, exits setup, and restarts the system.

Exit Discarding Changes

Exits setup without changes.

Load Setup Defaults

Loads standard default values (this is the same functionality as F9).

Discard Changes

Loads the original values of this boot time, not the default setup values.

Save Changes

Save all changes on all menus, but does not restart the system.

9. Cables and Software Drivers

Go to www.winsystems.com for cable information and software drivers.

Appendix A. Best Practices

This section outlines the best practices for operating the SBC35-CC405 in a safe, effective manner, that will not damage the board. Please read this section carefully.

Power Supply

Avoid Electrostatic Discharge (ESD)—Only handle the circuit board and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

Power Supply Budget

Evaluate your power supply budget. It is usually good practice to budget twice the typical power requirement for all of your devices.

Use Proper Power Connections (Voltage)—When verifying the voltage, measure it at the power connector on the SBC35-CC405. Measuring it at the power supply does not account for voltage drop through the wire and connectors.

Power Down

Make sure that power has been removed from the system before making or breaking any connections.

Power Supply OFF—The power supply should always be off before it is connected to the I/O Module. Do not hot-plug the SBC35-CC405 on a host platform that is already powered.

I/O Connections OFF—I/O Connections should also be off before connecting them to the embedded computer modules or any I/O cards. Connecting hot signals can cause damage whether the embedded system is powered or not.

Mounting and Protecting the I/O Module

The SBC35-CC405 must be mounted properly to avoid damage.

Mounting Holes—The mounting holes are plated on the top, bottom and through the barrel of the hole and are connected to the embedded computer module's ground plane. Traces are often routed in the inner layers right below, above or around the mounting holes.

- Never use a drill or any other tool in an attempt to make the holes larger.
- Never use screws with oversized heads. The head could come in contact with nearby components causing a short or physical damage.
- Never use self-tapping screws; they will compromise the walls of the mounting hole.
- Never use oversized screws that cut into the walls of the mounting holes.
- Always use all of the mounting holes. By using all of the mounting holes, you will provide the support that the embedded computer module needs to prevent bending or flexing.

Plug or Unplug Connectors Only on Fully Mounted Boards—Never plug or unplug connectors on a board that is not fully mounted. Many of the connectors fit tightly, and the force needed to plug or unplug them could cause the embedded computer module to flex.

Avoid Cutting the SBC35-CC405—Never use star washers or any fastening hardware that will cut into the SBC35-CC405.

Avoid Over-tightening of Mounting Hardware—Causing the area around the mounting holes to compress could damage interlayer traces around the mounting holes.

Use Appropriate Tools—Always use tools that are appropriate for working with small hardware. Large tools can damage components around the mounting holes.

Avoid Conductive Surfaces—Never allow the embedded computer module to be placed on a conductive surface. Many embedded systems use a battery to back up the clock-calendar and CMOS memory. A conductive surface such as a metal bench can short the battery causing premature failure.

Conformal Coating

Conformal coating by any source other than WINSYSTEMS voids the product warranty and will not be accepted for repair by WINSYSTEMS. If such a product is sent to WINSYSTEMS for repair, it will be returned at customer expense and no service will be performed. A WINSYSTEMS product conformally coated by WINSYSTEMS will be subject to regular WINSYSTEMS warranty terms and conditions.

Operations/Product Manuals

Every single board computer has an Operations manual or Product manual.

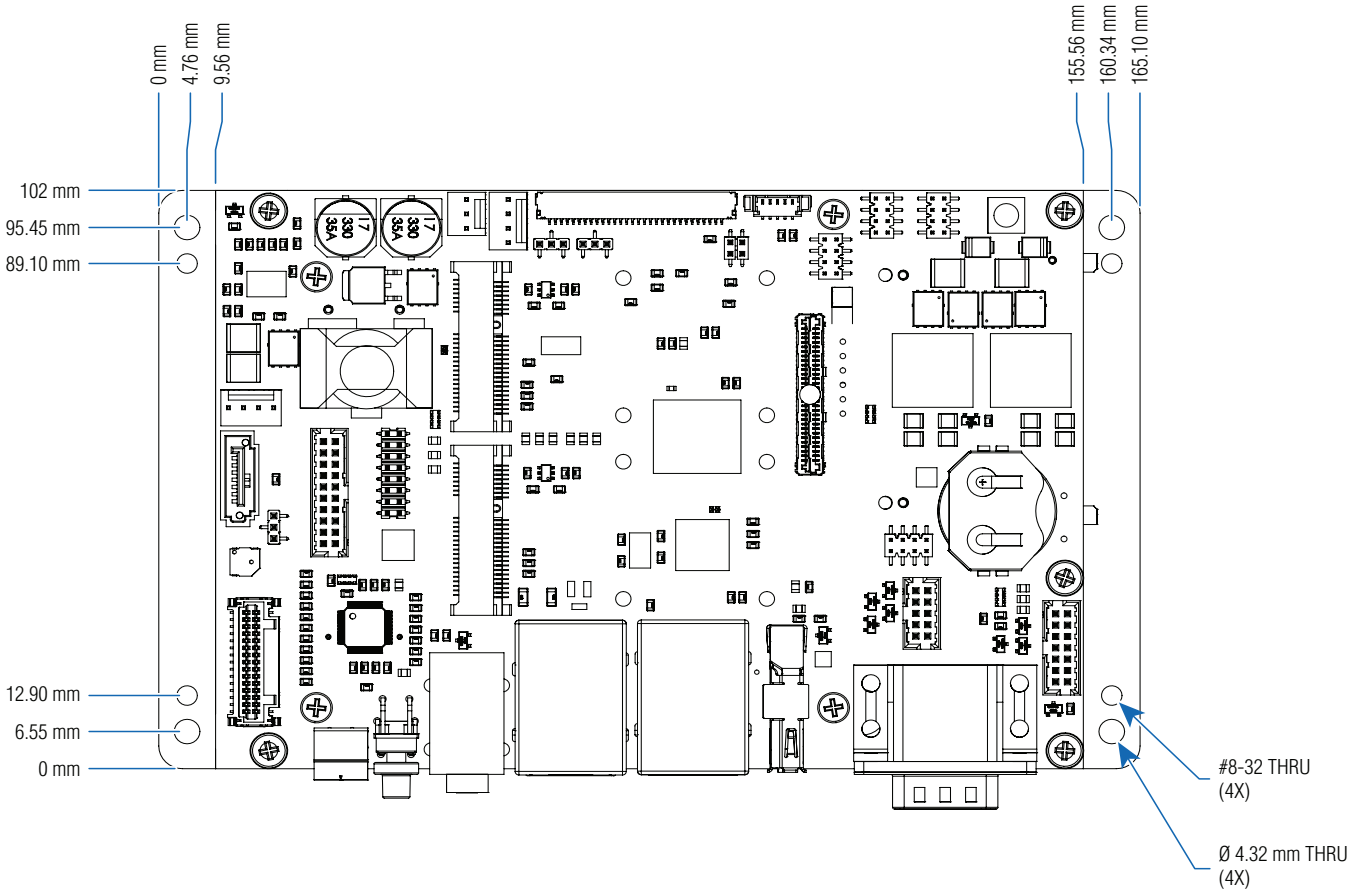
Periodic Updates—Operations/Product manuals are updated often. Periodically check the WinSystems website (https://www.winsystems.com) for revisions.

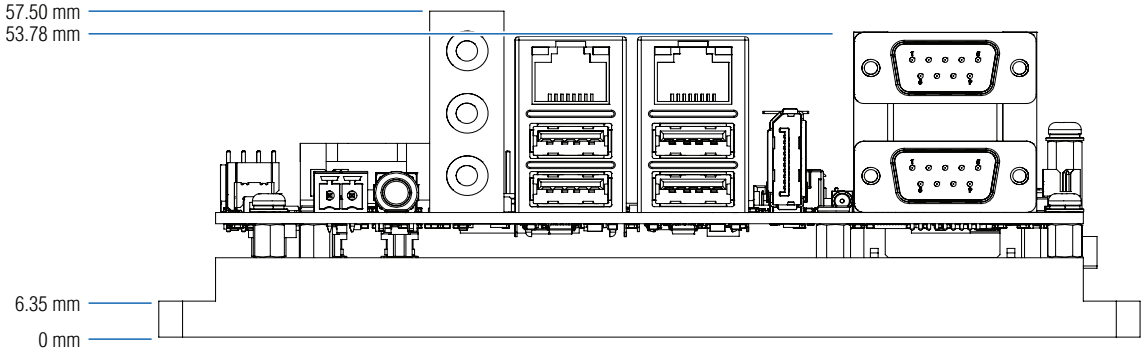
Check Pinouts—Always check the pinout and connector locations in the manual before plugging in a cable. Many I/O modules will have identical headers for different functions and plugging a cable into the wrong header can have disastrous results.

Contact an Applications Engineer—If a diagram or chart in a manual does not seem to match your board, or if you have additional questions, contact a WinSystems Applications Engineer at: +1-817-274-7553.

Appendix B. Mechanical Drawing

SBC35-CC405 Dimensions





Appendix C. Warranty Information

Full warranty information can be found at https://winsystems.com/company-policies/warranty/.