WINSYSTEMS®

PPM-C407

Intel® Atom™ E3800 PC/104-Plus Single Board Computer with Digital I/O

Product Manual

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Revision History

Document Version	Last Updated Date	Brief Description of Change
v1.0	2/2016	Initial release
v1.1	2/2017	Updated specifications, I/O ranges, and made minor text changes
v1.2	7/29/2025	Updated Conformal Coating, added Warranty link, updated all links

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Table of Contents

1. Before You Begin

Review the warnings in this section and the best practice recommendations (see “Best Practices” on page 52) when using and handling the WinSystems PPM-C407. Following these recommendations provides an optimal user experience and prevents damage. Read through this document and become familiar with the PPM-C407 before proceeding.

APPLYING CONFORMAL COATING AFTER PURCHASE WILL VOID YOUR WARRANTY. FAILING TO COMPLY WITH THESE BEST PRACTICES MAY DAMAGE THE PRODUCT AND VOID YOUR WARRANTY.

1.1 Warnings

Only qualified personnel should configure and install the PPM-C407. While observing the best practices, pay particular attention to the following:

Avoid Electrostatic Discharge (ESD)
Only handle the circuit board and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

2. Introduction

This manual provides configuration and usage information for the PPM-C407. If you still have questions, contact Technical Support at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

Refer to the WinSystems website for other accessories (including cable drawings and pinouts) that can be used with your PPM-C407.

3. Functionality

The PPM-C407 is a full-featured embedded single board computer that operates in the Windows 7, Windows 8, Windows 10, Windows CE, Linux and DOS environments. It features an Intel® Atom™ E3800 Processor, up to 4 GB soldered DDR3 RAM, PC/104 and PC/104-Plus bus connectors (stack-through connectors are optional), as well as optional fanless operation. It provides 24 lines of 5 V DC tolerant digital input-output (DIO), and also video output with audio support. Communication interfaces include Gigabit Ethernet, four USB 2.0 ports, two serial RS-232/422/485 channels and two serial RS-232. channels. Refer to “Features” on page 2 and “General Operation” on page 4 for specific information.

NOTE WinSystems can provide custom configurations for OEM clients. Please contact an Application Engineer for details.

4. Features

The PPM-C407 provides the following features:

Single Board Computer

- PC/104-Plus Compatible Single Board Computer
  - Optional stack-through PC/104-Plus connectors
- Available Multi-Core Intel® Atom™ E3800 Processors
  - E3815 1 core, 1.46 GHz
  - E3825 2 core, 1.33 GHz
  - E3845 4 core, 1.91 GHz

Operating Systems (compatibility)

- Windows (32/64-bit)
- Linux
- other x86-compatible

Memory

- Available 2 GB or 4 GB Soldered Down DDR3 RAM

BIOS

- Phoenix SecureCore™

Video Interfaces (Intel Gen7 Graphics, one or two simultaneously active displays)

- Mini DisplayPort (version 1.1)
- Video Graphics Array (VGA up to 2560 x 1536)
- Low-Voltage Differential Signaling (LVDS, 18 or 24 bpp)

Ethernet

- Intel® i210 Gigabit Ethernet port (1 gigabit per second, GbE) with Surge Suppression

Storage

- MiniPCIe/mSATA Socket (same connection as used for Bus Expansion)
- Bootable SATA Connector

Digital Input/Output (DIO)

- 24 lines (bi-directional) provided within the Lattice Semiconductor Corp., MachXO2™ FPGA (field-programmable gate array) interfaced to the processor with the Low Pin Count (LPC) interface.
- 5 V tolerant signals
- Each line programmable for input, output, or event sense
- Lines can be paired with external isolation and relay modules

Bus expansion

- PC/104-Plus (PC/104 and PCI-104)
- MiniPCIe/mSATA Socket (same connection as used for Storage)

Serial Interface

- Four USB 2.0 with Surge Suppression
- Serial Ports
  - Two RS232/422/485: speeds to 500 Kbps (0.5 Mbps)
  - Two RS232: speeds to 250 Kbps (0.25 Mbps)

Audio

- Stereo Audio (Line In, Line Out, Mic)

Power

- +5 V DC Power Input

Industrial Operating Temperature

- Fanless -40 °C to +85 °C (-40 °F to +185 °F)

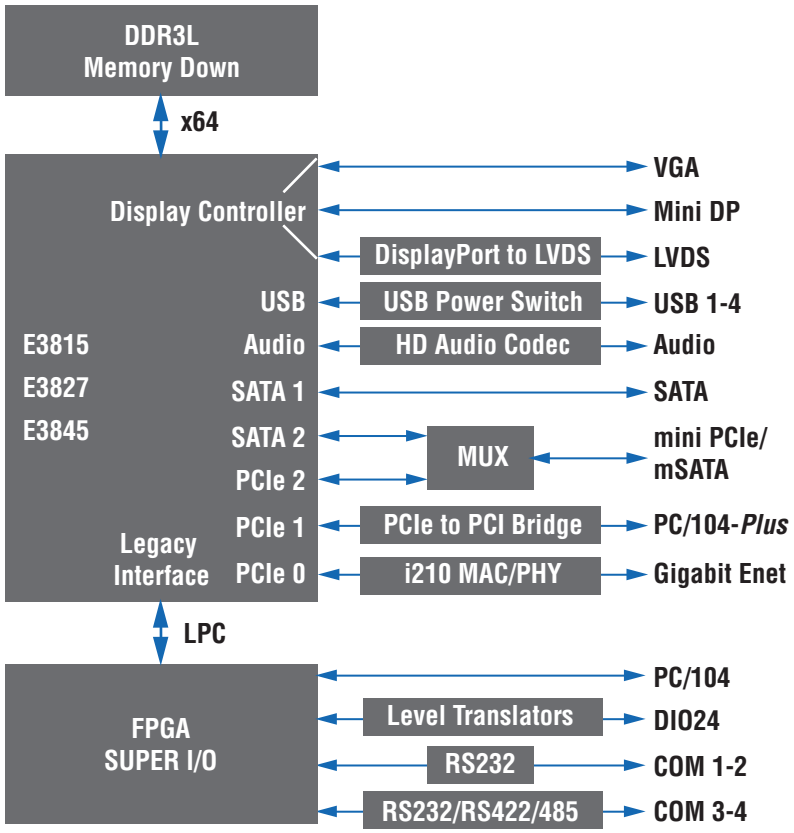
Additional features

- Watchdog timer from 1 second to 255 minutes (15,300 seconds)
- Real-Time Clock (RTC) with optional battery back up
- Status LEDs for Ethernet, 3.3 V Stand-By, and one software controlled
- Speaker output

5. General Operation

5.1 System Block Diagram

The PPM-C407 is a single-board computer (SBC). It is a full-featured embedded system with a variety of onboard I/O options. The following figure is a simplified system block diagram of the PPM-C407.



Three display interfaces (MiniDisplayPort, VGA, and LVDS) support up to two independent displays along with stereo audio. Communication interfaces include Gigabit Ethernet, four USB 2.0 ports, two serial RS-232/422/485 channels and two serial RS-232 channels. 24 digital I/O lines with event sense can be programmed individually for input, output, or interrupt driven applications. For additional flexibility, the I/O lines can be paired with external isolation and relay modules.

The PPM-C407 can provide an upgrade for existing PC/104-Plus Compatible Single Board Computers. It's designed for harsh environments and reliability, featuring soldered RAM for added shock and vibration resistance, and provides an optional fanless solution for operating temperatures between -40 °C and +85 °C (-40 °F and +185 °F).

The PPM-C407 processor options provide single, dual, or quad-core processing. Each processor option is available with 2 GB or 4 GB of soldered DDR3 memory and optional stack-through PC/104-Plus connectors.

Linux, Windows and other x86 operating systems can be initialized from the SATA, mSATA, or USB interfaces. This provides flexible data storage options.

6. Specifications

The PPM-C407 adheres to the following specifications and requirements:

PPM-C407 Specifications

Electrical	
V_{CC}	+5 V DC ±5% required **E3845-4G:** 1.7 A Typical, 2.5 A Maximum **E3825-2G**: 1.2 A Typical, 2.0 A Maximum **E3815-2G**: 1.4 A Typical, 2.0 A Maximum
Models[1, 2] [1] See processor for ***38XX*** models [2] Add **-ST** to the end of each part number for a stack-through configuration	**PPM-C407-*38XX*-2-0** PC/104-Plus SBC E3825 2 GB with heat spreader **PPM-C407-*38XX*-2-1** PC/104-Plus SBC E3825 2 GB with heatsink **PPM-C407-*38XX*-4-0** PC/104-Plus SBC E3825 4 GB with heat spreader **PPM-C407-*38XX*-4-1** PC/104-Plus SBC E3825 4 GB with heatsink **PPM-C407-*38XX*-2-0-ST** PC/104-Plus SBC E3845 2 GB with heat spreader **PPM-C407-*38XX*-2-1-ST** PC/104-Plus SBC E3845 2 GB with heatsink **PPM-C407-*38XX*-4-0-ST** PC/104-Plus SBC E3845 4 GB with heat spreader **PPM-C407-*38XX*-4-1-ST** PC/104-Plus SBC E3845 4 GB with heatsink
Processor	**3815:** E3815 single-core 1.46 GHz, 512 K cache (MOQ required) **3825:** E3825 dual-core 1.33 GHz, 1 MB cache **3845:** E3845 quad-core 1.91 GHz, 2 MB cache
Mechanical	
Dimensions	4.550 x 3.775 inches (115.57 x 95.59 mm)
Weight	7.592 oz (215.23 g), without optional heatsink
PCB thickness	0.078 inch (1.98 mm)

PPM-C407 Specifications (Continued)

Environmental	
Temperature	-40 °C to +85 °C (-40 °F to +185 °F)
Humidity (RH)	5% to 95% non-condensing
Mechanical Shock Testing	MIL-STD-202G, Method 213B, Condition A 50g half-sine, 11 ms duration per axis, 3 axis
Random Vibration Testing	MIL-STD-202G, Method 214A, Condition D .1g/Hz (11.95g rms), 20 minutes per axis, 3 axis
RoHS Compliant	Yes
Operating Systems	
Runs 32/64-bit Windows, Linux, and other x86-compatible operating systems.	

Additional Accessories

Standoff kits are available and recommended for use with the PPM-C407.

- KIT-PCM-STANDOFF-4: Four piece Nylon Hex PC/104 Standoff Kit
- KIT-PCM-STANDOFF-B-4: Four piece Brass Hex PC/104 Standoff Kit

The following table lists the items contained in each kit:

Kit	Component	Description	Qty
KIT-PCM-STANDOFF-4 4 pc. Nylon Hex PC/104 Standoff Kit	Standoff	Nylon 0.25” Hex, 0.600" Long Male/Female 4-40	4
	Hex Nut	Hex Nylon 4-40	4
	Screw	Phillips-Pan Head (PPH) 4-40 x 1/4" Stainless Steel	4
KIT-PCM-STANDOFF-B-4 4 pc.Brass Hex PC/104 Standoff Kit	Standoff	Brass 5 mm Hex, 0.600" Long Male/Female 4-40	4
	Hex Nut	4-40 x 0.095 Thick, Nickel Finish	4
	Screw	Phillips-Pan Head (PPH) 4-40 x 1/4" Stainless Steel	4

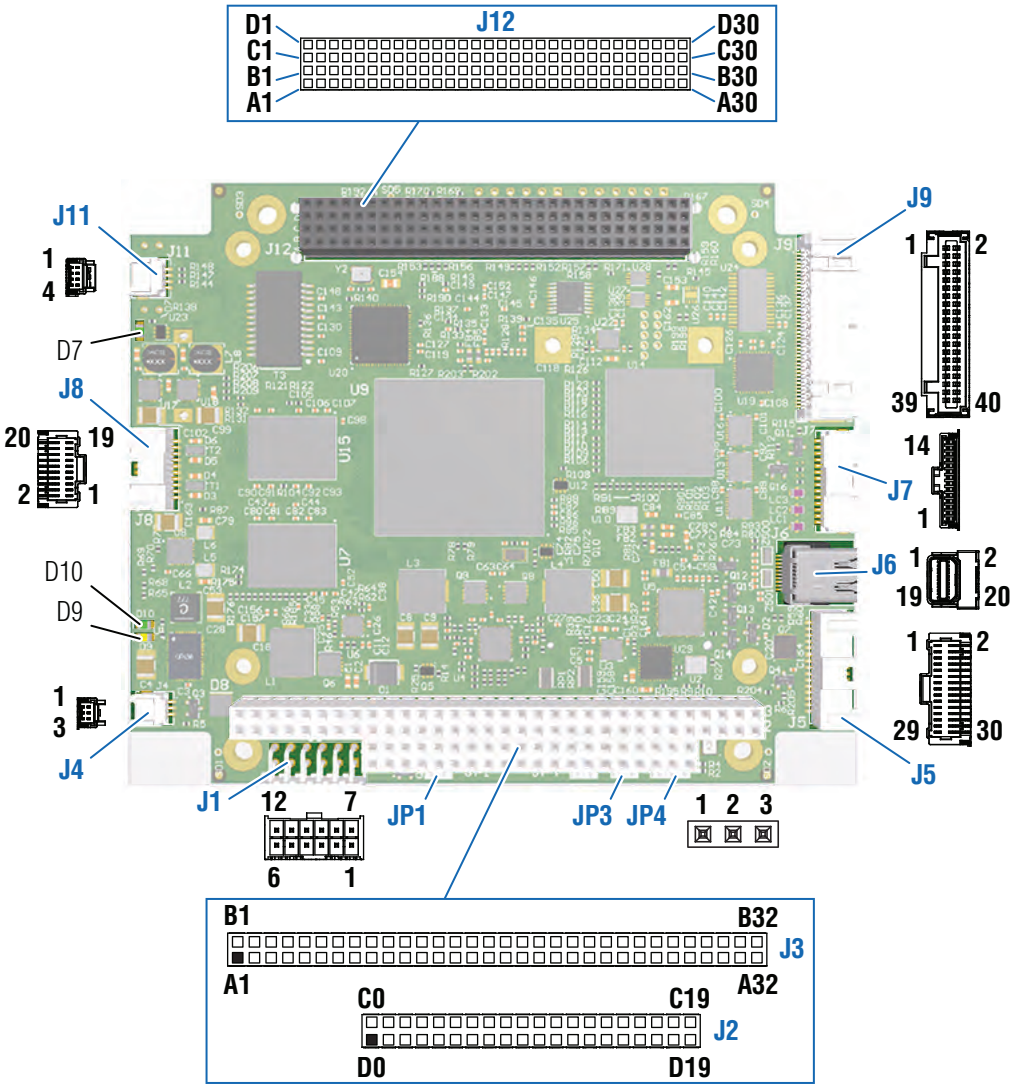
7. Configuration

This section describes the PPM-C407 components and configuration.

7.1 Component Layout

The PPM-C407 provides components on the top and bottom of the board.

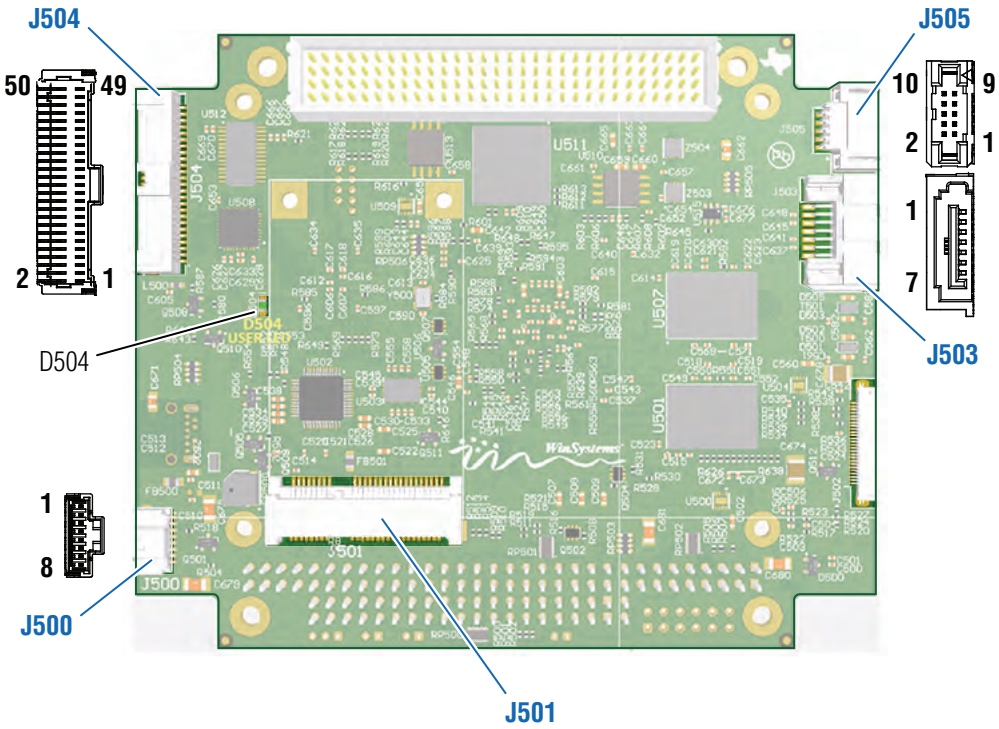
7.1.1 Top View



Top View Components:

Item	Description	Reference
J1	Power Connector	page 16
J2	PC/104 Bus (C/D, 16-bit ISA bus also includes J3) Connector	page 17
J3	PC/104 Bus (A/B, 8-bit ISA bus) Connector	page 17
J4	External Battery Connector	page 19
J5	LVDS and Audio Connector	page 20
J6	Mini DisplayPort	page 21
J7	VGA	page 22
J8	USB	page 23
J9	Serial Ports	page 24
J11	Ethernet External LEDs	page 26
J12	PC/104-Plus (PCI bus)	page 27
JP1	AT/ATX Power Mode	page 32
JP3	Basic Input/Output System (BIOS) Defaults	page 33
JP4	Low-Voltage Differential Signaling (LVDS)	page 33
D7, D9, D10	LED Indicators	page 34

7.1.2 Bottom View



Bottom View Components:

Item	Description	Reference
J500	Backlight	page 28
J501	Mini PCIe/mSATA Connector	page 29
J503	Serial ATA (SATA)	page 30
J504	Digital Input/Output	page 31
J505	Ethernet	page 32
D504	User LED Indicator	page 34

7.2 I/O Port Map

The PPM-C407 uses plug-and-play (PnP) BIOS resource allocation. Care must be taken to avoid contention with resources allocated by the BIOS.

The PPM-C407 utilizes a Low Pin Count to Industry Standard Architecture bridge (LPC to ISA Bridge) to address the PC/104 bus. Most legacy PC/104 modules are I/O mapped and function as expected. The LPC controller is the subtractive agent of the Intel Legacy Block. All transactions not claimed elsewhere are sent to the LPC controller. The LPC to ISA Bridge does not implement bus mastering cycles or direct memory access (DMA).

The following table contains the I/O ports used on the PPM-C407.

PCU I/O Addresses

I/O Address	Device
0000h-001Fh	DMA Controller 82C37
0020h-0021h	Interrupt Controller 8259 Master
0024h-0025h	Interrupt Controller 8259 Master
0028h-0029h	Interrupt Controller 8259 Master
002Ch-002Dh	Interrupt Controller 8259 Master
0030h-0031h	Interrupt Controller 8259 Master
0034h-0035h	Interrupt Controller 8259 Master
0038h-0039h	Interrupt Controller 8259 Master
003Ch-003Dh	Interrupt Controller 8259 Master
0040h-0043h	Timer counter 8254
0050h-0053h	Timer counter 8254
0060h	PS2 Control (data port)
0061h	NMI controller
0062h	8051 download 4K address counter
0064h	PS2 Control (status port)
0066h	8051 download 8-bit data port
0070h-0077h	RTC Controller
0080h-0083h	Port 80
0092h	Init Register (Reset Generator)
00A0h-00A1h	Interrupt Controller 8259 Slave
00A4h-00A5h	Interrupt Controller 8259 Slave
00A8h-00A9h	Interrupt Controller 8259 Slave
0ACh-00ADh	Interrupt Controller 8259 Slave
00B0h-00B1h	Interrupt Controller 8259 Slave

PCU I/O Addresses (Continued)

I/O Address	Device
00B2h-00B3h	Power Management
00B4h-00B5h	Interrupt Controller 8259 Slave
00B8h-00B9h	Interrupt Controller 8259 Slave
0120h-012Fh	Digital I/O (Default)
0298h-029Bh	Reserved for Super I/O Configuration
029C	Interrupt Status Register
029D	Status LED Register
029E-029F	Watchdog Timer Control
02E8h-02EFh	COM4 (Default)
02F8h-02FFh	COM2 (Default)
03E8h-03EFh	COM3 (Default)
03F8h-03FFh	COM1 (Default)
0400h-047Fh	Reserved ACPI
0564h-0568h	Advanced Watchdog
0800h-08FFh	Reserved
0CF9h	Reset Generator
2000-201Fh	Reserved SMBus
FED1C000h-FED1C3FFh	Reserved RCBA

7.3 Interrupt Map

Hardware Interrupts (IRQs) are supported for PC/104 (ISA), PCI, and PCIe devices. The user must reserve IRQs in the BIOS CMOS configuration for use by legacy devices. The PCIe/PnP BIOS will use unreserved IRQs when allocating resources during the boot process. The following tables contain the IRQ resources as used by the PPM-C407.

IRQ resources

IRQ	Device
IRQ0	Internal Timer /Counter 0 or HPET #0
IRQ1	Keyboard
IRQ2	Chained to Slave controller (IRQ9)
IRQ3	COM2 *
IRQ4	COM1 *
IRQ5	COM3 *
IRQ6	COM4 *
IRQ7	FREE **
IRQ8	Real Time Clock
IRQ9	FREE **
IRQ10	Digital I/O

IRQ resources (Continued)

IRQ	Device
IRQ11	PCI Interrupts
IRQ12	Mouse
IRQ13	Floating point processor
IRQ14	SATA Controller
IRQ15	SATA Controller ***

* These IRQ references are default settings that can be changed by the user in the CMOS Settings utility. Reference the Super I/O Control section under Intel.

** IRQ9 is commonly used by ACPI when enabled and may be unavailable (depending on operating system) for other uses.

*** IRQ15 is currently unavailable under the Windows operating systems.

Some IRQs can be freed for other uses if the hardware features they are assigned to are not being used. To free an interrupt, use the CMOS setup screens to disable any unused board features or their IRQ assignments.

Interrupt Status Register - 29CH

Bit	Name
Bit 0	COM1
Bit 1	COM2
Bit 2	COM3
Bit 3	COM4
Bit 4	N/A
Bit 5	N/A
Bit 6	N/A
Bit 7	N/A

WinSystems does not provide software support for implementing the Interrupt Status Register to share interrupts. Some operating systems, such as Windows XP and Linux, have support for sharing serial port interrupts (see your specific operating system's documentation for any available examples). You will need to implement the appropriate software to share interrupts for the other devices.

NOTE A 1 will be read for devices with an interrupt pending.

7.4 Register Definitions

The PPM-C407 uses the WinSystems exclusive application-specific integrated circuit (ASIC), the WS16C48. This device provides 48 lines of digital I/O. There are 16 unique registers within the WS16C48. The following table summarizes the registers.

I/O Address Offset	Page 0	Page 1	Page 2	Page 3
00h	Port 0 I/O	Port 0 I/O	Port 0 I/O	Port 0 I/O
01h	Port 1 I/O	Port 1 I/O	Port 1 I/O	Port 1 I/O
02h	Port 2 I/O	Port 2 I/O	Port 2 I/O	Port 2 I/O
03h	Port 3 I/O	Port 3 I/O	Port 3 I/O	Port 3 I/O
04h	Port 4 I/O	Port 4 I/O	Port 4 I/O	Port 4 I/O
05h	Port 5 I/O	Port 5 I/O	Port 5 I/O	Port 5 I/O
06h	Int_Pending	Int_Pending	Int_Pending	Int_Pending
07h	Page/Lock	Page/Lock	Page/Lock	Page/Lock
08h	Reserved	Pol_0	Enab_0	Int_ID0
09h	Reserved	Pol_1	Enab_1	Int_ID1
0Ah	Reserved	Pol_2	Enab_2	Int_ID2

The following sections provide details on each of the internal registers.

7.4.1 Port 0 through 5 I/O

Each I/O bit in each of the six ports can be individually programmed for input or output. Writing a 0 to a bit position causes the corresponding output pin to go to a high-impedance state (pulled high by external 10 KΩ resistors). This allows it to be used as an input. When used in the input mode, a read reflects the inverted state of the I/O pin, such that a high on the pin will read as a 0 in the register. Writing a 1 to a bit position causes that output pin to sink current (up to 12 mA), effectively pulling it low.

7.4.2 INT_PENDING

This read-only register reflects the combined state of the INT_ID0 through INT_ID2 registers. When any of the lower three bits are set, it indicates that an interrupt is pending on the I/O port corresponding to the bit position(s) that are set.

Reading this register allows an Interrupt Service Routine to quickly determine if any interrupts are pending and which I/O port has a pending interrupt.

7.4.3 PAGE/LOCK

This register serves two purposes. The upper two bits (D6 and D7) select the register page in use. Bits 0-5 allow for locking the I/O ports. Write a 1 to the I/O port position to prohibit further writes to the corresponding I/O port:

Page	D7	D6	D5-D0
Page 0	0	0	1/0
Page 1	0	1	1/0
Page 2	1	0	1/0
Page 3	1	1	1/0

7.4.4 POL0 through POL2

These registers are accessible when Page 1 is selected. They allow interrupt polarity selection on a port-by-port and bit-by-bit basis. Writing a 1 to a bit position selects the rising edge detection interrupts while writing a 0 to a bit position selects falling edge detection interrupts.

7.4.5 ENAB0 through ENAB2

These registers are accessible when Page 2 is selected. They allow for port-by-port and bit-by-bit enabling of the edge detection interrupts. When set to a 1, the edge detection interrupt is enabled for the corresponding port and bit. When cleared to 0, the bit's edge detection interrupt is disabled. Note that this register can be used to individually clear a pending interrupt by disabling and re-enabling the pending interrupt.

7.4.6 INT_ID0 through INT_ID2

These registers are accessible when Page 3 is selected. They are used to identify currently pending edge interrupts. A bit when read as a 1 indicates that an edge of the polarity programmed into the corresponding polarity register has been recognized. Note that a write to this register (value ignored) clears ALL of the pending interrupts in this register.

7.5 Watchdog Timer

The PPM-C407 features an advanced watchdog timer which can be used to guard against software lockups. Two interfaces are provided to the watchdog timer. The Advanced interface is the most flexible and recommended for new designs. The other interface option is provided for software compatibility with older WinSystems single board computers.

7.5.1 Advanced

The watchdog timer can be enabled in the BIOS Settings by entering a value for **Watchdog Timeout** on the **Intel** > **Super I/O Control** screen. Any non-zero value represents the number of minutes prior to reset during system boot. Once the operating system is loaded, the watchdog can be disabled or reconfigured in the application software.

NOTE Use a long timeout if the watchdog is enabled when trying to boot any operating system.

The watchdog can be enabled, disabled, or reset by writing the appropriate values to the configuration registers located at I/O addresses 565h and 566h. The watchdog is enabled by writing a timeout value other than zero to the I/O address 566h and disabled by writing 00h to this I/O address. The watchdog timer is serviced by writing the desired timeout value to I/O port 566h. If the watchdog has not been serviced within the allotted time, the circuit resets the CPU.

The timeout value can be set from 1 second to 255 minutes. If port 565h bit 7 equals 0, the timeout value written into I/O address 566h is in minutes. The timeout value written to address 566h is in seconds if port 565 bit 7 equals 1.

Watchdog Timer Examples

Port Address	Port Bit 7 Value	Port Address	Value	Reset Interval
565h	x	566h	00h	DISABLED
565h	1	566h	03h	3 seconds
565h	1	566h	1Eh	30 seconds
565h	0	566h	04h	4 Minutes
565h	0	566h	05h	5 Minutes
Software watchdog timer PET = PORT 566h, write the timeout value.				

7.6 Real-time Clock/Calendar

A real-time clock is used as the AT-compatible clock/calendar. It supports a number of features including periodic and alarm interrupt capabilities. In addition to the time and date keeping functions, the system configuration is kept in CMOS RAM contained within the clock section. A battery must be enabled for the real-time clock to retain time and date during a power down.

7.7 Power

The PPM-C407 draws power through the J1 connector (see “J1 Power Connector” on page 16). The main supply to the board is 5 V DC. If supplied to the input connector, the +12 V DC and -12 V DC supply only the PC/104 and PC/104-Plus connectors; 5 V DC stand-by is only required to supply the power connector for ATX mode operation.

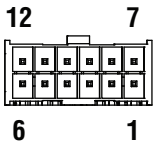
The PPM-C407 supports AT or ATX type power supplies. Jumper JP1 (see “JP1 AT/ATX Power Mode” on page 32) specifies the type of supply connected to the single board computer. AT Power is a simple on/off power supply with no interaction with the single board computer. Most embedded systems use this type of power supply (default setting).

7.8 Connectors

7.8.1 J1 Power Connector

Use this connection to supply power to the PPM-C407. Set Jumper JP1 (see “JP1 AT/ATX Power Mode” on page 32) to select the type of power supply operation (AT or ATX).

Layout and Pin Reference:



Pin	Name	Pin	Name
1	ATX_PWRGOOD	7	+5V_SB
2	GND	8	+5 V
3	GND	9	+5 V
4	+12VDC	10	-12 V
5	PSON_N	11	GND
6	PMC_RSTBTN_N	12	PWRBTN_N

Additional Information

This power connection uses a 12-pin Samtec IPL1-106-01-L-D-RA-K, 2x6, 2.54 mm pitch mini-mate locking header connector.

Matching connector:

- Samtec IPD1-06-D-K housing
- Samtec CC79L-2024-01L crimp pins

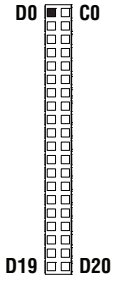
WinSystems cable CBL-PWR-700-18 simplifies this connection to the board.

7.8.2 J2 PC/104 bus (C/D, 16-bit ISA bus also includes J3) Connector J3 PC/104 bus (A/B, 8-bit ISA bus) Connector

The PC/104 bus is electrically equivalent to the 16-bit ISA bus. Standard PC/104 I/O cards can be populated on PPM-C407's connectors, located at J2 and J3. The interface does not support hot swap capability.

Layout and Pin Reference:

J2

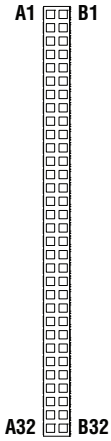


Pin	Name	Pin	Name
D0	GND	C0	GND
D1	MEMCS16#	C1	SBHE#
D2	IOCS16#	C2	LA23
D3	IRQ10	C3	LA22
D4	IRQ11	C4	LA21
D5	IRQ12	C5	LA20
D6	IRQ15	C6	LA19
D7	IRQ14	C7	LA18
D8	DACK0#	C8	LA17
D9	DRQ0	C9	MEMR#
D10	DACK5#	C10	MEMW#
D11	DRQ5	C11	SD8
D12	DACK6#	C12	SB9
D13	DRQ6	C13	SD10
D14)	DACK7#	C14	SD11
D15	DRQ7	C15	SD12
D16	+5V	C16	SD13
D17	MASTER#	C17	SD14
D18	GND	C18	SD15
D19	GND	C19	GND

#: Active Low Signal

B10 and C19 are key locations. WinSystems uses key pins as connections to GND.

J3



Pin	Name	Pin	Name
A1	IOCHK#	B1	GND
A2	SD7	B2	RESET
A3	SD6	B3	+5V
A4	SD5	B4	IRQ
A5	SD4	B5	-5V
A6	SD3	B6	DRQ2
A7	SD2	B7	-12V
A8	SD1	B8	SRDY#
A9	SD0	B9	+12V
A10	IOCHRDY	B10	GND
A11	AEN	B11	SMEMW#
A12	SA19	B12	SMEMR#
A13	SA18	B13	IOW#
A14	SA17	B14	IOR#
A15	SA16	B15	DACK3#
A16	SA15	B16	DRQ3
A17	SA14	B17	DACK1#
A18	SA13	B18	DRQ1
A19	SA12	B19	REFRESH#
A20	SA11	B20	BCLK
A21	SA10	B21	IRQ7
A22	SA9	B22	IRQ6
A23	SA8	B23	IRQ5
A24	SA7	B24	IRQ4
A25	SA6	B25	IRQ3
A26	SA5	B26	DACK2#
A27	SA4	B27	TC
A28	SA3	B28	BALE
A29	SA2	B29	+5V
A30	SA1	B30	OSC
A31	SA0	B31	GND
A32	GND	B32	GND

Additional Information

This connection uses different on-board connectors for stack-through or non-stack-through models:

J2 (40-pin) Connector

- Teka PC220-W1BD-M (non-stack-through, solder bearing)
- Teka PC220-W1A7-M (stack-through, solder bearing)

J3 (64-pin) Connector

- Teka PC232-W1BD-M (non-stack-through, solder bearing)
- Teka PC232-W1A7-M (stack-through, solder bearing)

No keys in connector and no cut pins.

7.8.3 J4 External Battery Connector

An optional external battery, connected to J4, supplies the PPM-C407 board with standby power for the real-time clock and CMOS setup RAM. An extended temperature lithium battery is available from WinSystems, part number:

- BAT-LTC-E-36-16-2
- BAT-LTC-E-36-27-2

A power supervisory circuit contains the voltage sensing circuit and an internal power switch to route the battery or standby voltage to the circuits selected for backup. The battery automatically switches ON when the VCC of the systems drops below the battery voltage and back OFF again when VCC returns to normal.

Layout and Pin Reference:

	Pin	Name
	1	GND
	2	BAT+
	3	NC

Additional Information

This connection uses MOLEX part number 501953-0307 (WinSystems part number: G650-2003-7FB).

Matching connector:

- MOLEX part number: 501939-0300
- MOLEX Crimp Terminal: 501334

WinSystems battery BAT-LTC-E-36-16-2 and BAT-LTC-E-36-27-2 (connected to J3) simplify these connections to the board.

BAT-LTC-E-36-16-2

BAT-LTC-E-36-27-2

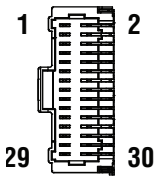
7.8.4 J5 LVDS and Audio Connector

NOTE The PPM-C407 has one VGA, one DisplayPort and one Low-Voltage Differential Signaling (LVDS) interface. Only two of the three outputs may be active simultaneously.

The LVDS portion of this connector can be configured (see “JP4 Low-Voltage Differential Signaling (LVDS)” on page 33). Use the LVDS portion to connect to the LVDS interface (includes pins 1 through 21, non-shaded in the following table).

Use the audio portion to connect to the Audio interface (pins 22 through 30, shaded in the following table).

Layout and Pin Reference:



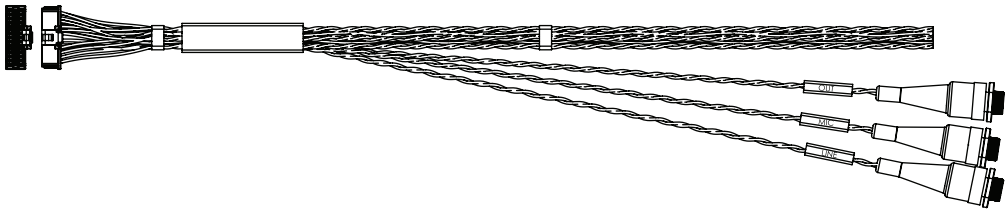
Pin	Name	Pin	Name
1	LVDS_VCC (LVDS)	2	GND (LVDS)
3	D0- (LVDS)	4	D0+ (LVDS)
5	D1- (LVDS)	6	D1+ (LVDS)
7	LVDS_VCC (LVDS)	8	GND (LVDS)
9	D2- (LVDS)	10	D2+ (LVDS)
11	D3- (LVDS)	12	D3+ (LVDS)
13	LVDS_VCC (LVDS)	14	GND (LVDS)
15	CLK- (LVDS)	16	CLK+ (LVDS)
17	DDC_CLK (LVDS)	18	GND (LVDS)
19	DDC_DATA (LVDS)	20	GND (LVDS)
21	GND (LVDS)	22	ANALOG_GND (AUDIO)
23	OUT_R (AUDIO)	24	MIC_R (AUDIO)
25	OUT_L (AUDIO)	26	MIC_L (AUDIO)
27	ANALOG_GND (AUDIO)	28	ANALOG_GND (AUDIO)
29	LINE_R (AUDIO)	30	LINE_L (AUDIO)
Non-shaded cells designate LVDS interface.			
Shaded cells designate Audio Interface.			

Additional Information

The LVDS interface terminates at a portion of a Molex 501571-3007, 2x15, 1 mm pitch (Pico-Clasp™) right angle locking header connector (WS G650-2030-7HB) shared with the Audio interface.

Matching connectors:

- LVDS: Molex 501189-3010 housing with Molex 501193-2000 crimp pins.
- Backlight: Molex 501330-1100 with Molex 501334-0000 crimp pins.
- WinSystems cables simplify connections to the board:
  - CBL-LVDSAB-005-12: LVDS/Audio & Bklt to 7" Ampire with Audio Jacks
  - CBL-LVDSB-006-12: LVDS & Bklt to 7" Ampire without Audio
  - CBL-LVDSA-007-12: LVDS/Audio to 12" Mitsubishi with Audio Jacks
  - CBL-LVDSA-008-12: LVDS to 12" Mitsubishi without Audio
  - CBL-LVDSAB-003-12: LVDS/Audio & Bklt to 6.5" AUO with Audio Jacks
  - CBL-SPL-001-14: LVDS/Audio to unterminated LVDS with Audio Jacks (shown)



7.8.5 J6 Mini DisplayPort

NOTE The PPM-C407 has one VGA, one DisplayPort and one Low-Voltage Differential Signaling (LVDS) interface. Only two of the three outputs may be active simultaneously.

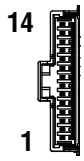
Layout and Pin Reference:

	PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
	1	GND	Ground	2	Hot Plug Detect	Hot Plug Detect
	3	ML_Lane 0 (p)	Lane 0 (positive)	4	CONFIG1	CONFIG1
	5	ML_Lane 0 (n)	Lane 0 (negative)	6	CONFIG2	CONFIG2
	7	GND	Ground	8	GND	Ground
	9	ML_Lane 1 (p)	Lane 1 (positive)	10	ML_Lane 3 (p)	Lane 3 (positive)
	11	ML_Lane 1 (n)	Lane 1 (negative)	12	ML_Lane 3 (n)	Lane 3 (negative)
	13	GND	Ground	14	GND	Ground
	15	ML_Lane 2 (p)	Lane 2 (positive)	16	AUX_CH (p)	Auxiliary Channel (positive)
	17	ML_Lane 2 (n)	Lane 2 (negative)	18	AUX_CH (n)	Auxiliary Channel (negative)
	19	GND	Ground	20	DP_PWR	Power for connector

7.8.6 J7 VGA

NOTE The PPM-C407 has one VGA, one DisplayPort and one Low-Voltage Differential Signaling (LVDS) interface. Only two of the three outputs may be active simultaneously.

Layout and Pin Reference:



Pin	Name	Description
1	VGA_RED	CRT red signal input
2	GND	GND
3	VGA_GREEN	CRT green signal input
4	GND	GND
5	VGA_BLUE	CRT blue signal input
6	GND	GND
7	VGA_HSYNC	CRT Horizontal Synchronization
8	GND	GND
9	VGA_VSYNC	CRT Vertical Synchronization
10	GND	GND
11	DDC_SDA	CRT DDC Data
12	GND	GND
13	DDC_SCL	CRT DDC clock
14	VCC	5V input for CRT

Additional Information

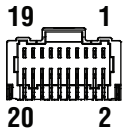
The VGA interface terminates with a Molex 501568-1407, 1x14, 1 mm pitch (Pico-Clasp™) right angle locking header connector (WS G650-2014-7FB).

Matching connector: Molex 501330-1400 housing with Molex 501334-0000 crimp pins. WinSystems cable CBL-VGA-002-12 (Pico-Clasp to DB-15) simplifies this connection to the board.

7.8.7 J8 USB

The PPM-C407 provides four USB2.0 ports with Littlefuse PGB1010603MR (WS G607-0013-004) ESD surge protection and Murata DLW21HN900SQ2L common mode noise suppressors (WS G605-1014-000). The TI TPS2505B1RGWR (WS G673-0025-131) USB power switch is used to enhance the stability of powering USB devices.

Layout and Pin Reference:

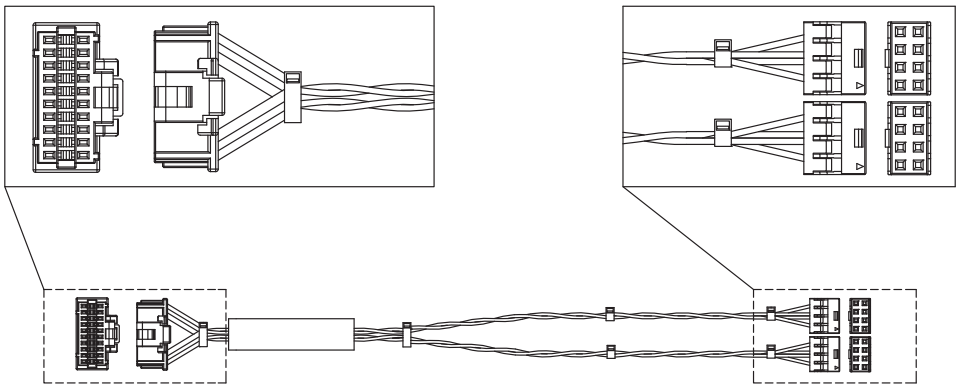


Pin	Name	Pin	Name
1	USB1V	2	USB2V
3	USB1_N	4	USB2_N
5	USB1_P	6	USB2_P
7	GND	8	GND
9	GND	10	GND
11	GND	12	GND
13	USB3V	14	USB4V
15	USB3_N	16	USB4_N
17	USB3_P	18	USB4_P
19	GND	20	GND

The four ports terminate at a Molex 501571-2007, 2x10, 1 mm pitch (Pico-Clasp™) right angle locking header connector (WS G650-2020-7HB).

Matching connector: Molex 501189-2010 housing with Molex 501193-2000 crimp pins. WinSystems cables simplify connections to the board:

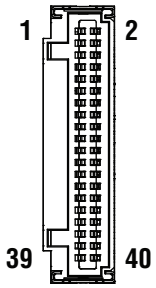
- CBL-USB4-000-14: Pico-Clasp to unterminated
- CBL-USB4-001-12: Pico-Clasp to Pico-Clasp
- CBL-USB4-002-12: Pico-Clasp to 2each, 2x4, 2 mm pitch housing (shown)



7.8.8 J9 Serial Ports

The PPM-C407 provides four serial ports through the Lattice MachX02 FPGA interfaced to the processor with the Low Pin Count (LPC) interface. Two serial ports support RS232, RS422 and RS485 protocols (using the Exar SP339E multi-protocol transceiver). The other two ports support RS232 (only) using the Maxim MAX3241E transceiver.

Layout and Pin Reference:

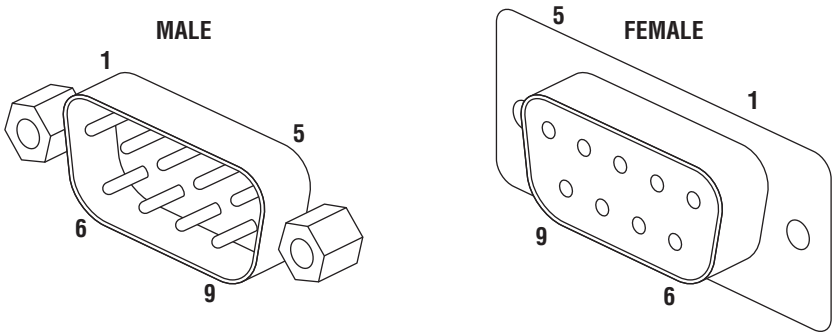


Pin	Name	Pin	Name
1	DCD1	2	DSR1
3	RXD1	4	RTS1
5	TXD1	6	CTS1
7	DTR1	8	RI1
9	GND	10	GND
11	DCD2	12	DSR2
13	RXD2	14	RTS2
15	TXD2	16	CTS2
17	DTR2	18	RI2
19	GND	20	GND
21	DCD3	22	DSR3
23	RXD3	24	RTS3
25	TXD3	26	CTS3
27	DTR3	28	RI3
29	GND	30	GND
31	DCD4	32	DSR4
33	RXD4	34	RTS4
35	TXD4	36	CTS4
37	DTR4	38	RI4
39	GND	40	GND

Four independent, asynchronous serial channels are on-board. All serial ports are configured as Data Terminal Equipment (DTE). Both the send and receive registers of each port have a 16-byte FIFO. All serial ports have 16C550-compatible UARTs. The RS-232 transceivers have charge pumps to generate the plus and minus voltages so the PPM-C407 only requires +5 V to operate. Each port is set up to provide internal diagnostics such as loopback and echo mode on the data stream. An independent, software programmable baud rate generator is selectable from 50 through 115.2 kbps. Individual modem handshake control signals are supported for all ports.

RS-232 interface levels are supported on all four serial ports which can be enabled in the BIOS. COM3 and COM4 also have RS-422/RS-485 support.

COM1, COM2, COM3, COM4 (DB-9 Male and Female)

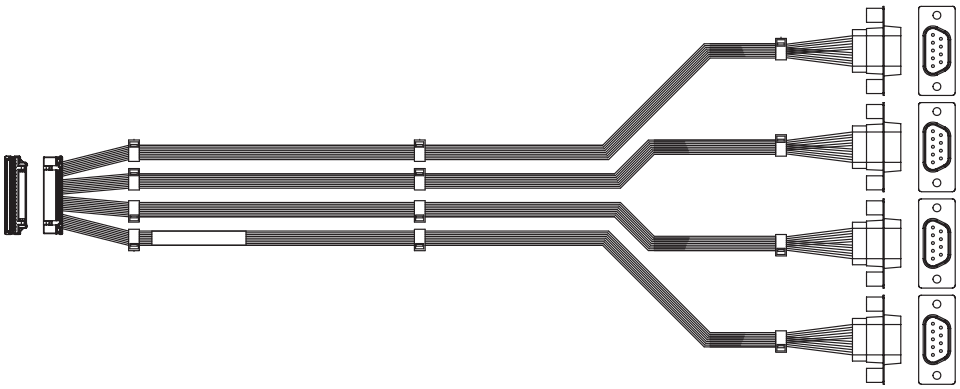


Pin	RS-232	RS-422	RS-485
1	DCD	N/A	N/A
2	RX	TX+	TX/RX+
3	TX	RX+	N/A
4	DTR	N/A	N/A
5	GND	GND	GND
6	DSR	TX-	TX/RX-
7	RTS	RX-	N/A
8	CTR	N/A	N/A
9	RI	N/A	N/A

The four ports terminate with a Molex 502046-4070, 2x20, 1.25 mm pitch (Duo-Clasp™) right angle locking header connector (WS G650-2040-7HC).

Matching connection: Molex 503110-4000 housing with Molex 501930-1100 crimp pins. WinSystems cables simplify connections to the board:

- CBL-SER4-000-14: Duo-Clasp to unterminated
- CBL-SER4-001-12: Duo-Clasp to Duo-Clasp
- CBL-SER4-002-12: Duo-Clasp to 4xDB9 (shown)



7.8.9 J11 Ethernet External LEDs

On-board Ethernet activity signals are provided at this connector. These activity signals are also available off-board for enclosures or other applications that have remote mounting requirements. Each external LED signal has an on-board 200 Ω resistor (in series).

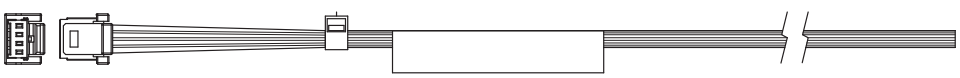
Layout and Pin Reference:

	Pin	Name	Descrption
1 4	1	EXT_LED0	External LED 0
	2	EXT_LED1	External LED 1
	3	EXT_LED2	External LED 2
	4	V3P3A	+3.3V Power

The Ethernet activity LEDs terminate at a Molex 501953-0407, 1x4, 1 mm pitch (Pico-Clasp™) right angle locking header connector (WS G650-2004-7FB).

Matching connection: Molex 501939-0400 housing with Molex 501334-0000 crimp pins. WinSystems cables simplify connections to the board:

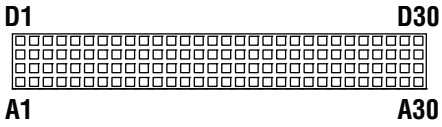
- CBL-LED3-000-14A: Pico-Clasp to unterminated (shown)
- CBL-LED3-001-12B: Pico-Clasp to Pico-Clasp



7.8.10 J12 PC/104-Plus (PCI bus)

The PC/104-Plus is electrically equivalent to the 33 MHz PCI bus. Interface is PC/104-Plus version 2.0 compliant.

Layout and Pin Reference:



Pin	A	B	C	D
1	GND	RESERVED	+5V	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD007	GND	AD06
5	GND	AD009	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1#	AD15	+3.3V
9	SERR#	GND	RESERVED	PAR
10	GND	PERR#	+3.3V	RESERVED
11	STOP#	+3.3V	LOCK#	GND
12	+3.3V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	+3.3V
14	GND	AD16	+3.3V	C/BE2#
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0#	GND	REQ1#	VI/O
24	GND	REQ2#	+5V	GNT0#
25	GNT1#	VI/O	GNT2#	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD#	+5V	RST#
29	+12V	INTA#	INTB#	INTC#
30	-12V	REQ3#	GNT3#	GND

= Active Low Signal

Shaded cells indicate power pins.

Additional Information

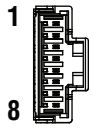
No keys in connector and no cut pins. This connection uses different connectors for stack-through or non-stack-through models:

120 Pin Connector:

- Teka 2MR430-BDWM-368-00 (non-stack-through, solder bearing), WS G650-0120-0BA
- Teka 2MR430-A7WM-368-0 (stack-through, solder bearing), WS G650-0120-09A

7.8.11 J500 Backlight

Layout and Pin Reference:



Pin	Name	Description
1	V5	+5V Power
2	BKLT_EN_N	Backlight Enable -
3	BKLT_EN	Backlight Enable +
4	GND	Ground
5	V12+	+12V Power
6	BKLT_PWM	Backlight PWM Brightness Control
7	V3P3S	+3.3V Power
8	V5	+5V Power

The backlight interface terminates at a Molex 501568-0807, 1x8, 1 mm pitch (Pico-Clasp™) vertical locking header connector (WS G650-2008-6F0).

Matching connector: Molex 501330-1100 with Molex 501334-0000 crimp pins.

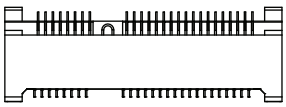
WinSystems cables simplify connections to the board:

- CBL-LVDSAB-005-12: LVDS/Audio & Backlight to 7" Ampire with Audio Jacks
- CBL-LVDSB-006-12: LVDS & Backlight to 7" Ampire without Audio
- CBL-LVDSAB-003-12: LVDS/Audio & Backlight to 6.5" AUO with Audio Jacks

7.8.12 J501 Mini-PCIe/mSATA Connector

The PPM-C407 provides a mini-PCIe socket to support a variety of peripherals as available in this format. The socket alternatively supports a mSATA device in this socket. A sense circuit identifies the type of device present in the socket and auto-switches to handle either type.

Layout and Pin Reference:

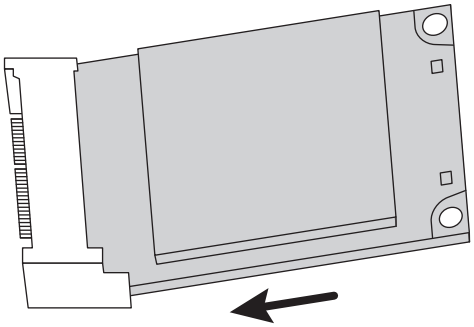


Pin	Name	Pin	Name
1	WAKE#	2	3.3Vaux
3	COEX1	4	GND
5	COEX2	6	1.5V
7	CLKREQ#	8	UIM_PWR
9	GND	10	UIM_DATA
11	REFCLK-	12	UIM_CLK
13	REFCLK+	14	UIM_RST
15	GND	16	UIM_VPP
17	RSVD(UIM_C8)	18	GND
19	RSVD(UIM_C4)	20	W_DISABLE#
21	GND	22	PERST#
23	PERn0	24	3.3Vaux
25	PERp0	26	GND
27	GND	28	1.5V
29	GND	30	SMB_CLK
31	PERn0	32	SMB_DATA
33	PERp0	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	3.3Vaux	40	GND
41	3.3Vaux	42	LED_WWAN#
43	GND	44	LED_WLAN#
45	RSVD	46	LED_WPAN#
47	RSVD	48	1.5V
49	RSVD	50	GND
51	MSATA DET	52	3.3Vaux

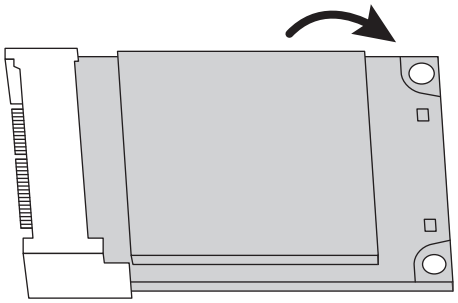
Shaded cells indicate unconnected signals.

To install a miniPCIe/mSATA into J501:

1. Insert the miniPCIe/mSATA



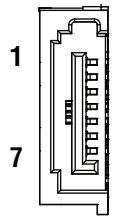
2. Push the free end of the card toward the circuit board and then secure it with two (2 mm) screws (WinSystems P/N: G527-0000-400).



7.8.13 J503 Serial ATA (SATA)

The PPM-C407 provides a SATA interface to support connection of a variety of SATA devices.

Layout and Pin Reference:

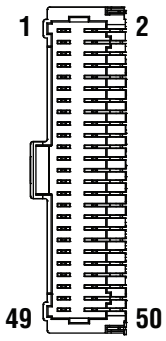
	Pin	Name
	1	GND
	2	A+
	3	A-
	4	GND
	5	B-
	6	B+
	7	GND

The SATA interface terminates at an industry standard 7-pin, right angle SATA connector Molex 47080-4005 (WS G650-7007-600). WinSystems cable CBL-SATA-701-20 simplifies connection to the board.

7.8.14 J504 Digital Input/Output

The PPM-C407 supports 24 lines of digital input/output (DIO) via the Lattice MachX02 FPGA interfaced to the processor with the Low Pin Count (LPC) interface. These lines maintain the WinSystems standard DIO register definition and by using the TI TXS0108E level converters, all signals are 5 V tolerant.

Layout and Pin Reference:



Pin	Name	Pin	Name
1	Port 2 Bit 7	2	GND
3	Port 2 Bit 6	4	GND
5	Port 2 Bit 5	6	GND
7	Port 2 Bit 4	8	GND
9	Port 2 Bit 3	10	GND
11	Port 2 Bit 2	12	GND
13	Port 2 Bit 1	14	GND
15	Port 2 Bit 0	16	GND
17	Port 1 Bit 7	18	GND
19	Port 1 Bit 6	20	GND
21	Port 1 Bit 5	22	GND
23	Port 1 Bit 4	24	GND
25	Port 1 Bit 3	26	GND
27	Port 1 Bit 2	28	GND
29	Port 1 Bit 1	30	GND
31	Port 1 Bit 0	32	GND
33	Port 0 Bit 7	34	GND
35	Port 0 Bit 6	36	GND
37	Port 0 Bit 5	38	GND
39	Port 0 Bit 4	40	GND
41	Port 0 Bit 3	42	GND
43	Port 0 Bit 2	44	GND
45	Port 0 Bit 1	46	GND
47	Port 0 Bit 0	48	GND
49	+5 V	50	GND

The I/O is terminated at a Molex 501571-5007, 2x25, 1 mm pitch (Pico-Clasp™) right angle locking header connector (WS G650-2050-7HB).

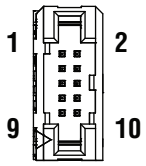
Matching connector: The mate is the Molex 501189-5010 housing with Molex 501193-2000 crimp pins. WinSystems cables simplify connections to the board:

- CBL-DIO24-000-14: Pico-Clasp to unterminated
- CBL-DIO24-001-12: Pico-Clasp to Pico-Clasp
- CBL-DIO24-002-12: Pico-Clasp to 2x25, 0.1" pitch housing

7.8.15 J505 Ethernet

The PPM-C407 has an Intel® i210 single chip 1 Gb/s Ethernet Controller that includes full magnetics (Bothhand GST5009) and surge suppression.

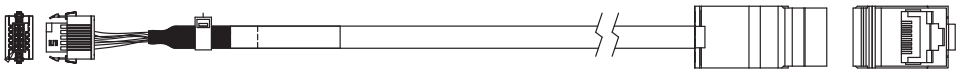
Layout and Pin Reference:

	Pin	Name	Pin	Name
	1	MX0_P	2	MX0_N
	3	MX1_P	4	MX1_N
	5	MX2_P	6	MX2_N
	7	MX3_P	8	MX3_N
	9	NC	10	NC

The Ethernet connection is a Samtec TFM-105-02-L-DH, 2x5, 0.05" pitch locking header connector (WS G650-2010-5H0A).

Matching connector: Samtec ISDF-05-D-M housing with Samtec CC03L-2830-01-G crimp pins. WinSystems cables simplify connection to the board:

- CBL-ENET1-302-12: RJ45 Jack (shown)
- CBL-ENET1-303-12: RJ45 Plug



7.9 Jumpers

Jumper Part Number SAMTEC 2SN-BK-G applies to all jumpers. These are available in a ten piece kit from WinSystems (Part# KIT-JMP-G-200).

7.9.1 JP1 AT/ATX Power Mode

The presence of a jumper at JP1 specifies the style of supply connected to the single board computer (see “J1 Power Connector” on page 16). AT Power is a simple on/off power supply with no interaction with the single board computer. Most embedded systems use this type of power supply (default setting).

Purpose: Specifies the style of power supply connected

Jumper Pin Reference:

	Jumper	AT / ATX Mode Select
	1-2	Jumper Installed: AT Mode (Default)
	Open	Open (no jumper installed): ATX Mode

7.9.2 JP3 Basic Input/Output System (BIOS) Programming Defaults

If you have saved EEPROM values that prevent you from accessing BIOS menus, the board can be reset to factory defaults as follows:

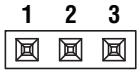
1. Turn the system off.
2. Install the jumper at **JP3**.
3. Turn the system on and enter the **BIOS Main Menu** using the **F2** key. Factory defaults will be loaded at this point.
4. Remove the jumper on **JP3**.
5. Select **Exit Saving Changes** from the **Exit Menu**.

Jumper Pin Reference:

	Jumper	Defaults Mode
	1-2	Jumper Installed: Boot using BIOS defaults
	Open	Open (no jumper installed): Boot using presently saved BIOS settings

7.9.3 JP4 Low-Voltage Differential Signaling (LVDS)

The presence and position of a jumper at JP4 configures the J5 connector (see “J5 LVDS and Audio Connector” on page 20) for the Video Electronics Standards Association (VESA) or the Japan Electronic Industry Development Association (JEIDA) standard, and bits-per-pixel (bpp).

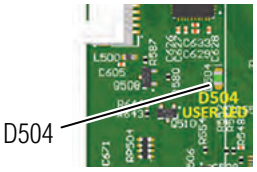
	Jumper	LVDS setting
	1-2	18-bpp VESA or JEIDA (default)
	2-3	24-bpp VESA
	Open	24-bpp JEIDA

7.10 LED Indicators

	LED	Description
	D7	Indicates when an Ethernet activity occurs
	D9	Indicates when the board is in stand-by power states (S3, S4, or S5)
	D10	Indicates when the board is in the run power state (S0) and all power supplies are good
	D504	Indicates when a user defined event occurs. For location and details, see “D504 User LED” on page 34.

7.10.1 D504 User LED

A user LED (D504) can be used for any application specific purpose. The LED can be turned on in software applications by writing a 1 to I/O port 29DH. The LED can be turned off by writing a 0 to 29DH.



8. BIOS

8.1 General Information

The PPM-C407 includes a BIOS from Phoenix Technologies to assure full compatibility with PC operating systems and software. The basic system configuration is stored in battery backed CMOS RAM within the clock/calendar. As an alternative, the CMOS configuration may be stored in EEPROM for operation without a battery. For more information of CMOS configuration, see the BIOS Settings Storage Options section of this manual. Access to this setup information is via the Setup Utility in the BIOS.

8.2 Entering Setup

To enter setup, power up the computer and press F2 when either the splash screen is displayed or when the **Press F2 for Setup** message is displayed. It may take a few seconds before the main setup menu screen is displayed.

8.3 Navigation of the Menus

Use the Up and Down arrow keys to move among the selections and press **Enter** when a selection is highlighted to enter a sub-menu or to see a list of choices. See “BIOS Screens” on page 36 for available options.

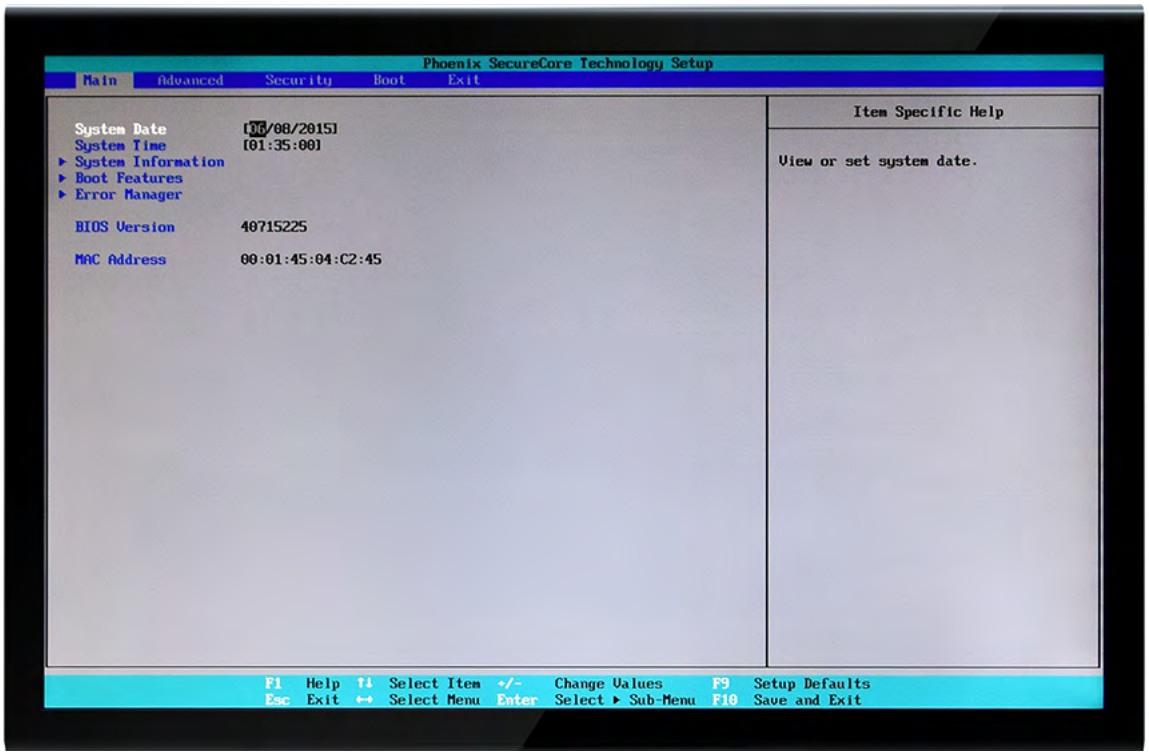
8.4 BIOS Splash Screen

Custom BIOS Splash Screens can be accommodated for OEM customers. Please contact one of our Application Engineers for details.

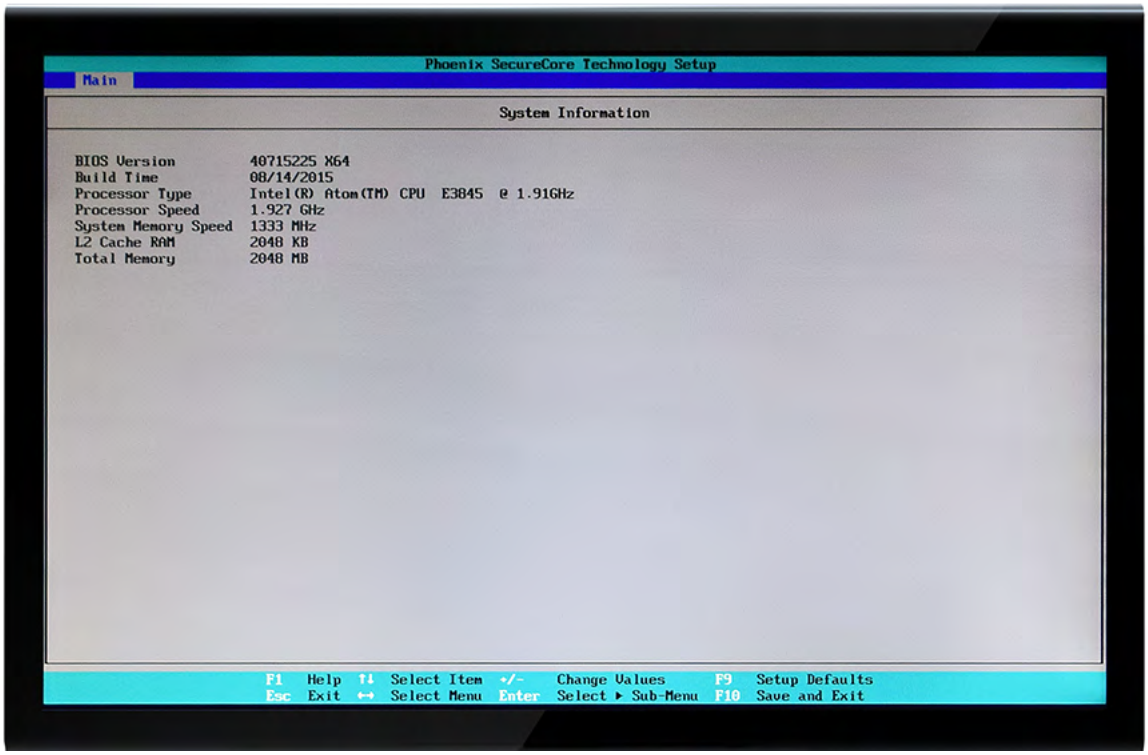
8.5 BIOS Screens

The following BIOS screens contain the options and sample settings for the PPM-C407. Your actual configuration may differ from the screens shown here. Use care when modifying BIOS settings.

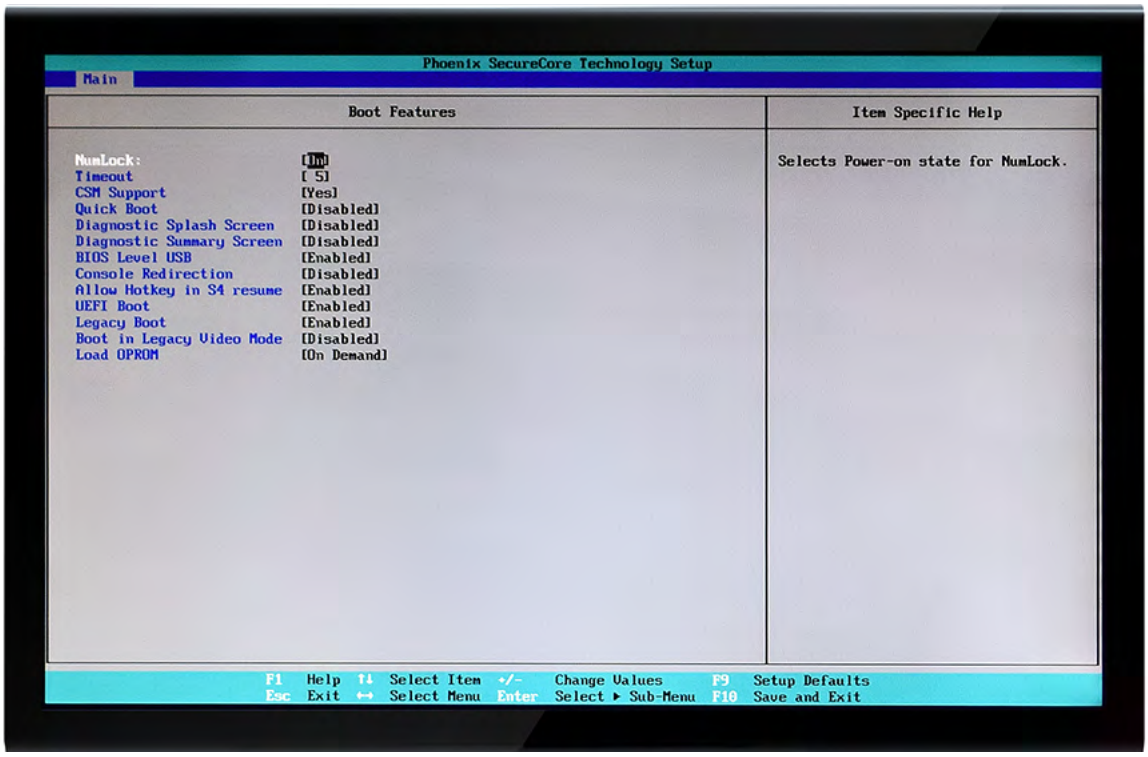
Main



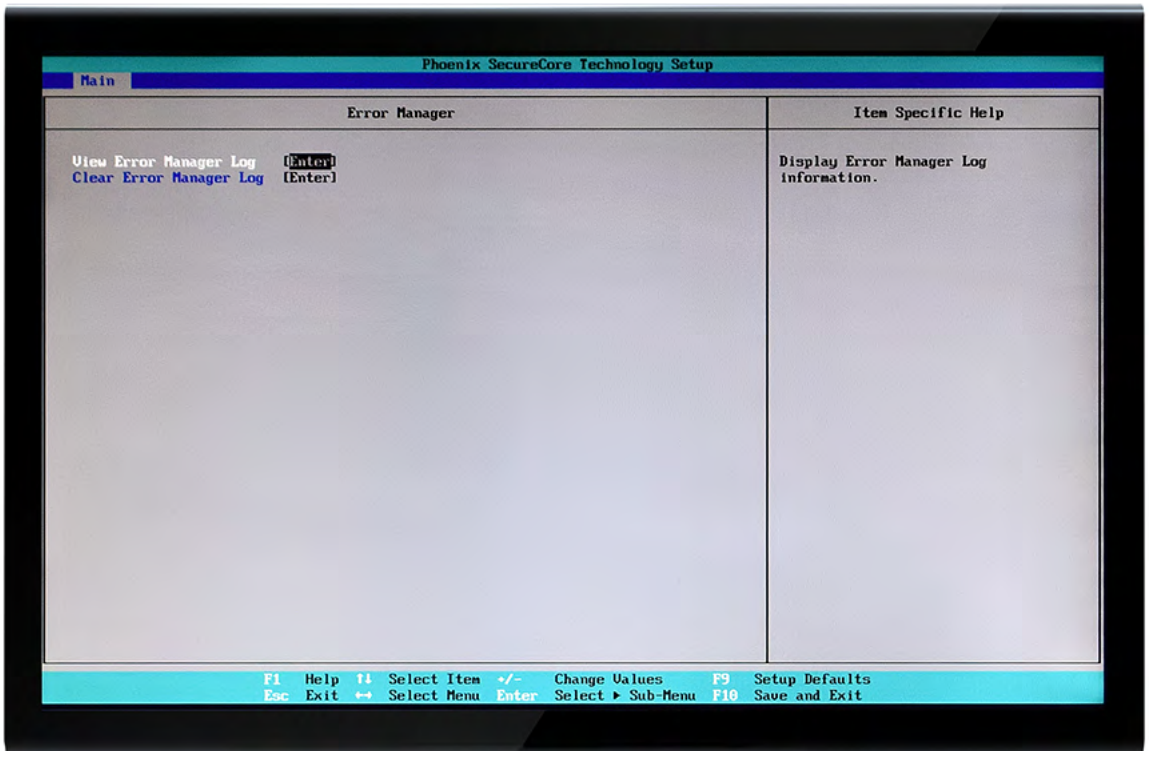
Main: System Information



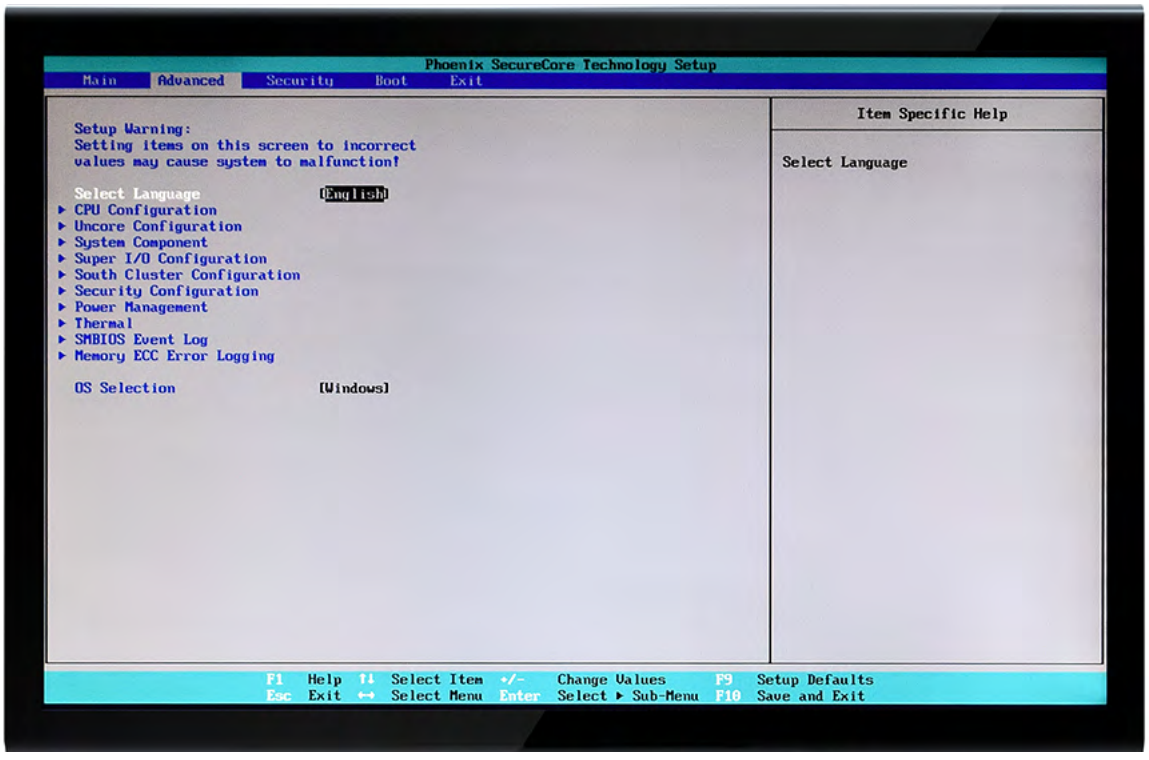
Main: Boot Features



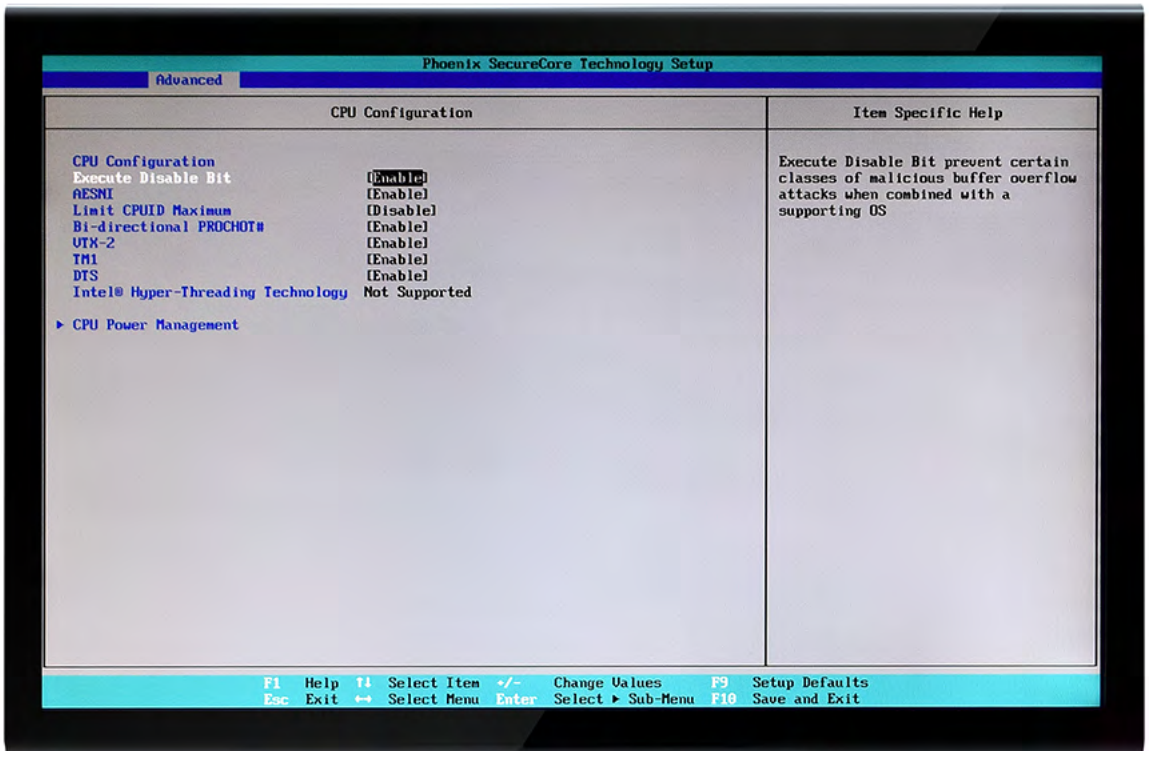
Main: Error Manager



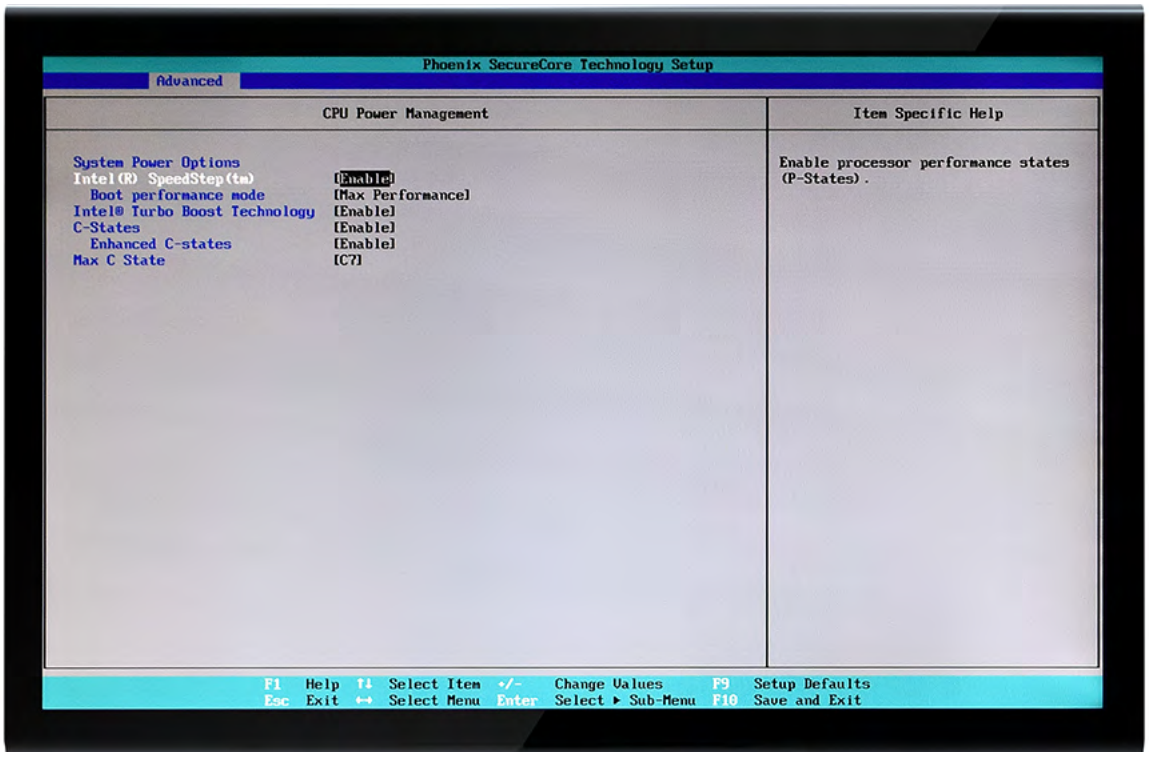
Advanced



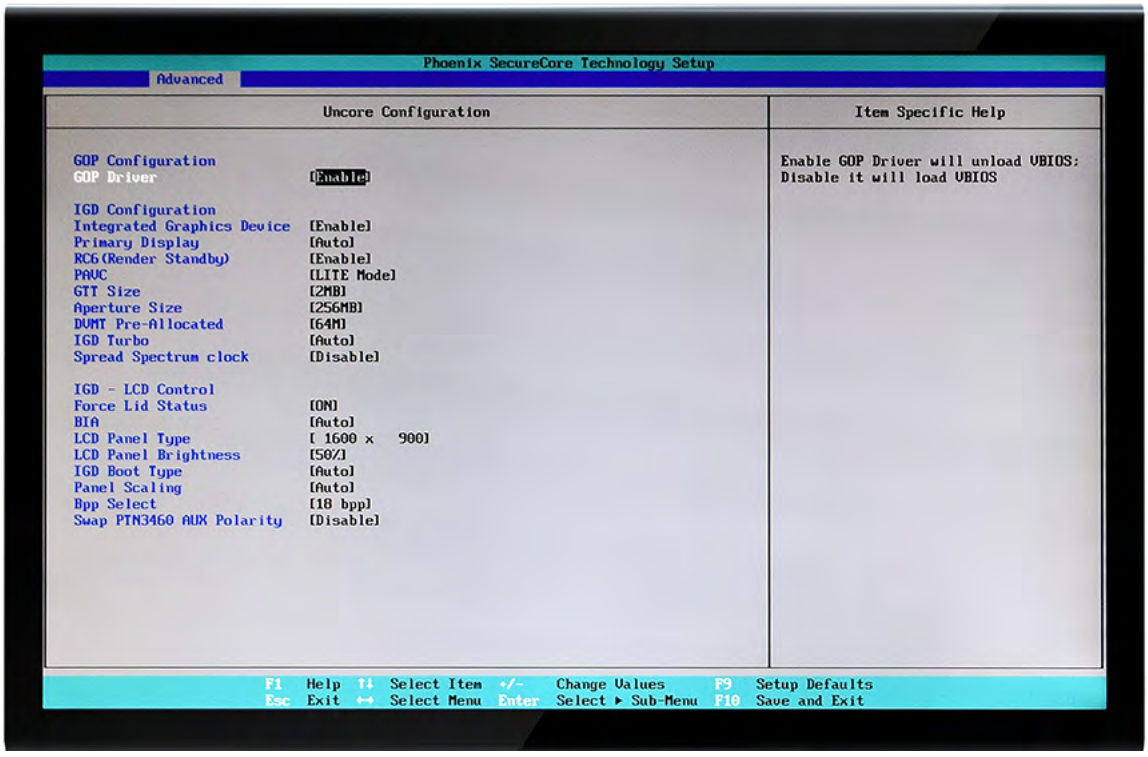
Advanced: CPU Configuration



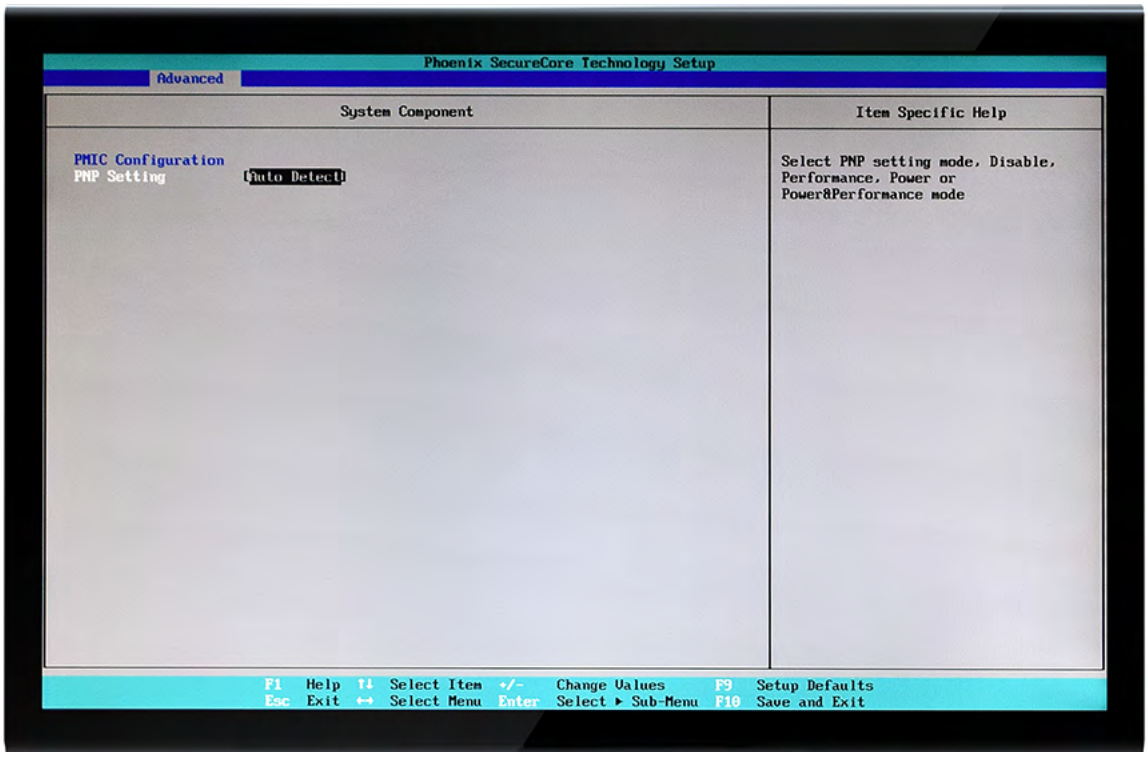
Advanced: CPU Configuration: CPU Power Management



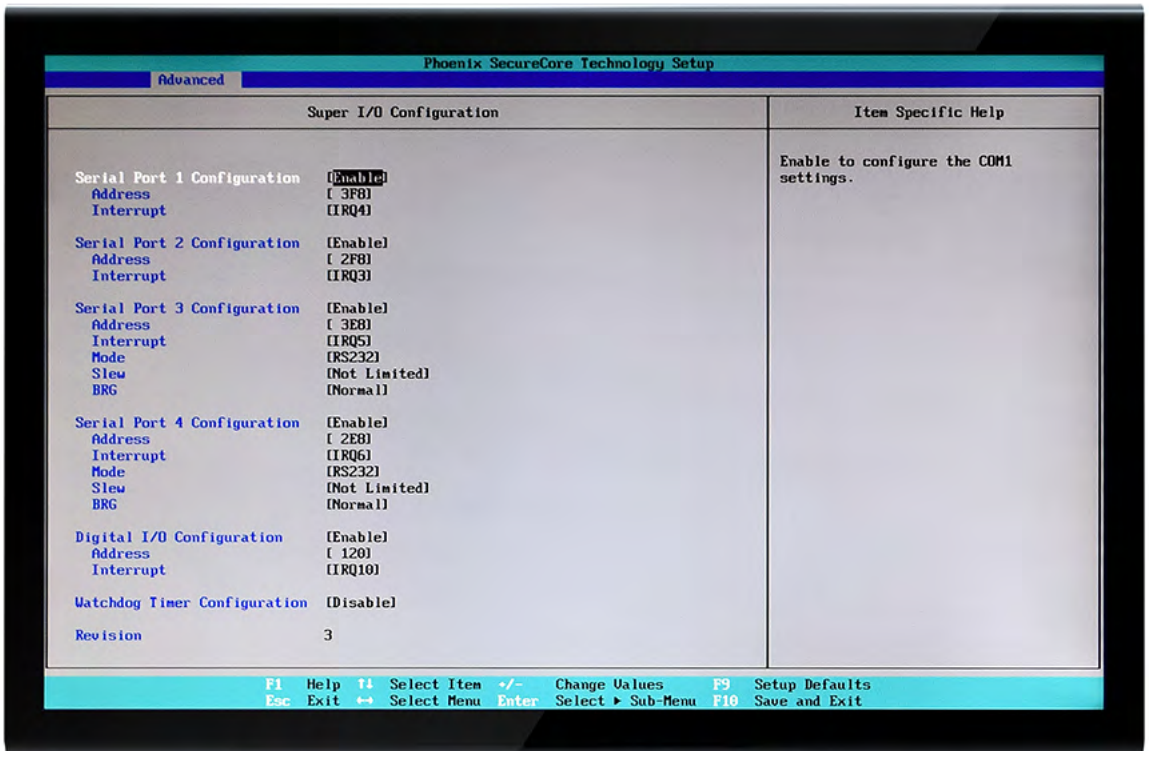
Advanced: Uncore Configuration



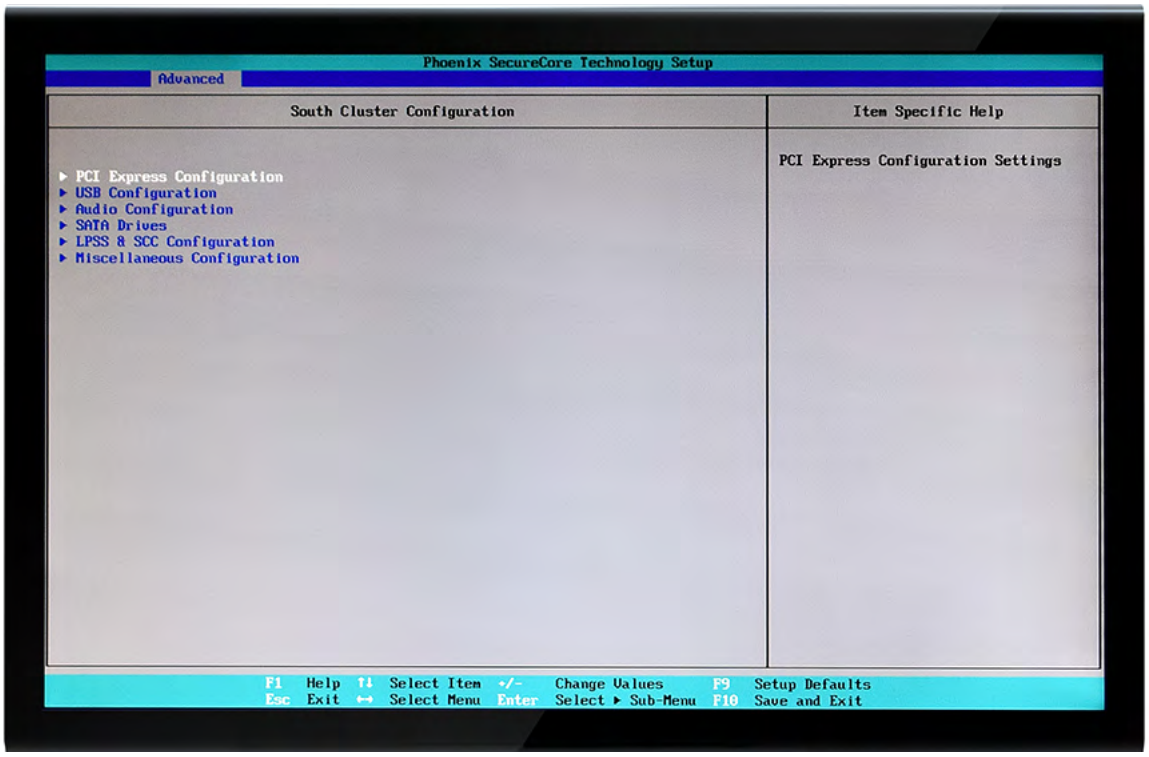
Advanced: System Component



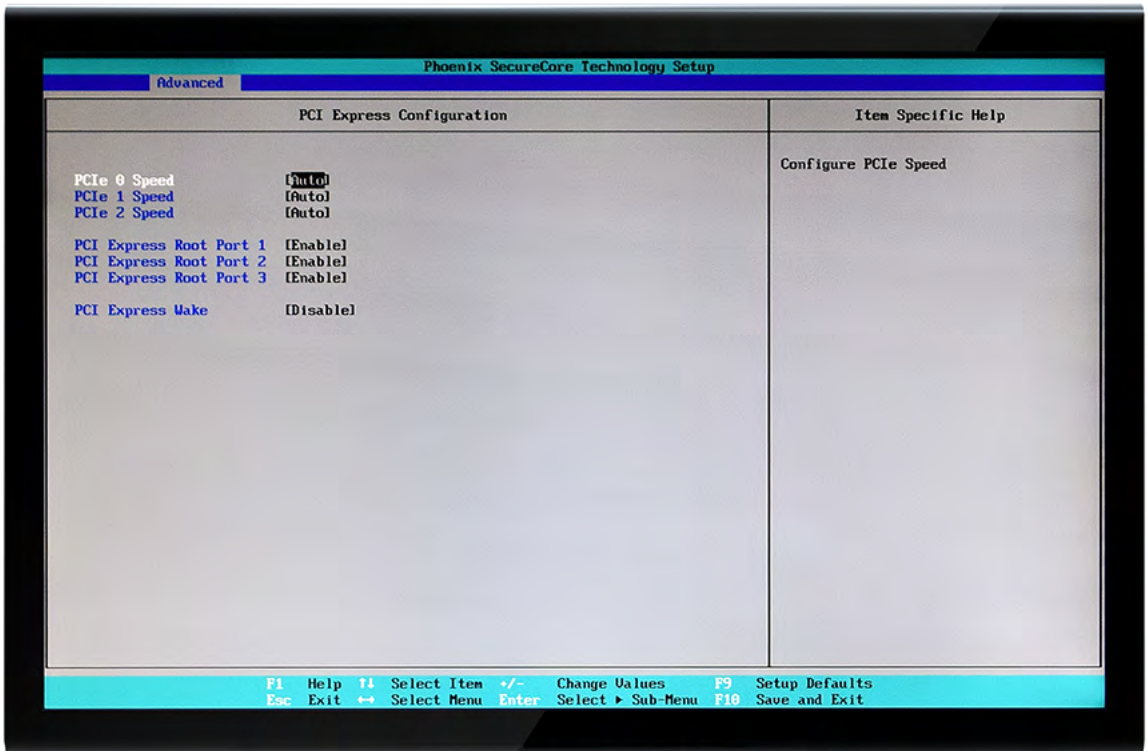
Advanced: Super I/O Configuration



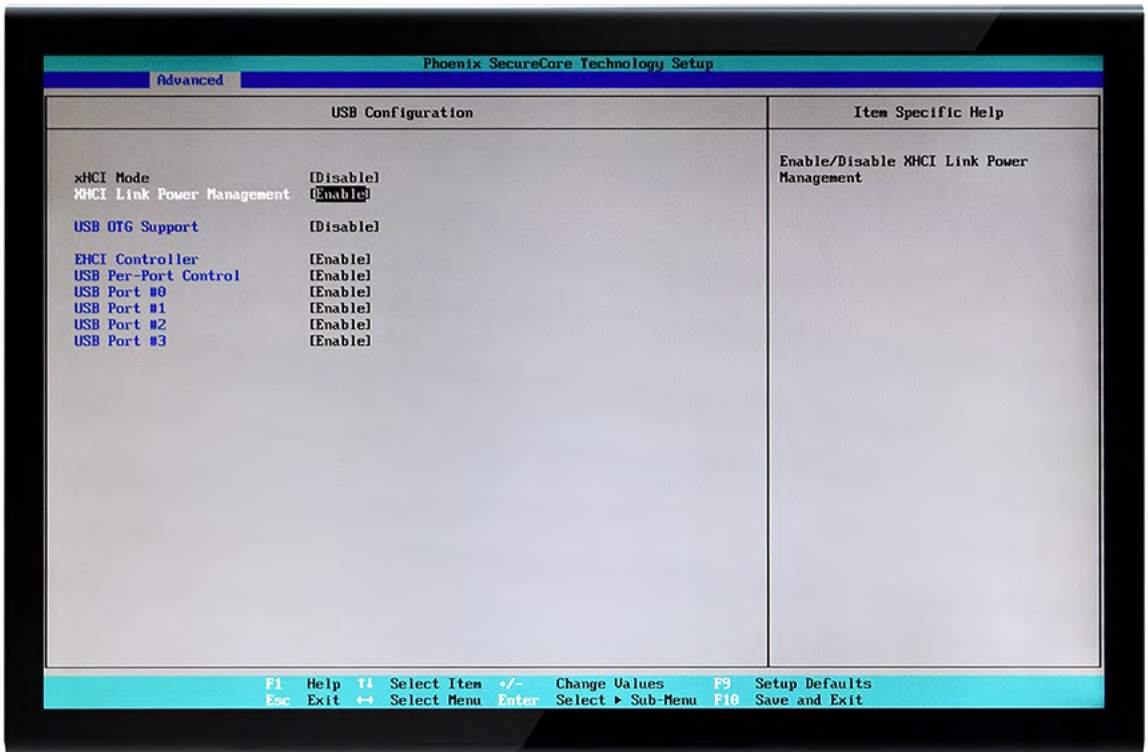
Advanced: South Cluster Configuration



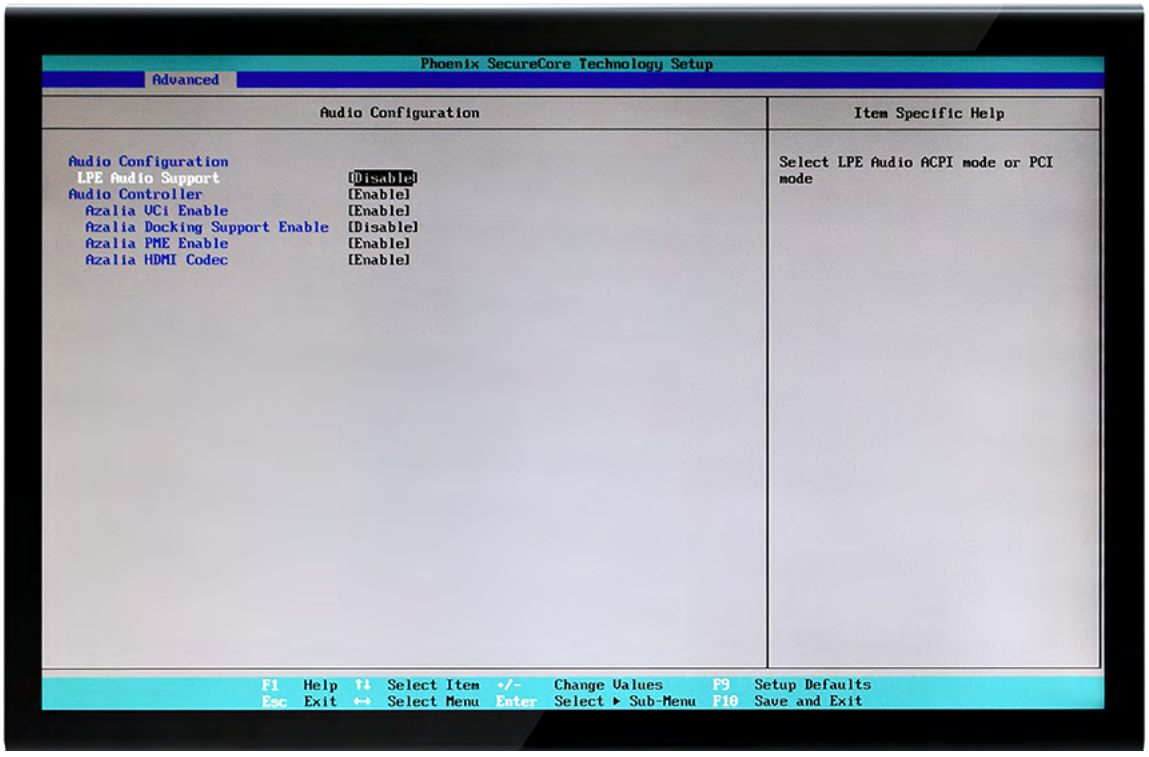
Advanced: South Cluster Configuration: PCI Express Configuration



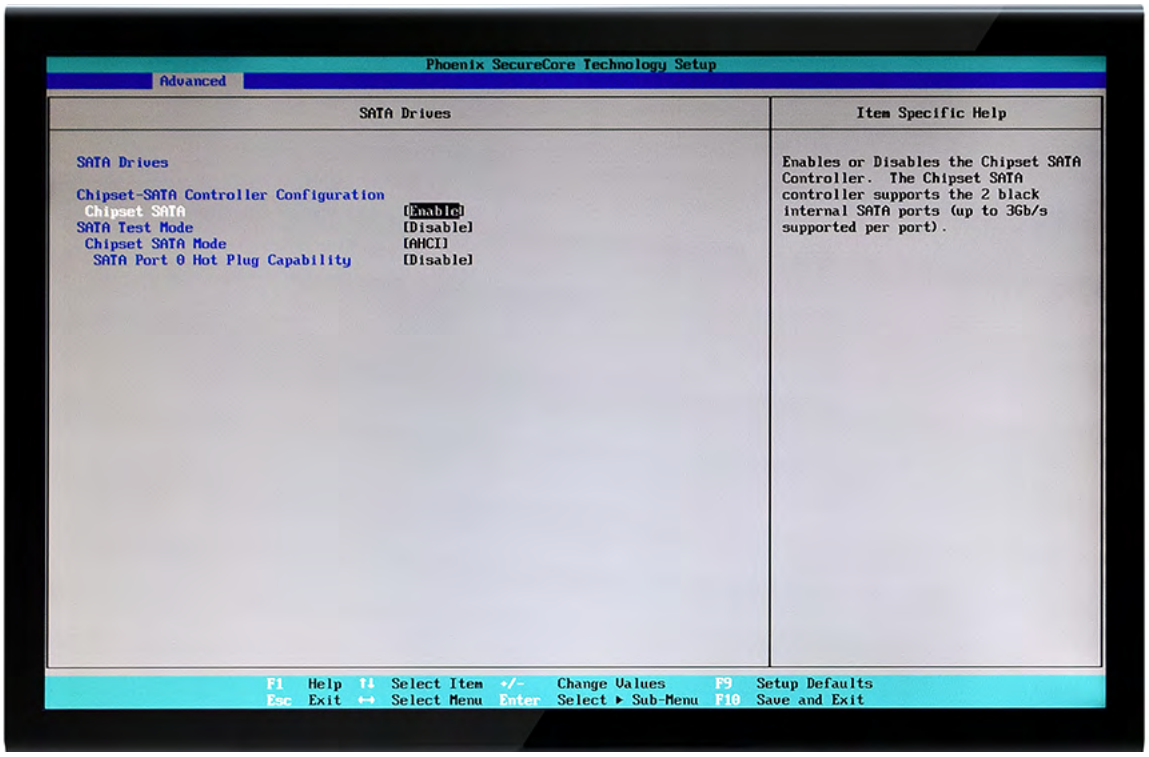
Advanced: South Cluster Configuration: USB configuration



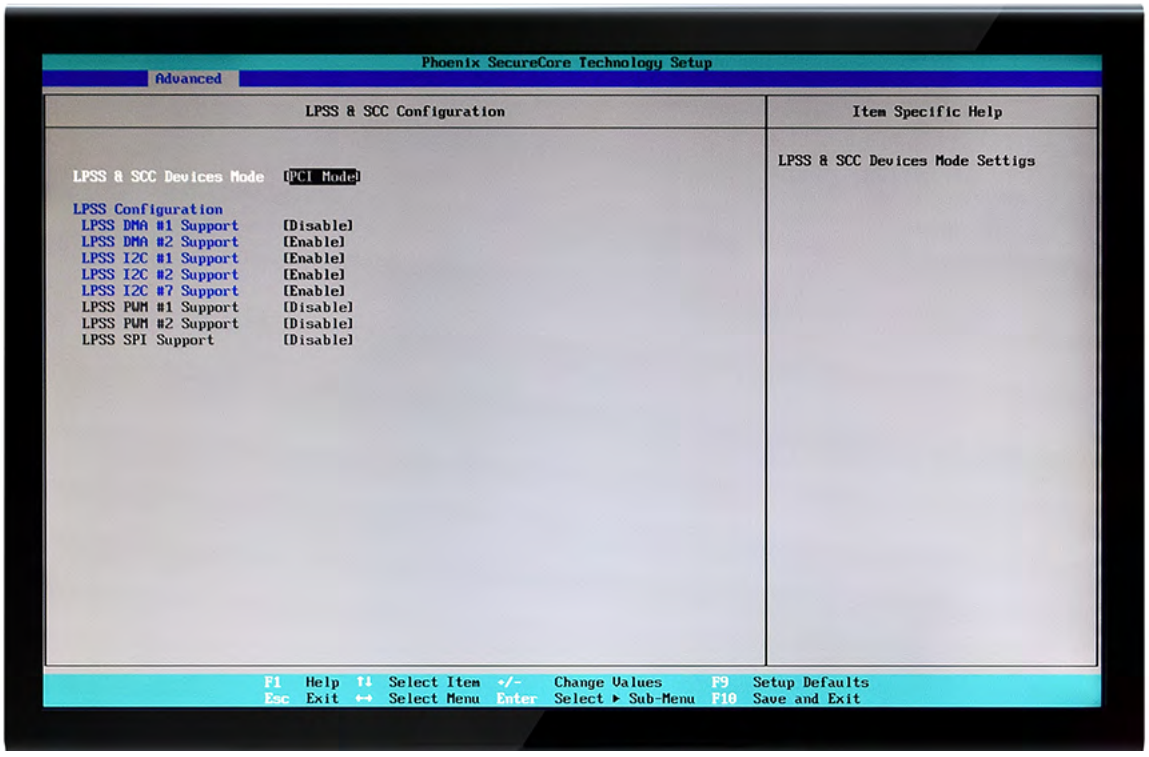
Advanced: South Cluster Configuration: Audio Configuration



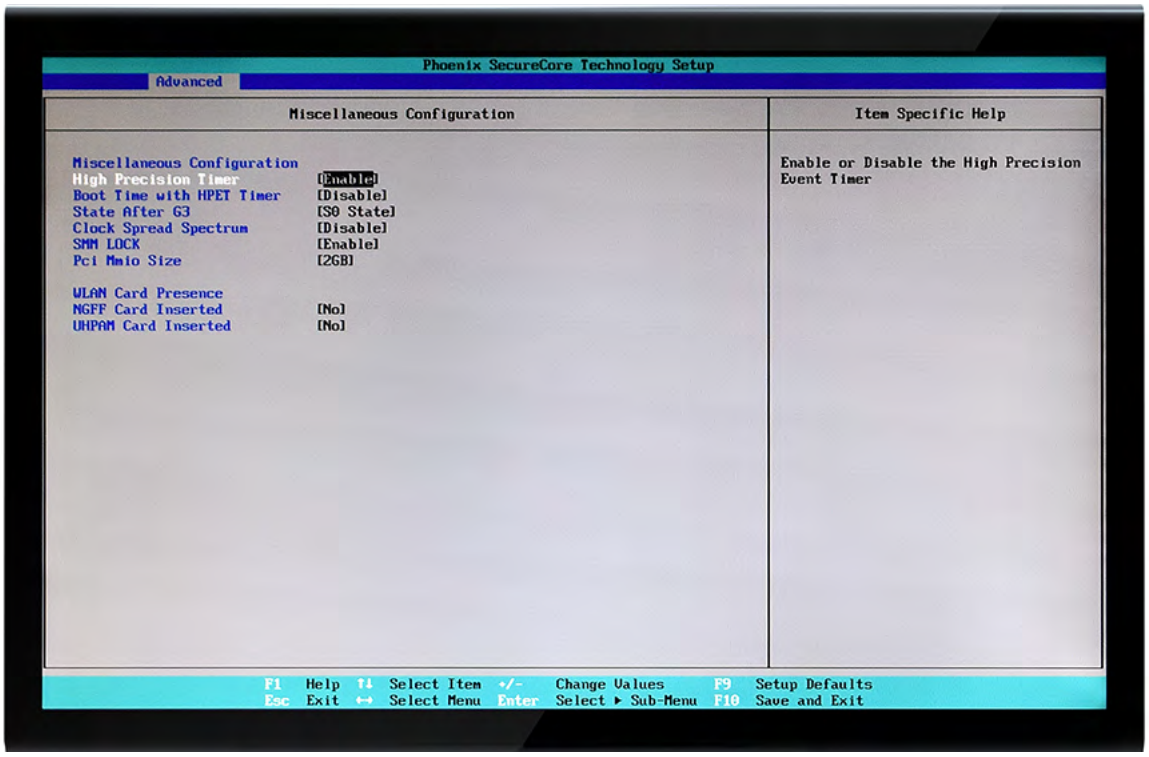
Advanced: South Cluster Configuration: SATA Drives



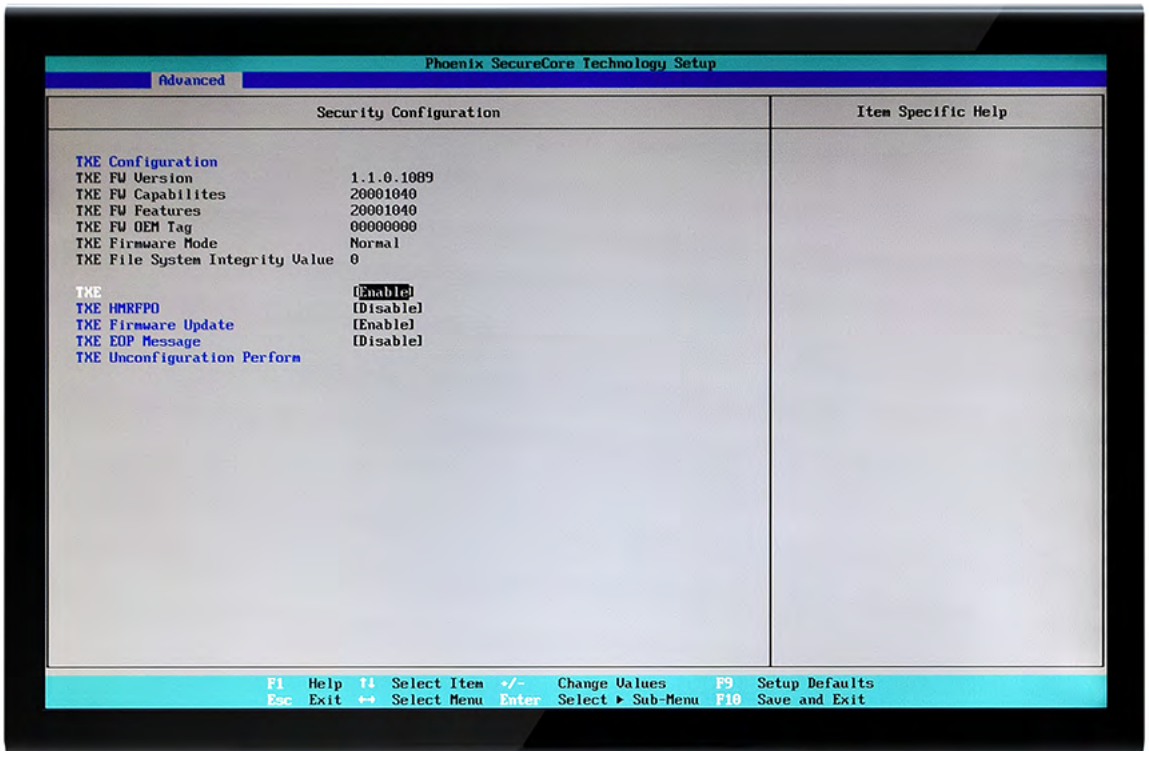
Advanced: South Cluster Configuration: LPSS & SCC Configuration



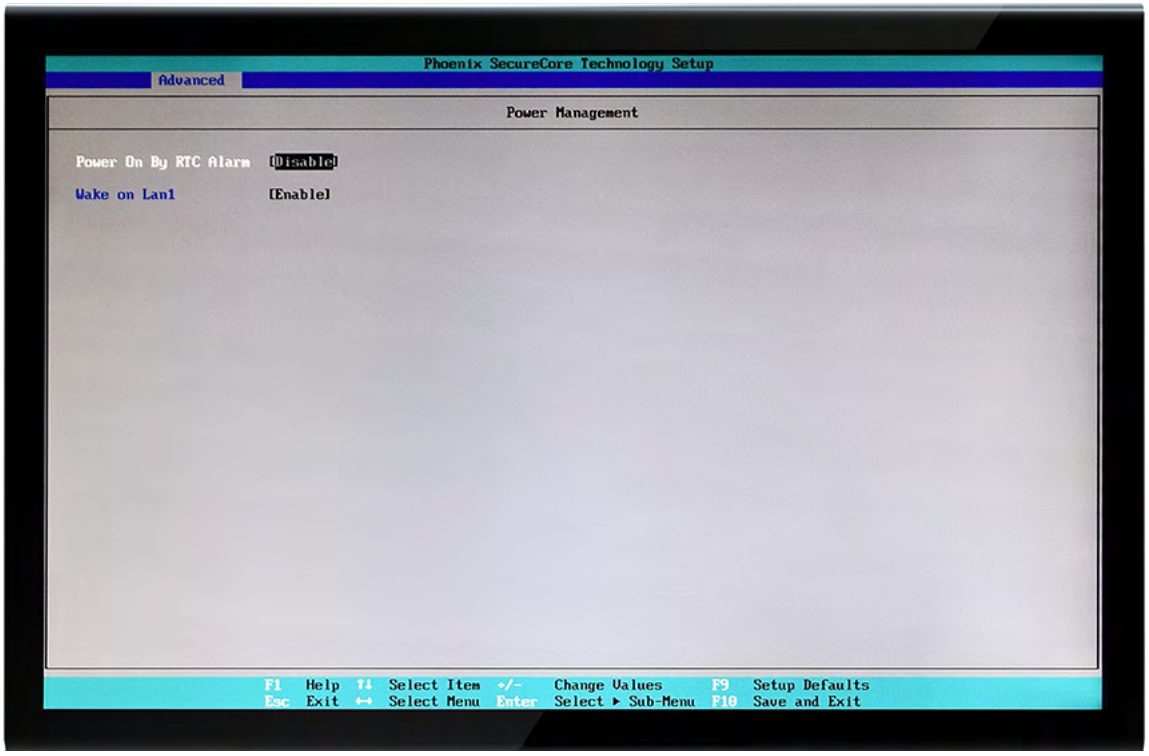
Advanced: South Cluster Configuration: Miscellaneous Configuration



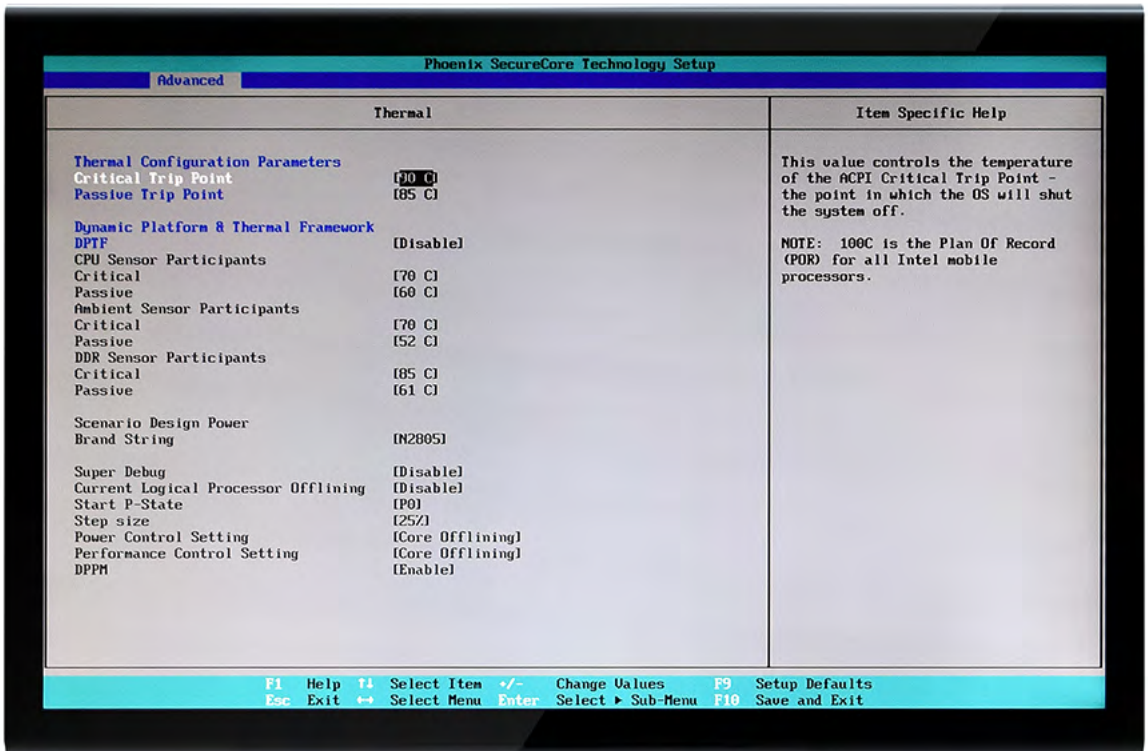
Advanced: Security Configuration



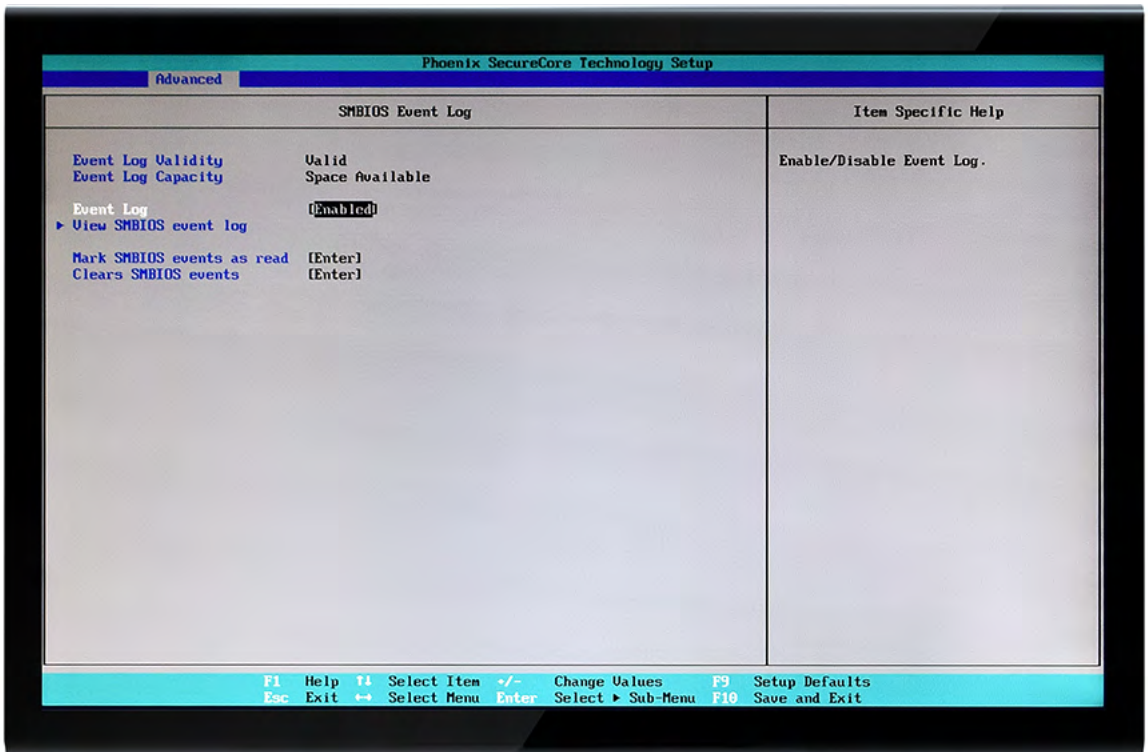
Advanced: Power Management



Advanced: Thermal Configuration

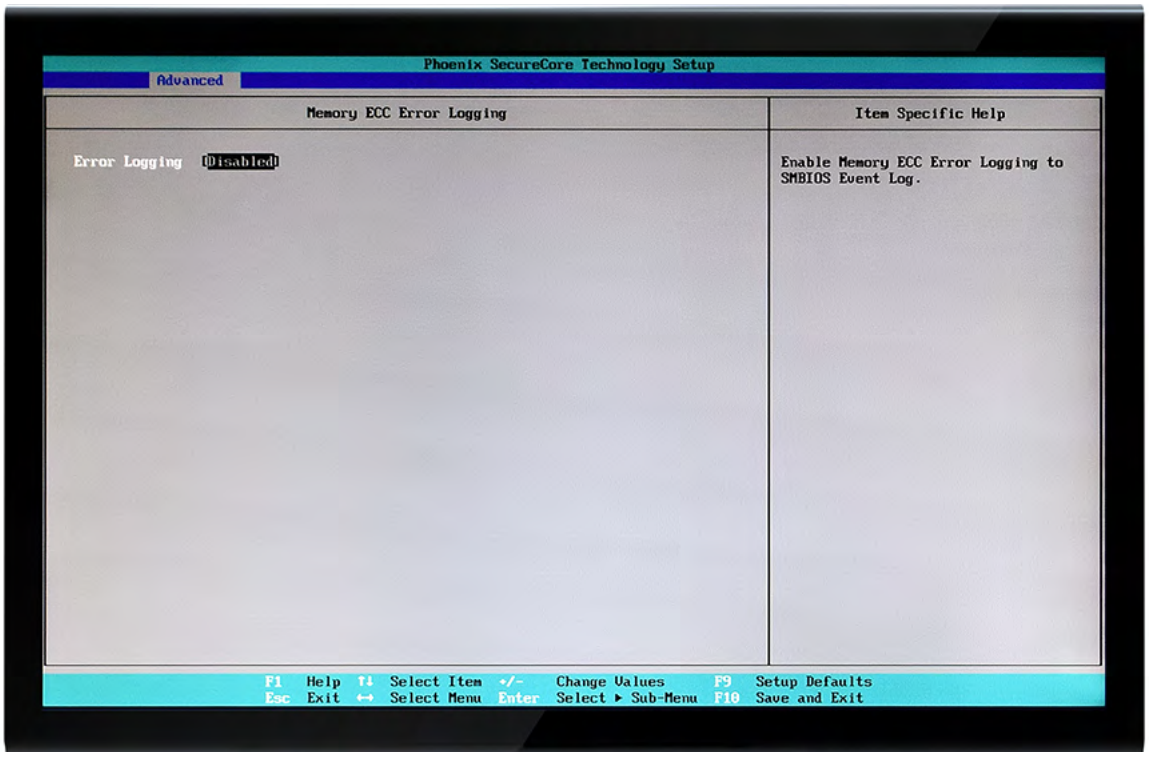


Advanced: SMBIOS Event Log

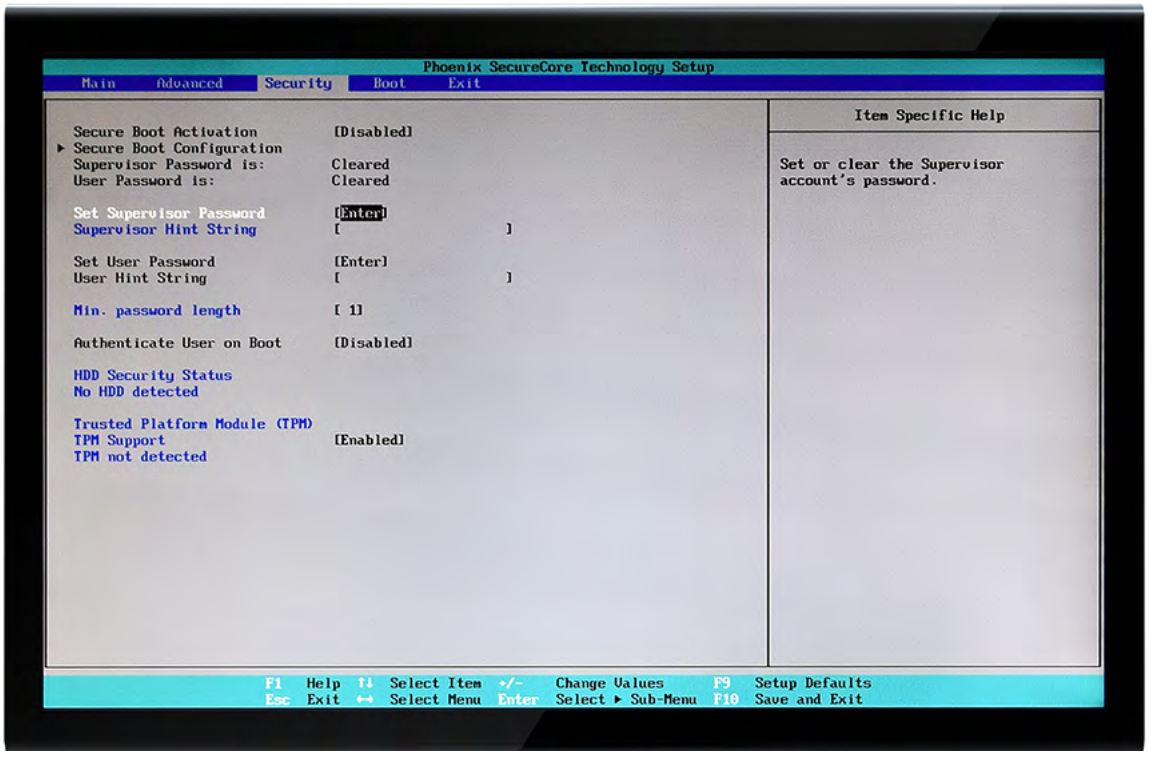


Advanced: SMBIOS Event Log: View SMBIOS event log

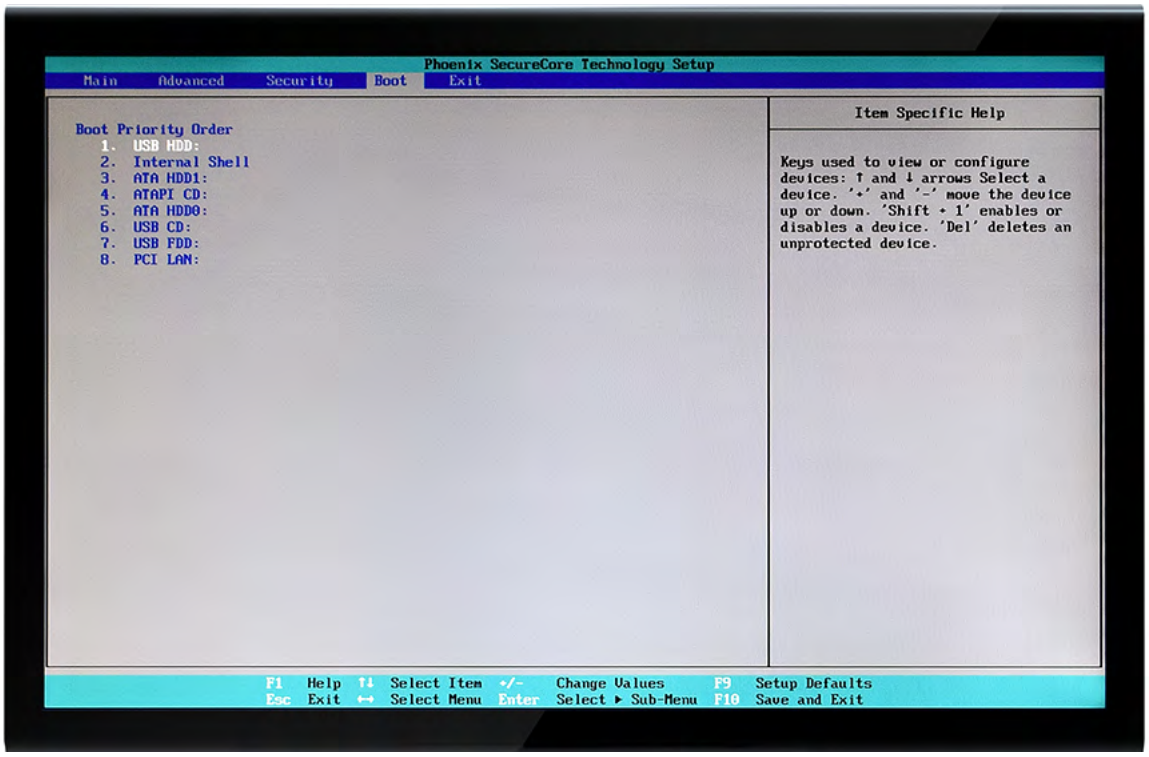
Advanced: Memory ECC Error Logging



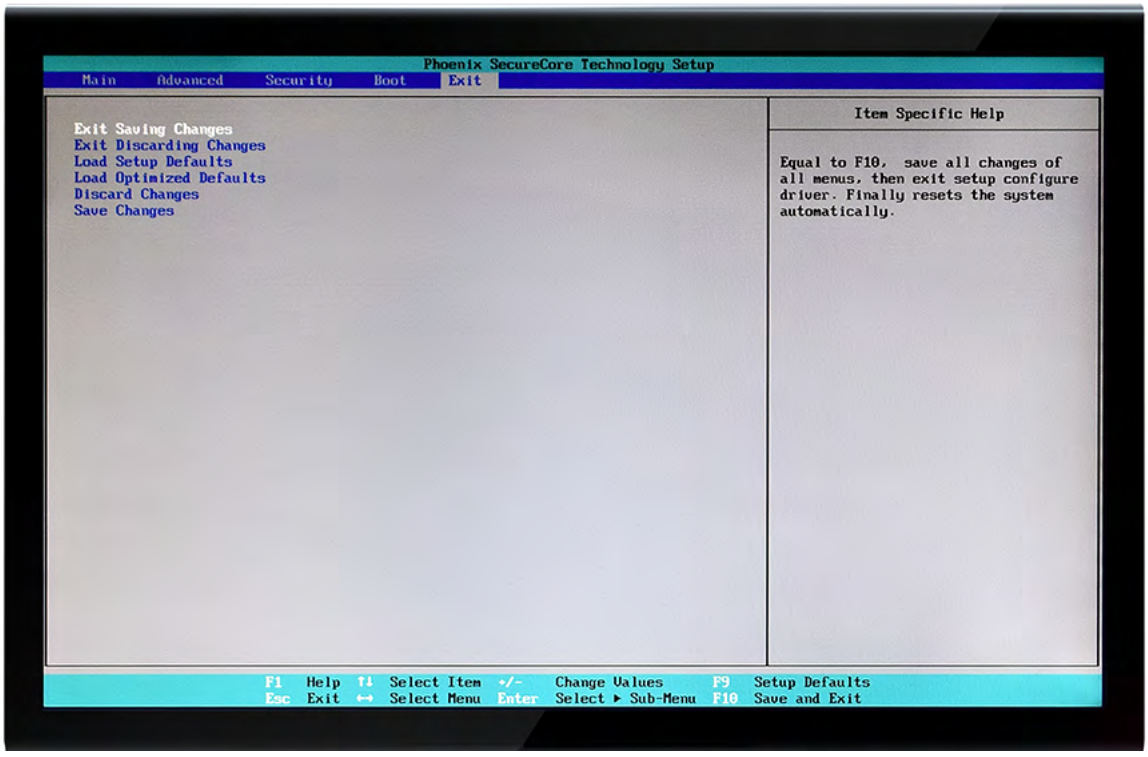
Security



Boot



Exit


Phoenix SecureCore Technology Setup
Main Advanced Security Boot Exit
Exit Saving Changes
Exit Discarding Changes
Load Setup Defaults
Load Optimized Defaults
Discard Changes
Save Changes
Item Specific Help
Equal to F10, save all changes of all menus, then exit setup configure driver. Finally resets the system automatically.
F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults
Esc Exit ↔ Select Menu Enter Select ▸ Sub-Menu F10 Save and Exit

9. Cables

WinSystems cables and batteries simplify connection to the PPM-C407. The following table lists available items.

Item	Part Number	Connection	Description
Cables	CBL-PWR-700-18	See “J1 Power Connector” on page 16.	Power connection
	CBL-LVDSAB-005-12	See “J5 LVDS and Audio Connector” on page 20.	LVDS/Audio and Backlight to 7" Ampire with Audio Jacks
	CBL-LVDSB-006-12		LVDS and Backlight to 7" Ampire without Audio
	CBL-LVDSA-007-12		LVDS/Audio to 12" Mitsubishi with Audio Jacks
	CBL-LVDSA-008-12		LVDS to 12" Mitsubishi without Audio
	CBL-LVDSAB-003-12		LVDS/Audio & Bklt to 6.5" AUO with Audio Jacks
	CBL-SPL-001-14		LVDS/Audio to unterminated LVDS with Audio Jacks
	CBL-VGA-002-12	See “J7 VGA” on page 22.	
	CBL-USB4-000-14:	See “J8 USB” on page 23.	Pico-Clasp to unterminated
	CBL-USB4-001-12:		Pico-Clasp to Pico-Clasp
	CBL-USB4-002-12		Pico-Clasp to 2each, 2x4, 2 mm pitch housing
	CBL-SER4-000-14	See “J9 Serial Ports” on page 24.	Duo-Clasp to unterminated
	CBL-SER4-001-12		Duo-Clasp to Duo-Clasp
	CBL-SER4-002-12		Duo-Clasp to 4xDB9.
	CBL-LED3-000-14A	See “J11 Ethernet External LEDs” on page 26.	Pico-Clasp to unterminated
	CBL-LED3-001-12B		Pico-Clasp to Pico-Clasp
	CBL-LVDSAB-005-12	See “J500 Backlight” on page 28.	LVDS/Audio and Backlight to 7" Ampire with Audio Jacks
	CBL-LVDSB-006-12		LVDS and Backlight to 7" Ampire without Audio
	CBL-LVDSAB-003-12		LVDS/Audio and Backlight to 6.5" AUO with Audio Jacks
	CBL-SATA-701-20	See “J503 Serial ATA (SATA)” on page 30.	SATA interface
	CBL-DIO24-000-14	See “J504 Digital Input/Output” on page 31.	Pico-Clasp to unterminated
	CBL-DIO24-001-12		Pico-Clasp to Pico-Clasp
	CBL-DIO24-002-12		Pico-Clasp to 2x25, 0.1" pitch housing
	CBL-ENET1-302-12	See “J505 Ethernet” on page 32.	RJ45 Jack
	CBL-ENET1-303-12		RJ45 Plug
Batteries	BAT-LTC-E-36-16-2	See “J4 External Battery Connector” on page 19.	External 3.6V, 1650 mAH battery with plug-in connector
	BAT-LTC-E-36-27-2		External 3.6V, 2700 mAH battery with plug-in connector

10. Software Drivers

Go to www.winsystems.com for information on available software drivers.

Appendix A. Best Practices

The following paragraphs outline the best practices for operating the PPM-C407 in a safe, effective manner, that will not damage the board. Please read this section carefully.

Power Supply

Avoid Electrostatic Discharge (ESD)—Only handle the circuit board and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

Power Supply Budget

Evaluate your power supply budget. It is usually good practice to budget twice the typical power requirement for all of your devices.

Zero-Load Power Supply

Use a zero-load power supply whenever possible. A zero-load power supply does not require a minimum power load to regulate. If a zero-load power supply is not appropriate for your application, then verify that the single board computer's typical load is not lower than the power supply's minimum load. If the single board computer does not draw enough power to meet the power supply's minimum load, then the power supply will not regulate properly and can cause damage to the PPM-C407.

Use Proper Power Connections (Voltage)—When verifying the voltage, measure it at the power connector on the PPM-C407. Measuring it at the power supply does not account for voltage drop through the wire and connectors.
The PPM-C407 requires +5V (±5%) to operate. Verify the power connections. Incorrect voltages can cause catastrophic damage.
Populate all of the +5V and ground connections. Most single board computers will have multiple power and ground pins, and all of them should be populated. The more copper connecting the power supply to the PPM-C407 the better.

Adjusting Voltage

If you have a power supply that allows you to adjust the voltage, it is a good idea to set the voltage at the power connector of the PPM-C407 to 5.1 V. The PPM-C407 can tolerate up to 5.25 V, so setting your power supply to provide 5.1 V is safe and allows for a small amount of voltage drop that will occur over time as the power supply ages and the connector contacts oxidize.

Power Harness

Minimize the length of the power harness. This will reduce the amount of voltage drop between the power supply and the PPM-C407.

Gauge Wire

Use the largest gauge wire that you can. Most connector manufacturers have a maximum gauge wire they recommend for their pins. Try going one size larger; it usually works and the extra copper will help your system perform properly over time.

Contact Points

WinSystems' boards mostly use connectors with gold finish contacts. Gold finish contacts are used exclusively on high speed connections. Power and lower speed peripheral connectors may use a tin finish as an alternative contact surface. It is critical that the contact material in the mating connectors is matched properly (gold to gold and tin to tin). Contact areas made with dissimilar metals can cause oxidation/corrosion resulting in unreliable connections.

Pin Contacts

Often the pin contacts used in cabling are not given enough attention. The ideal choice for a pin contact would include a design similar to Molex's or Trifurcon's design, which provides three distinct points to maximize the contact area and improve connection integrity in high shock and vibration applications.

Power Down

Make sure that power has been removed from the system before making or breaking any connections.

Power Supply OFF—The power supply should always be off before it is connected to the I/O Module. Do not hot-plug the PPM-C407 on a host platform that is already powered.

I/O Connections OFF—I/O Connections should also be off before connecting them to the embedded computer modules or any I/O cards. Connecting hot signals can cause damage whether the embedded system is powered or not.

Mounting and Protecting the I/O Module

The PPM-C407 must be mounted properly to avoid damage. Standoff kits are available and recommended for use with the PPM-C407.

- KIT-PCM-STANDOFF-4: Four piece Nylon Hex PC/104 Standoff Kit
- KIT-PCM-STANDOFF-B-4: Four piece Brass Hex PC/104 Standoff Kit

The following table lists the items contained in each kit:

Kit	Component	Description	Qty
KIT-PCM-STANDOFF-4 4 pc. Nylon Hex PC/104 Standoff Kit	Standoff	Nylon 0.25” Hex, 0.600" Long Male/Female 4-40	4
	Hex Nut	Hex Nylon 4-40	4
	Screw	Phillips-Pan Head (PPH) 4-40 x 1/4" Stainless Steel	4
KIT-PCM-STANDOFF-B-4 4 pc.Brass Hex PC/104 Standoff Kit	Standoff	Brass 5 mm Hex, 0.600" Long Male/Female 4-40	4
	Hex Nut	4-40 x 0.095 Thick, Nickel Finish	4
	Screw	Phillips-Pan Head (PPH) 4-40 x 1/4" Stainless Steel	4

Placing the PPM-C407 on Mounting Standoffs—Be careful when placing the PPM-C407 on the mounting standoffs. Sliding the board around until the standoffs are visible from the top can cause component damage on the bottom of the board.

Do Not Bend or Flex the PPM-C407—Bending or flexing can cause irreparable damage. Embedded computer modules are especially sensitive to flexing or bending around Ball Grid Array (BGA) devices. BGA devices are extremely rigid by design and flexing or bending the embedded computer module can cause the BGA to tear away from the printed circuit board.

Mounting Holes—The mounting holes are plated on the top, bottom and through the barrel of the hole and are connected to the embedded computer module’s ground plane. Traces are often routed in the inner layers right below, above or around the mounting holes.

- Never use a drill or any other tool in an attempt to make the holes larger.
- Never use screws with oversized heads. The head could come in contact with nearby components causing a short or physical damage.
- Never use self-tapping screws; they will compromise the walls of the mounting hole.
- Never use oversized screws that cut into the walls of the mounting holes.
- Always use all of the mounting holes. By using all of the mounting holes you will provide the support the embedded computer module needs to prevent bending or flexing.

Plug or Unplug Connectors Only on Fully Mounted Boards—Never plug or unplug connectors on a board that is not fully mounted. Many of the connectors fit rather tightly and the force needed to plug or unplug them could cause the embedded computer module to be flexed.

Avoid Cutting the PPM-C407—Never use star washers or any fastening hardware that will cut into the PPM-C407.

Avoid Over-tightening of Mounting Hardware—Causing the area around the mounting holes to compress could damage interlayer traces around the mounting holes.

Use Appropriate Tools—Always use tools that are appropriate for working with small hardware. Large tools can damage components around the mounting holes.

Avoid Conductive Surfaces—Never allow the embedded computer module to be placed on a conductive surface. Many embedded systems use a battery to back up the clock-calendar and CMOS memory. A conductive surface such as a metal bench can short the battery causing premature failure.

Adding PC/104 Boards to your Stack

Be careful when adding PC/104 boards to your stack—Never allow the power to be turned on when a PC/104 board has been improperly plugged onto the stack. It is possible to misalign the PC/104 card and leave a row of pins on the end or down the long side hanging out of the connector. If power is applied with these pins misaligned, it will cause the I/O board to be damaged beyond repair.

Conformal Coating

Conformal coating by any source other than WINSYSTEMS voids the product warranty and will not be accepted for repair by WINSYSTEMS. If such a product is sent to WINSYSTEMS for repair, it will be returned at customer expense and no service will be performed. A WINSYSTEMS product conformally coated by WINSYSTEMS will be subject to regular WINSYSTEMS warranty terms and conditions.

Operations/Product Manuals

Every single board computer has an Operations manual or Product manual.

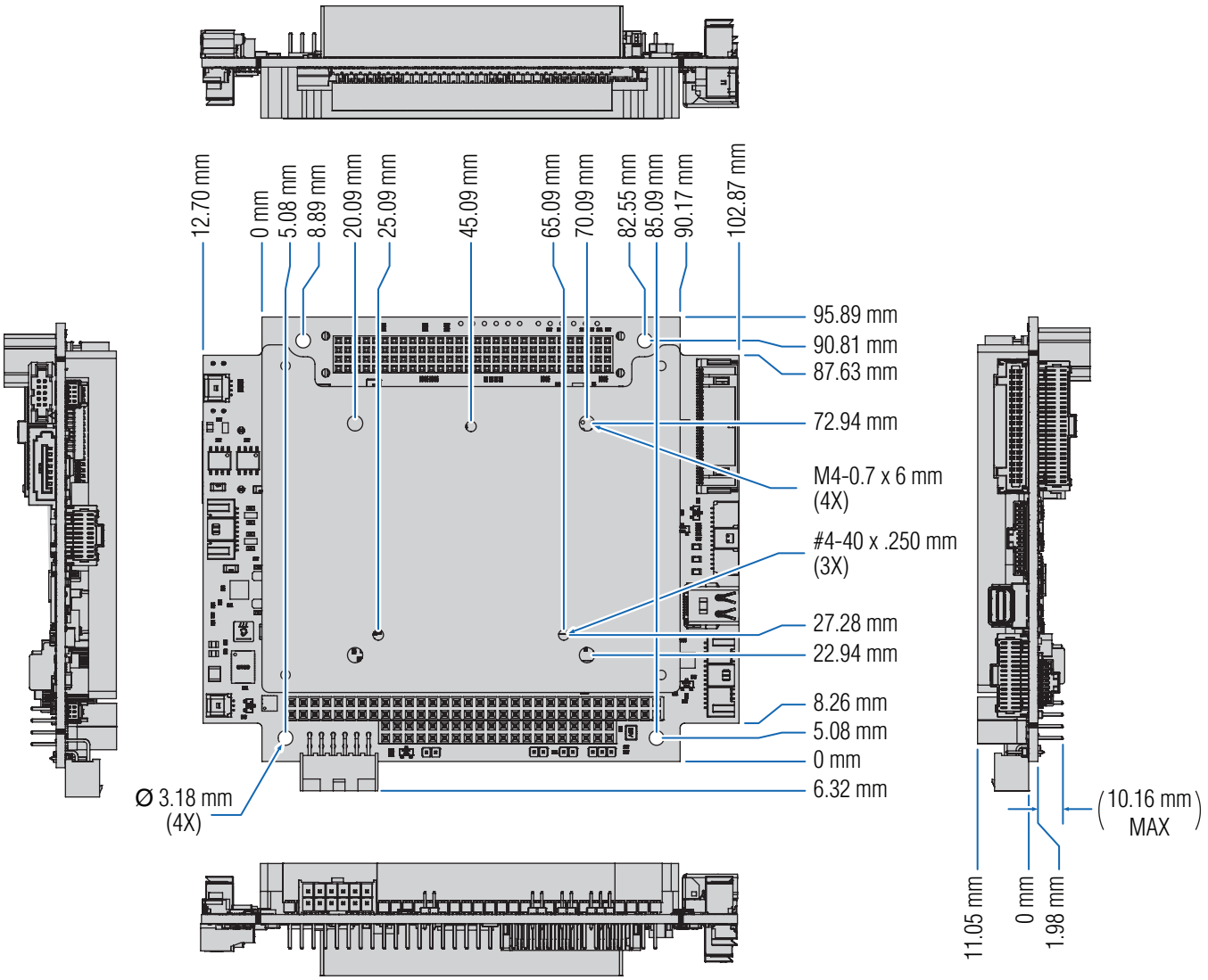
Periodic Updates—Operations/Product manuals are updated often. Periodically check the WinSystems website (https://www.winsystems.com) for revisions.

Check Pinouts—Always check the pinout and connector locations in the manual before plugging in a cable. Many I/O modules will have identical headers for different functions and plugging a cable into the wrong header can have disastrous results.

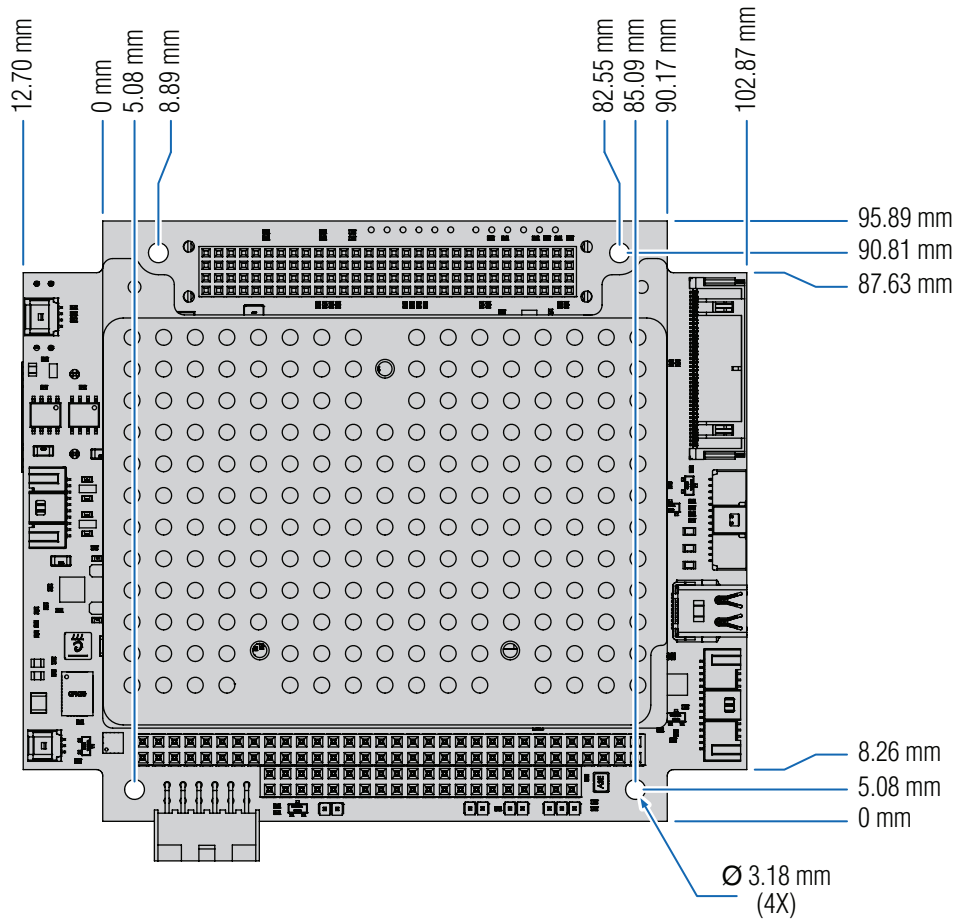
Contact an Applications Engineer—If a diagram or chart in a manual does not seem to match your board, or if you have additional questions, contact a WinSystems Applications Engineer at: +1-817-274-7553.

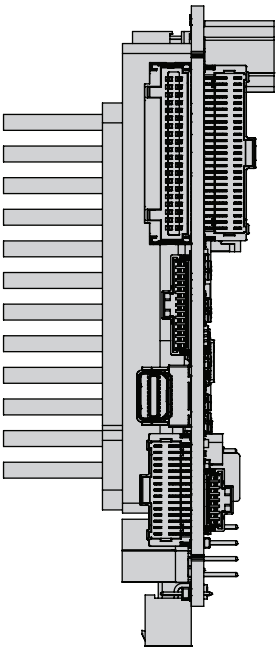
Appendix B. Mechanical Drawings

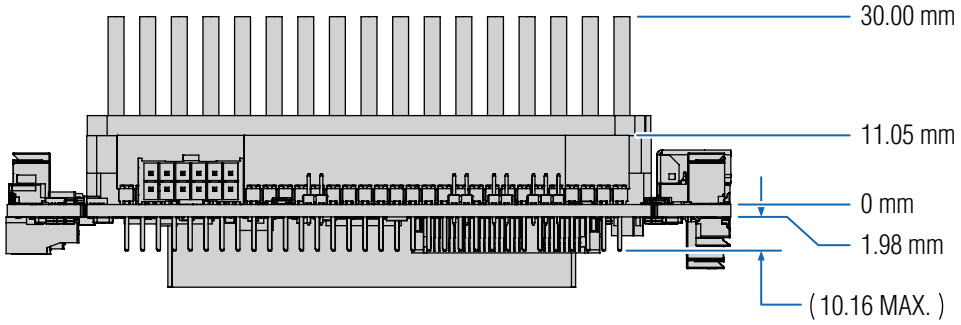
PC/104-Plus SBC E38*XX* without heatsink



PC/104-Plus SBC E38XX with heatsink







Appendix C. Power-on Self-Test (POST) Codes

If the system hangs before the BIOS can process the error, the value displayed at the I/O port address 80h is the code of the last successful operation. In this case, the screen does not display an error code.

Basic POST Codes

The following is a list of the checkpoint codes written at the start of each test and their corresponding audio beep codes issued for terminal errors.

Table C–1: Basic Post Codes

Code	Symbol	Description
20	ACPI_SMI	SCT ACPI SMI Services DXE driver
21	ACPI_SUPPORT	ACPI table manipulating driver
22	ACPI_TABLE	Generic ACPI table support, Simple Boot Flag, various ACPI table producers
23	ACPI_TABLEHOLDER	ACPI table loader initialization and protocols
24	AHCI_ASPI	AHCI ASPI Legacy SMM driver
25	AHCI_BUS	AHCI UEFI driver
26	AHCI_PASS_THRU	Driver sending ATA commands to AHCI controller
27	BLOCK_IO_THUNK	EFI glue for BIOS INT13h HDD services
28	BOOT_MANAGER	UEFI Boot Manager
29	BOOT_MENU	UEFI Boot Menu
2A	BOOT_MODE	Boot mode selection in PEI phase
2B	BOOT_NON_PARTITION	User forced boot from non-primary partition
2C	BOOT_SCRIPT	Boot script save
2D	BOOT_TIME	Boot time measurement support
2E	BOOT_TYPE	PEI boot type support (cold, warm, power on, S3…)
2F	CAPSULE_SERVICES	Capsule update and capsule runtime support
30	CARDBUS	Cardbus support
31	CONSOLE_SPLITTER	Console input/output support, text device console support
32	CRISIS_RECOVERY	Locate a crisis recovery firmware volume
33	CRYPTO	Cryptographic driver in SMM
34	CSM_SMM	USB Legacy, APM, INT1A and SD card support in SMM
35	DATA_HUB	Creating and manipulating data hub
36	DEVICE_PATH	DevicePath support
37	DIAGNOSTIC	Diagnostic and summary splash screen
38	DISK_IO	Disk IO driver. Converts a block oriented device to a byte oriented device
39	DXE_IPL	Load DXE core from DXE firmware volume

Table C–1: Basic Post Codes (Continued)

Code	Symbol	Description
3A	EBC	EBC interpret
3B	EMBEDDED_CONTROLLER	Embedded/Keyboard Controller driver
3C	ERROR_LOG	Error Manager, Error Log, SERR support
3D	FILESYSTEM	Enhanced FAT filesystem
3E	FIRMWARE_DEVICE	Generic firmware device (flash part) driver
3F	FIRMWARE_VOLUME	Firmware volume related drivers (fault tolerant update, simple file system)
40	FIRSTWARE	(unused)
41	FLASH_COMMUNICATION	Phoenix Flash Interface (allocate, initialize, runtime)
42	FLOPPY	ISA Floppy Driver
43	FONT	Installing HII font packages
44	GRAPHICS_CONSOLE	Text output via GOP driver
45	HDD_PASSWORD	HDD password and Software Setting Preservation
46	HII_DATABASE	UEFI HII support
47	HII_FORMS_BROWSER	UEFI HII From Browser (BIOS Setup)
48	HII_FORMS_BROWSER_LAYOUT	UEFI HII From Browser Layout (BIOS Setup)
49	HII_FORMS_BROWSER_VIEW	UEFI HII From Browser screen interface (BIOS Setup)
4A	ICRYPTSVC	Cryptographic driver in SMM, iCrypt support
4B	IDE_BUS	IDE bus support driver
4C	IDE_CONTROLLER	Generic IDE controller support driver
4D	IDE_PASS_THRU	Interface to send ATA commands to devices
4E	IMAGE	Image decoder (BMP, GIF, JPEG support)
4F	INTERRUPT_CONTROLLER	8259 Interrupt Controller
50	IPMI	IPMI support
51	ISA_BUS	ISA bus support (driver binding)
52	KEY_TRANSLATION	Virtual and onscreen keyboard, touch support
53	KEYBOARD_CONTROLLER	Standard ISA keyboard controller driver
54	KEYBOARD_THUNK	(unused)
55	LEGACY_BIOS	Legacy BIOS support, legacy tables
56	LOCK_SMRAM	System Management RAM locking
57	MEMORY_TEST	RAM test
58	METRONOME	Legacy metronome (periodic timer ticks)
59	MONOTONIC_COUNTER	Monotonic counter
5A	NETWORK	Network stack (SNP, DPC, MNP, ARP, TCP/IP, DHCP, FTP ...)
5B	OEM_ACTIVATION	OEM Activation, SLP support
5C	PARTITION	Partition support - MBR, GPT, El Torito
5D	PASSWORD	Password pop-up and reset
5E	PCI_BUS	PCI bus support drivers

Table C–1: Basic Post Codes (Continued)

Code	Symbol	Description
5F	PPI_NEEDED	(unused)
60	PROGRESS_INDICATOR	Progress bar support in Boot Manager
61	PS2_KEYBOARD	PS/2 keyboard driver
62	PS2_MOUSE	PS/2 mouse driver
63	RESET	Reset platform via port CF9h
64	RTC	Standard ISA RTC support
65	RUNTIME	Switch over to Runtime
66	S3_SSMI	S3 Boot Script support
67	S3_SUPPORT	ACPI S3 Save support
68	SCSI_BUS	SCSI bus driver
69	SCSI_DISK	SCSI disk driver
6A	SCSI_PASS_THRU	SCSI OpROM Pass Thru
6B	SECTION_EXTRACTION	Extracting section from a firmware file
6C	SECURE_BOOT	Secure Boot DXE driver
6D	SECURE_FLASH	Secure Flash support (capsule flash update)
6E	SECURE_KEY	Phoenix SecureKey SMM support
6F	SECURITY_SDM	SDM driver, providing access to secure data
70	SECURITY_STUB	Platform security stub driver
71	SERIAL	PCI/ISA serial port, serial mouse
72	SETUP	Setup pages
73	SMBIOS	SMBIOS tables initialization and update
74	SMBIOS_EVENT_LOG	SMBIOS Event Log
75	SMM_COMMUNICATION	Phoenix SMM Communication (DXE <-> SMM interface)
76	SMM_RUNTIME	SMM Ready To Boot, SMM Runtime Infrastructure
77	SMM_SERVICES	SMM driver register, dispatch and communicate
78	SPEAKER	Speaker support (beeps)
79	SPLASH	Logo splash screen
7A	SSMI_ALLOCATOR	Software SMI allocator
7B	STATUS_CODE	Status code drivers (PORT 80, Serial)
7C	TCG	TCG / TPM support
7D	TEXT_CONSOLE	UEFI VGA text console
7E	TIMER	UEFI Watchdog and 8254 timer
7F	TPM_NV	(unused)
80	UNICODE	Unicode character set support
81	USB_BUS	USB bus driver
82	USB_CONTROLLER	USB controller driver (UHCI, OHCI, EHCL XHCI)
83	USB_DEVICE	USB device drivers (keyboard, mouse, mass storage ...)
84	USB_PROTOCOL	USB protocol drivers

Table C–1: Basic Post Codes (Continued)

Code	Symbol	Description
85	USER_MANAGER	User manager driver (PBA, security)
86	VARIABLE_DEFAULT	(unused)
87	VARIABLE_SERVICES	Variable services
88	VGA	Simple Text and GOP on legacy VGA Option ROM
89	APEI	ACPI APEI support (aka WHEA)
8A	CSM_PREPARETOBOOT_ENTRY	CSM "Prepare to boot" called
8B	CSM_PREPARETOBOOT_EXIT	CSM "Prepare to boot" exited
8C	CSM_INT19_ENTRY	(unused)
8D	CSM_BOOTDEVICE_ENTRY	(unused)
8E	CSM_BOOTDEVICE_EXIT	(unused)
8F	CSM_INT19_EXIT	(unused)
90	FLASH_DEVICE	Flash device driver (flash part)
91	FLASH_CONTROLLER	Flash controller driver (chipset / EC)
92	SIO_PEI	Super I/O PEI module
93	SIO_DXE	Super I/0 DXE driver
94	HARDWARE_MONITOR	Hardware monitor driver
A0	PLATFORM_STAGE0	Platform Stage0 module (early PEI platform init)
A1	PLATFORM_STAGE1	Platform Stage1 module (PEI platform init)
A2	PLATFORM_STAGE2	Platform Stage2 module (late PEI platform init)
A3	PLATFORM_DXE	Platform DXE driver
A4	PLATFORM_S3SAVE	Platform S3 save DXE and SMM drivers
A5	PLATFORM_FLASH	Platform flash driver
A6	PLATFORM_SMM	Platform SMM initialization driver
A7	PLATFORM_PCI	Platform PCI bus driver
A8	PLATFORM_CSM	Platform specific legacy BIOS protocol
A9	PLATFORM_ADVHII	Platform Advanced HII (setup page)
AA	PLATFORM_SETUP	Setup entry and default configuration

Architectural Diagnostic Codes

Architectural Diagnostic diagnostic codes describe important events in the BIOS initialization sequence.

Table C–2: Architectural Diagnostic Codes

Code	Symbol	Description
F0	SEC_ENTRY	SEC phase entry (reset vector)
F1	SEC_EXIT	SEC phase exit
F2	PEI_ENTRY	PEI phase entry (PEI dispatch)
F3	PEI_EXIT	PEI phase exit
F4	IPL_DXE	DXE IPL normal boot path
F5	IPL_S3	DXE IPL S3 boot path to OS
F6	S3_OS	S3 boot to OS
F7	IPL_RECOVERY	DXE IPL crisis recovery boot path
F8	IPL_EXIT	Exiting DXE IPL, starting DXE phase
F9	DXE_ENTRY	DXE dispatch start
FA	DXE_EXIT	DXE dispatch exit
FB	PEI_MEMORY	No permanent memory found in PEI phase
FC	PEI_IPL	No DXE IPL found in PEI phase
FD	IPL_DXE	No DXE found in IPL
FE	IPL_PPI	Missing PPIs needed by DXE
FF	DXE_ARCH	Missing architectural protocols at the end of DXE

Progress and Error Codes

Progress and error codes are only displayed on POST diagnostic displays that show four digits. On these displays, the most significant two digits show the progress or error code from the table in this section (Progress and Error Codes), while the least significant two digits show the diagnostic code (see tables above). For example: 0345 indicates the component was loaded, the DXE/UEFI entry point called, and DXE driver initialization of the HDD password feature.

Table C–3: Progress and Error Codes

Code	Symbol	Description
01	COMP_PEI_BEGIN	The component was loaded and the PEI entry point called
02	COMP_PEI_END	The component returned from the entry point
03	COMP_DXE_BEGIN	The component was loaded and the DXE/UEFI entry point called
04	COMP_DXE_END	The component returned from the entry point
05	COMP_SUPPORTED	The Supported() member function of the component's instance of the Driver Binding protocol was called
06	COMP_START	The Start() member function of the component's instance of the Driver Binding protocol was called
07	COMP_STOP	The Stop() member function of the component's instance of the Driver Binding protocol was called
08	COMP_SMM_INIT	The component was loaded and the entry point called inside of SMM
09	DEVICE_ERROR	The driver encountered a condition where it cannot proceed due to a hardware failure
0A	RESOURCE_ERROR	The driver encountered a condition where it cannot proceed due to being unable to acquire resources
0B	DATA_CORRUPT	The driver encountered a condition where it found invalid data and could not continue
0C	COMP_PEI_CALLBACK	The component received a callback in PEI phase
0D	COMP_DXE_CALLBACK	The component received a callback in DXE phase

Appendix D. Warranty Information

Full warranty information can be found at https://winsystems.com/company-policies/warranty/.