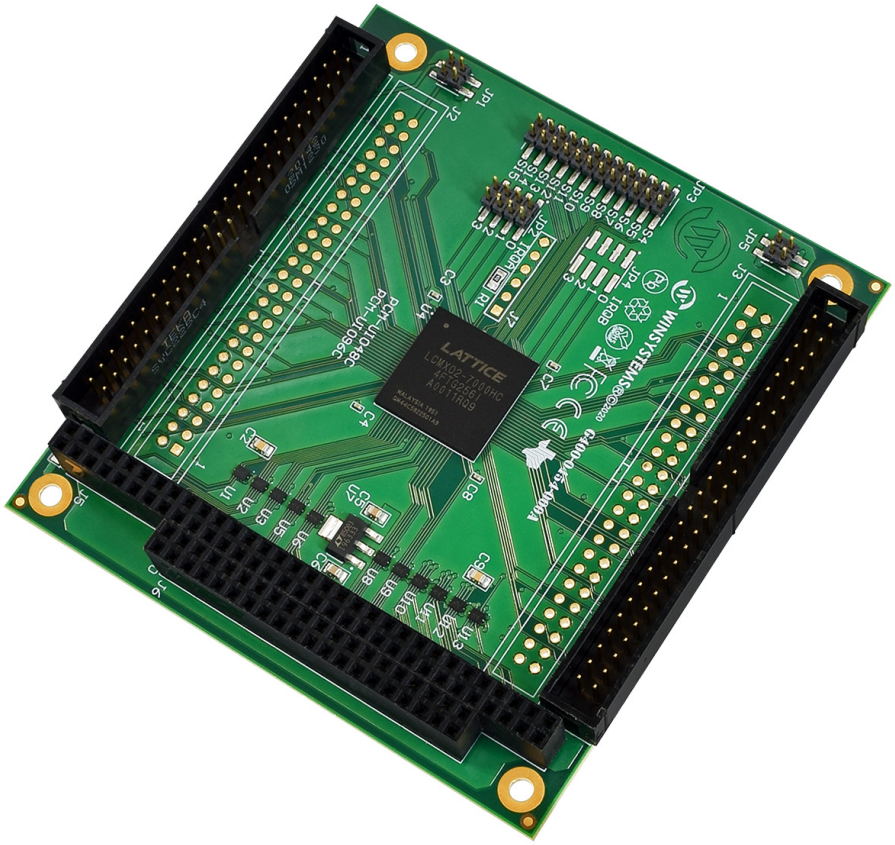
WINSYSTEMS®

PCM-UIO48C-16

Universal 48-Channel Digital I/O with Interruptible Event Sense

Product Manual



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Revision History

Document Version	Last Updated Date	Brief Description of Change
v1.0	9/16/20	Initial release
v1.1	7/29/2025	Updated Conformal Coating, added Warranty link, updated all links

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Trademark Acknowledgments

Table of Contents

1. Before You Begin

Review the warnings in this section and the best practice recommendations (see “Best Practices” on page 18) when using and handling the WINSYSTEMS PCM-UIO48C-16. Following these recommendations provides an optimal user experience and prevents damage. Read through this document and become familiar with the PCM-UIO48C-16 before proceeding.

APPLYING CONFORMAL COATING AFTER PURCHASE WILL VOID YOUR WARRANTY. FAILING TO COMPLY WITH THESE BEST PRACTICES MAY DAMAGE THE PRODUCT AND VOID YOUR WARRANTY.

1.1 Warnings

Only qualified personnel should configure and install the PCM-UIO48C-16. While observing best practices, pay particular attention to the following.

Avoid Electrostatic Discharge (ESD)
Only handle the circuit board and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

2. Introduction

This manual provides configuration and usage information for the PCM-UIO48C-16. If you still have questions, contact Technical Support at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Time (CT).

Refer to the WINSYSTEMS website at http://www.winsystems.com/ for other accessories (including cable drawings and pinouts) that can be used with your PCM-UIO48C-16.

3. Functionality

The PCM-UIO48C-16 is a highly versatile PC/104 input/output module providing 48 channels of digital I/O. The major feature of this card is its ability to monitor 24 channels for both rising and falling digital edge transitions, latch them, and then interrupt the host processor notifying that a change-of-input status has occurred. This is an efficient way of signaling the CPU of real-time events without the burden of polling the digital I/O channels.

3.1 Parallel I/O Controller

WINSYSTEMS has developed the WS16C48 universal I/O controller functionality to support the various input/output and interrupt configurations. The WS16C48 supports 48 digital I/O channels addressed through six contiguous registers.

A six-bit Write Mask register allows the user to disable writes on a byte basis to configure the group as a “read only” port.

Each I/O channel is individually programmable for input, output, or output with read back operation. The input channels are connected so the current status of its output port can be read from the corresponding input port (read back). If the port is used as input only, then the corresponding output port bit must be cleared.

Each output channel is latched and has an open collector driver (with a pull-up resistor) capable of sinking 12 mA of current. This allows direct control of up to 48 opto-isolated signal conditioning modules to a single card for high-density I/O support.

3.2 Event Sense Operation

The WS16C48 supports 24 event sense channels to generate an interrupt when an event occurs. This means that 24 channels of the PCM-UIO48C-16 can sense a positive or negative transition on the input. Transition polarity is programmable and enabled on a bit-by-bit basis. Each channel’s transition is latched by the event so that even short duration pulses is recognized.

The PCM-UIO48C-16 can generate a system interrupt request which can be routed via jumper to the IRQ channels on the PC/104 bus. An interrupt ID register is maintained for each channel for writing more efficient Interrupt Service Routines.

Sample drivers are downloadable for Linux, Windows XP, and C from the WINSYSTEMS’ website.

3.3 PC/104 Interface

The PCM-UIO48C-16 is a PC/104 compatible stackthrough card, which is I/O port mapped on any even 16-byte boundary.

3.4 I/O Connectors

The signals from the WS16C48 controller are wired to two 50-pin connectors, **J1** and **J4**. Each connector supports 24 data channels which are alternated with 24 ground lines for reduced noise and crosstalk.

The PCM-UIO48C-16's pinout is compatible with the industry-standard 4 to 24 position I/O module mounting racks (Opto-22, Crydom, Gordos, etc.). The racks accept AC and DC modules which optically isolate the computer from electrical transients and excessive voltages from the field devices.

4. Features

The PCM-UIO48C-16 provides the following features.

Digital I/O

- 48 bidirectional channels with input, output, or output with readback (FPGA with WS16C48 compatible programmed logic)
- 12 mA sink current

Event Sense

- 24 channels support event sense
- Programmable polarity for each channel
- Software-enabled interrupt for each channel
- Change-of-state latched for each channel

Power

- +5 V ±5% at 12 mA (excluding rack power with no loads on the outputs)

Industrial Operating Temperature Range

- -40°C to 85°C

Form Factor

- PC/104-compliant
- 3.60 in. x 3.80 in. (90 mm x 96 mm)

Additional Specifications

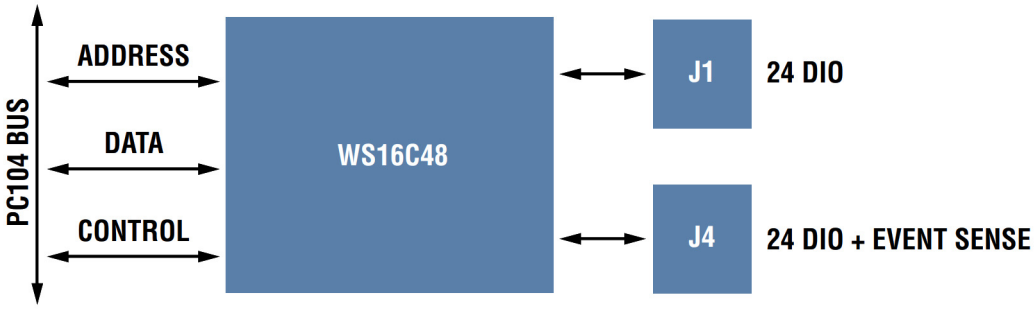
- Compatible with industry-standard I/O racks
- Write-protection mask register for each port
- Fused +5 V logic supply for I/O modules
- 8-bit, 16-bit PC/104 interface

5. General Operation

5.1 System Block Diagram

The PCM-UIO48C-16 uses a Lattice MachXO2 FPGA to communicate between the PC/104 ISA bus and the 48 DIO.

NOTE The PCM-UIO48C-16 uses only **J1** and **J4** connectors.



6. Specifications

The PCM-UIO48C-16 adheres to the following specifications and requirements.

Feature	Specification
Electrical	
V_{CC}	+5 V ±5% @12 mA typical with no I/O connections
Models	PCM-UIO48C-16
Maximum Power Usage	+5 V @ 12 mA required
Bus Interface	PC/104 16-bit
I/O Addressing	16-bit user jumperable base address Each board uses 32 consecutive I/O addresses
Mechanical	
Dimensions	3.55 in. x 3.775 in. (90 mm x 96 mm)
Weight	2.33 oz. (66 gm)
PCB Thickness	0.078 in. (1.98 mm)
Jumpers	0.025 in. square posts on 0.10 in. centers
Connectors	50-pin 0.10 in. grid RN type IDH-50-LP

Feature	Specification
Environmental	
Temperature	-40 to +85°C (-40 to +185°F)
Humidity (RH)	5% to 95% noncondensing
Mean time between failure (MTBF) [a]	MTBF (hours) 1330247.16 MTBF (years) 151.854 Prediction Model: MIL-HDBK-217F
RoHS Compliant	Yes
Operating Systems	
Compatible with Windows and Linux	

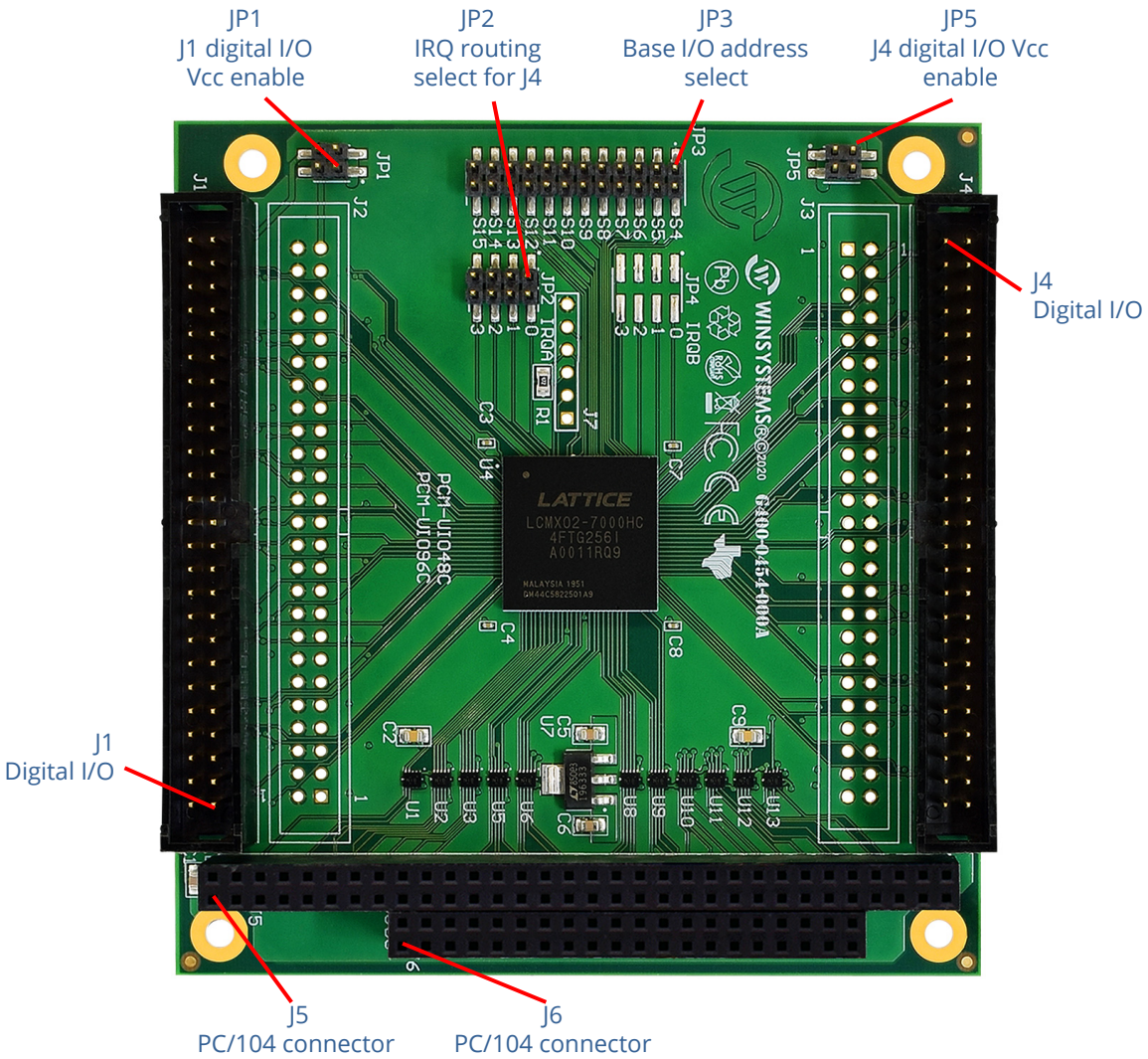
a. A MTBF measurement is based on a statistical sample and is not intended to predict any one specific unit's reliability; thus MTBF is not, and should not be construed as, a warranty measurement.

7. Configuration

This section describes the PCM-UIO48C-16 components and configuration.

7.1 Component Layout

7.1.1 Top View



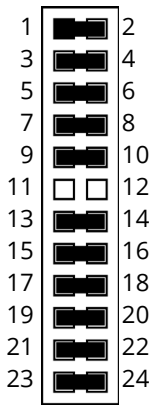
Item	Description	Reference
J1, J4	Digital I/O Headers	page 13
JP1, JP5	J1, J4 Digital I/O Vcc Enable	page 13
JP3	Base I/O Address Select	page 11
JP2	Interrupt Routing Select	page 11
J5, J6	PC/104 Bus Interface	page 14

7.2 Jumpers

7.2.1 JP3 - Base I/O Address Select

The PCM-UIO48C-16 is I/O mapped and requires 32 sequential port addresses. The base address is jumper selectable at **JP3**. Take care to choose an I/O area that does not conflict with other resources in the system. Address bits S0 to S3 are not selectable. **J7** begins at address bit S4.

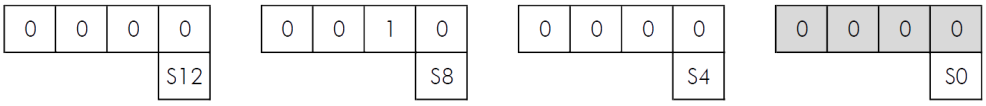
Layout and Pin Reference

Diagram	Pin	Name
	1–2	S4
	3–4	S5
	5–6	S6
	7–8	S7
	9–10	S8
	11–12	S9
	13–14	S10
	15–16	S11
	17–18	S12
	19–20	S13
	21–22	S14
	23–24	S15

Example

200HEX Default

- Jumper OPEN = 1
- Jumper INSTALLED = 0



7.2.2 JP2 - Interrupt Routing Select for J4

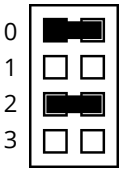
The PCM-UIO48C-16 can generate an interrupt on up to 24 different channels each with its own polarity select. Interrupt support is provided on the first 24 bits at ports 0, 1, and 2 (connector **J4**). This interrupt can be routed to the PC/104 bus via the jumper at **JP2**.

The interrupt select jumper **JP2** uses a 4-bit binary system. See below for an example of how to set IRQ 10.

Example

IRQ 10

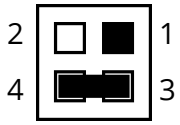
- Jumper OPEN = 1
- Jumper INSTALLED = 0

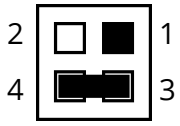


7.2.3 JP1, JP5 Digital I/O Vcc Enable

The digital I/O connector can provide +5 V to an I/O rail, when required. +5 V is provided at pin 49 on connector **J1** when **JP1** is jumpered. +5 V is provided at pin 49 on connector **J4** when **JP5** is jumpered. See below for jumper pinouts for **JP1** and **JP5**.

Layout and Pin Reference

JP1	Pin	Name
	3–4	J1 Vcc Enable

JP5	Pin	Name
	3–4	J4 Vcc Enable

7.3 Connectors

7.3.1 J1, J4 - Digital I/O Headers

The PCM-UIO48C-16 routes its 48 channels to 50-pin IDC connectors at **J1** and **J4**. The following table shows the pin definitions.

Layout and Pin Reference

Diagram	Pin	Name	Pin	Name
J4 1 o o 2 3 o o 4 5 o o 6 7 o o 8 9 o o 10 11 o o 12 13 o o 14 15 o o 16 17 o o 18 19 o o 20 21 o o 22 23 o o 24 25 o o 26 27 o o 28 29 o o 30 31 o o 32 33 o o 34 35 o o 36 37 o o 38 39 o o 40 41 o o 42 43 o o 44 45 o o 46 47 o o 48 49 o o 50	50	GND	49	VCC
	48	GND	47	Port 0 Bit 0
	46	GND	45	Port 0 Bit 1
	44	GND	43	Port 0 Bit 2
	42	GND	41	Port 0 Bit 3
	40	GND	39	Port 0 Bit 4
	38	GND	37	Port 0 Bit 5
	36	GND	35	Port 0 Bit 6
	34	GND	33	Port 0 Bit 7
	32	GND	31	Port 1 Bit 0
	30	GND	29	Port 1 Bit 1
	28	GND	27	Port 1 Bit 2
	26	GND	25	Port 1 Bit 3
	24	GND	23	Port 1 Bit 4
	22	GND	21	Port 1 Bit 5
	20	GND	19	Port 1 Bit 6
	18	GND	17	Port 1 Bit 7
	16	GND	15	Port 2 Bit 0
	14	GND	13	Port 2 Bit 1
	12	GND	11	Port 2 Bit 2
	10	GND	9	Port 2 Bit 3
	8	GND	7	Port 2 Bit 4
	6	GND	5	Port 2 Bit 5
	4	GND	3	Port 2 Bit 6
	2	GND	1	Port 2 Bit 7

Diagram	Pin	Name	Pin	Name
J1 1 o o 2 3 o o 4 5 o o 6 7 o o 8 9 o o 10 11 o o 12 13 o o 14 15 o o 16 17 o o 18 19 o o 20 21 o o 22 23 o o 24 25 o o 26 27 o o 28 29 o o 30 31 o o 32 33 o o 34 35 o o 36 37 o o 38 39 o o 40 41 o o 42 43 o o 44 45 o o 46 47 o o 48 49 o o 50	50	GND	49	VCC
	48	GND	47	Port 3 Bit 0
	46	GND	45	Port 3 Bit 1
	44	GND	43	Port 3 Bit 2
	42	GND	41	Port 3 Bit 3
	40	GND	39	Port 3 Bit 4
	38	GND	37	Port 3 Bit 5
	36	GND	35	Port 3 Bit 6
	34	GND	33	Port 3 Bit 7
	32	GND	31	Port 4 Bit 0
	30	GND	29	Port 4 Bit 1
	28	GND	27	Port 4 Bit 2
	26	GND	25	Port 4 Bit 3
	24	GND	23	Port 4 Bit 4
	22	GND	21	Port 4 Bit 5
	20	GND	19	Port 4 Bit 6
	18	GND	17	Port 4 Bit 7
	16	GND	15	Port 5 Bit 0
	14	GND	13	Port 5 Bit 1
	12	GND	11	Port 5 Bit 2
	10	GND	9	Port 5 Bit 3
	8	GND	7	Port 5 Bit 4
	6	GND	5	Port 5 Bit 5
	4	GND	3	Port 5 Bit 6
	2	GND	1	Port 5 Bit 7

NOTE Pin 49 on each connector can supply +5 V to the I/O rail.

7.3.2 J5, J6- PC/104 Bus Interface

The PCM-UIO48C-16 connects to the processor through the PC/104 bus connector at **J5**/**J6**. Refer to the PC/104 Bus Specification for specific signal and mechanical specifications.

For reference, the following figure shows the pin definitions for **J5**. and **J6**.

Layout and Pin Reference

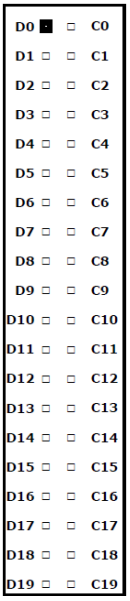
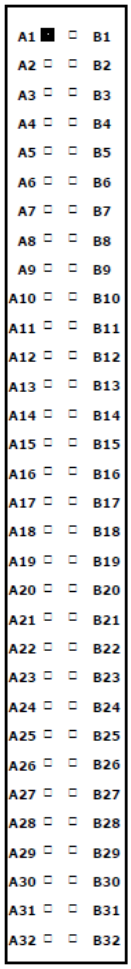
Diagram	Pin	Name	Pin	Name
J6 	D0	GND	C0	GND
	D1	MEMCS16#	C1	SBHE#
	D2	IOCS16#	C2	LA23
	D3	IRQ10	C3	LA22
	D4	IRQ11	C4	LA21
	D5	IRQ12	C5	LA20
	D6	IRQ15	C6	LA19
	D7	IRQ14	C7	LA18
	D8	DACK0#	C8	LA17
	D9	DRQ0	C9	MEMR#
	D10	DACK5#	C10	MEMW#
	D11	DRQ5	C11	SD8
	D12	DACK6#	C12	SB9
	D13	DRQ6	C13	SB10
	D14	DACK7#	C14	SB11
	D15	DRQ7	C15	SB12
	D16	+5V	C16	SB13
	D17	MASTER#	C17	SB14
	D18	GND	C18	SB15
	D19	GND	C19	KEY

Diagram	Pin	Name	Pin	Name
J5 	A1	IOCHK#	B1	GND
	A2	SD7	B2	RESET
	A3	SD6	B3	+5V
	A4	SD5	B4	IRQ9
	A5	SD4	B5	-5V
	A6	SD3	B6	DRQ2
	A7	SD2	B7	-12V
	A8	SD1	B8	SRDY#
	A9	SD0	B9	+12V
	A10	IOCHRDY	B10	KEY
	A11	AEN	B11	SMEMW#
	A12	SA19	B12	SMEMR#
	A13	SA18	B13	IOW#
	A14	SA17	B14	IOR#
	A15	SA16	B15	DACK3#
	A16	SA15	B16	DRQ3
	A17	SA14	B17	DACK1#
	A18	SA13	B18	DRQ1
	A19	SA12	B19	REFRESH#
	A20	SA11	B20	BCLK
	A21	SA10	B21	IRQ7
	A22	SA9	B22	IRQ6
	A23	SA8	B23	IRQ5
	A24	SA7	B24	IRQ4
	A25	SA6	B25	IRQ3
	A26	SA5	B26	DACK2#
	A27	SA4	B27	TC
	A28	SA3	B28	BALE
	A29	SA2	B29	+5V
	A30	SA1	B30	OSC
	A31	SA0	B31	GND
	A32	GND	B32	GND

Notes:

- # indicates active low signal.
- B10 and C19 are key locations. WINSYSTEMS uses key pins as connections to GND.
- Signal timing and function are as specified in ISA specification.
- Signal source/sink current differ from ISA values.

7.4 Register Definitions

The PCM-UIO48C-16 uses a Lattice MachXO2 FPGA with WINSYSTEMS WS16C48 ASIC compatible programmed logic. This provides 48 channels of digital I/O. There are 17 unique registers within the WS16C48 logic. The following table summarizes the registers, and the text that follows provides details on each of the internal registers.

I/O Address Offset	Page 0	Page 1	Page 2	Page 3
00H	Port 0 I/O			
01H	Port 1 I/O			
02H	Port 2 I/O			
03H	Port 3 I/O			
04H	Port 4 I/O			
05H	Port 5 I/O			
06H	Int_Pending			
07H	Page/Lock			
08H	N/A	Pol_0	Enab_0	Int_ID0
09H	N/A	Pol_1	Enab_1	Int_ID1
0AH	N/A	Pol_2	Enab_2	Int_ID2

7.5 Register Details

7.5.1 Port 0 through 5 I/O

Each I/O bit in each of the six ports can be individually programmed for input or output. Writing a **0** to a bit position causes the corresponding output pin to go to a high-impedance state (pulled high by external 10 KΩ resistors). This allows it to be used as an input. When used in the input mode, a read reflects the inverted state of the I/O pin, such that a high on the pin reads as a 0 in the register. Writing a **1** to a bit position causes that output pin to sink current (up to 12 mA), effectively pulling it low.

NOTE Only ports 0 through 2 support interrupts.

7.5.2 Int_Pending

This read-only register reflects the combined state of the INT_ID0 through INT_ID2 registers. When any of the lower three bits are set, it indicates that an interrupt is pending on the I/O port corresponding to the bit positions that are set. Reading this register allows an interrupt service routine to quickly determine if any interrupts are pending and which I/O port has a pending interrupt.

7.5.3 Page/Lock

This register serves two purposes. The upper two bits select the register page in use as shown in the following table.

D7	D6	Page
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

Bits 5-0 allow for locking the I/O ports. Writing a **1** to the I/O port position prohibits further writes to the corresponding I/O port.

7.5.4 Pol_0 - Pol_2

These registers are accessible when Page 1 is selected. They allow interrupt polarity selection on a port–by–port and bit-by-bit basis. Writing a **1** to a bit position selects the rising edge detection interrupts while writing a **0** to a bit position selects falling edge detection interrupts.

7.5.5 Enab_0 - Enab_2

These registers are accessible when Page 2 is selected. They allow for port-by- port and bit-by-bit enabling of the edge detection interrupts. When set to a **1** the edge detection interrupt is enabled for the corresponding port and bit. When cleared to **0**, the bit's edge detection interrupt is disabled. Note that this register can be used to individually clear a pending interrupt by disabling and re-enabling the pending interrupt.

7.5.6 Int_ID0 - Int_ID2

These registers are accessible when Page 3 is selected. They are used to identify currently pending edge interrupts. A bit when read as a **1** indicates that an edge of the polarity programmed into the corresponding polarity register has been recognized. Note that a write to this register (value ignored) clears ALL of the pending interrupts in this register.

8. Accessories

The following cables are available ONLY for model **PCM-UIO48C-16**.

Go to www.winsystems.com for more information on WINSYSTEMS cables and batteries.

Item	Part Number	Description
Termination board	ISM-TRM-RELAY	Industrial PC/104 relay board, 16 SPDT relays
Termination board	ISM-TRM-ISO-OUT	Termination board, 24 isolated outputs
Termination board	ISM-TRM-ISO-IN	Termination board - 24 isolated inputs
Termination board	ISM-TRM-COMBO	Termination board - 8 in, 8 out, and 8 relays

Standoff kits are available and recommended for use with the PCM-UIO48C-16. The following table lists the items contained in each kit.

Kit	Component	Description	Qty
KIT-G-PCM-STANDOFF-4 4 pc. nylon hex PC/104 standoff kit	Standoff	Nylon 0.25” hex, 0.600” long male/female 4-40	4
	Hex nut	Hex nylon 4-40	4
	Screw	Phillips-pan head (PPH) 4-40 x 1/4” stainless steel	4
KIT-PCM-STANDOFF-B-4 4 pc. brass hex PC/104 standoff kit	Standoff	Brass 5 mm hex, 0.600” long male/female 4-40	4
	Hex nut	4-40 x 0.095 thick, nickel finish	4
	Screw	Phillips-pan head (PPH) 4-40 x 1/4” stainless steel	4

9. Software Drivers

Go to www.winsystems.com for more information on available software drivers.

Appendix A. Best Practices

The following paragraphs outline the best practices for operating the PCM-UIO48C-16 in a safe, effective manner, that does not damage the board. Read this section carefully.

Power Supply

Avoid Electrostatic Discharge (ESD)
Only handle the circuit board and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

Power Supply Budget

Evaluate your power supply budget. It is usually good practice to budget twice the typical power requirement for all of your devices.

Zero-load Power Supply

Use a zero-load power supply whenever possible. A zero-load power supply does not require a minimum power load to regulate. If a zero-load power supply is not appropriate for your application, then verify that the embedded system's typical load is not lower than the power supply's minimum load. If the embedded system does not draw enough power to meet the power supply's minimum load, then the power supply does not regulate properly and can cause damage to the PCM-UIO48C-16.

Use Proper Power Connections (Voltage)
When verifying the voltage, measure it at the power connector of your embedded system. Measuring it at the power supply does not account for voltage drop through the wire and connectors.

The PCM-UIO48C-16 requires 5 V to operate. Verify the power connections. Incorrect voltages can cause catastrophic damage.

The PCM-UIO48C-16 accepts 5 V via the PC/104 connector.

Power Harness

Minimize the length of the power harness. This reduces the amount of voltage drop between the power supply and the embedded system.

Gauge Wire

Use the largest gauge wire that you can. Most connector manufacturers have a maximum gauge wire they recommend for their pins.

Contact Points

WINSYSTEMS boards mostly use connectors with gold finish contacts. Gold finish contacts are used exclusively on high-speed connections. Power and lower speed peripheral connectors may use a tin finish as an alternative contact surface. It is critical that the contact material in the mating connectors is matched properly (gold to gold and tin to tin). Contact areas made with dissimilar metals can cause oxidation/corrosion, resulting in unreliable connections.

Pin Contacts

Often the pin contacts used in cabling are not given enough attention. The ideal choice for a pin contact would include a design similar to Molex or Trifurcon designs, which provide three distinct points to maximize the contact area and improve connection integrity in high shock and vibration applications.

Power Down

Make sure that power has been removed from the system before making or breaking any connections.

Power Supply OFF—Always turn off the power supply before connecting to the I/O Module. Do not hot-plug the PCM-UIO48C-16 on a host platform that is already powered.

I/O Connections OFF—Turn off all I/O connections before connecting them to the PCM-UIO48C-16 or any other I/O cards. Connecting hot signals can cause damage whether the embedded system is powered or not.

Mounting and Protecting the I/O Module

To avoid damage, mount the PCM-UIO48C-16 properly. Standoff kits are available and recommended for use with the PCM-UIO48C-16.

Placing the PCM-UIO48C-16 on mounting standoffs—Be careful when placing the PCM-UIO48C-16 on the mounting standoffs. Sliding the board around until the standoffs are visible from the top can cause component damage on the bottom of the board.

Do not bend or flex the PCM-UIO48C-16—Bending or flexing can cause irreparable damage. Embedded computer modules are especially sensitive to flexing or bending around ball grid array (BGA) devices. BGA devices are extremely rigid by design, and flexing or bending the embedded computer module can cause the BGA to tear away from the printed circuit board.

Mounting holes—The mounting holes are plated on the top, bottom, and through the barrel of the hole. The mounting holes are connected to the embedded computer module's ground plane.

- Never use a drill or any other tool in an attempt to make the holes larger.
- Never use screws with oversized heads. The head could come in contact with nearby components causing a short or physical damage.
- Never use self-tapping screws; they compromise the walls of the mounting hole.
- Never use oversized screws that cut into the walls of the mounting holes.
- Always use all of the mounting holes. By using all of the mounting holes, you provide the support the embedded computer module needs to prevent bending or flexing.

Plug or unplug connectors only on fully mounted boards—Never plug or unplug connectors on a board that is not fully mounted. Many of the connectors fit rather tightly and the force needed to plug or unplug them could cause the embedded computer module to be flexed.

Avoid cutting the PCM-UIO48C-16—Never use star washers or any fastening hardware that cut into the PCM-UIO48C-16.

Avoid over-tightening of mounting hardware—Causing the area around the mounting holes to compress could damage interlayer traces around the mounting holes.

Use appropriate tools—Always use tools that are appropriate for working with small hardware. Large tools can damage components around the mounting holes.

Avoid conductive surfaces—Never allow the embedded computer module to be placed on a conductive surface. Many embedded systems use a battery to back up the clock-calendar and CMOS memory. A conductive surface such as a metal bench can short the battery causing premature failure.

Adding PC/104 to your Stack

Be careful when adding PC/104 boards to your stack—Never allow the power to be turned on when a PC/104 board has been improperly plugged onto the stack.

Conformal Coating

Conformal coating by any source other than WINSYSTEMS voids the product warranty and will not be accepted for repair by WINSYSTEMS. If such a product is sent to WINSYSTEMS for repair, it will be returned at

customer expense and no service will be performed. A WINSYSTEMS product conformally coated by WINSYSTEMS will be subject to regular WINSYSTEMS warranty terms and conditions.

Operations/Product Manuals

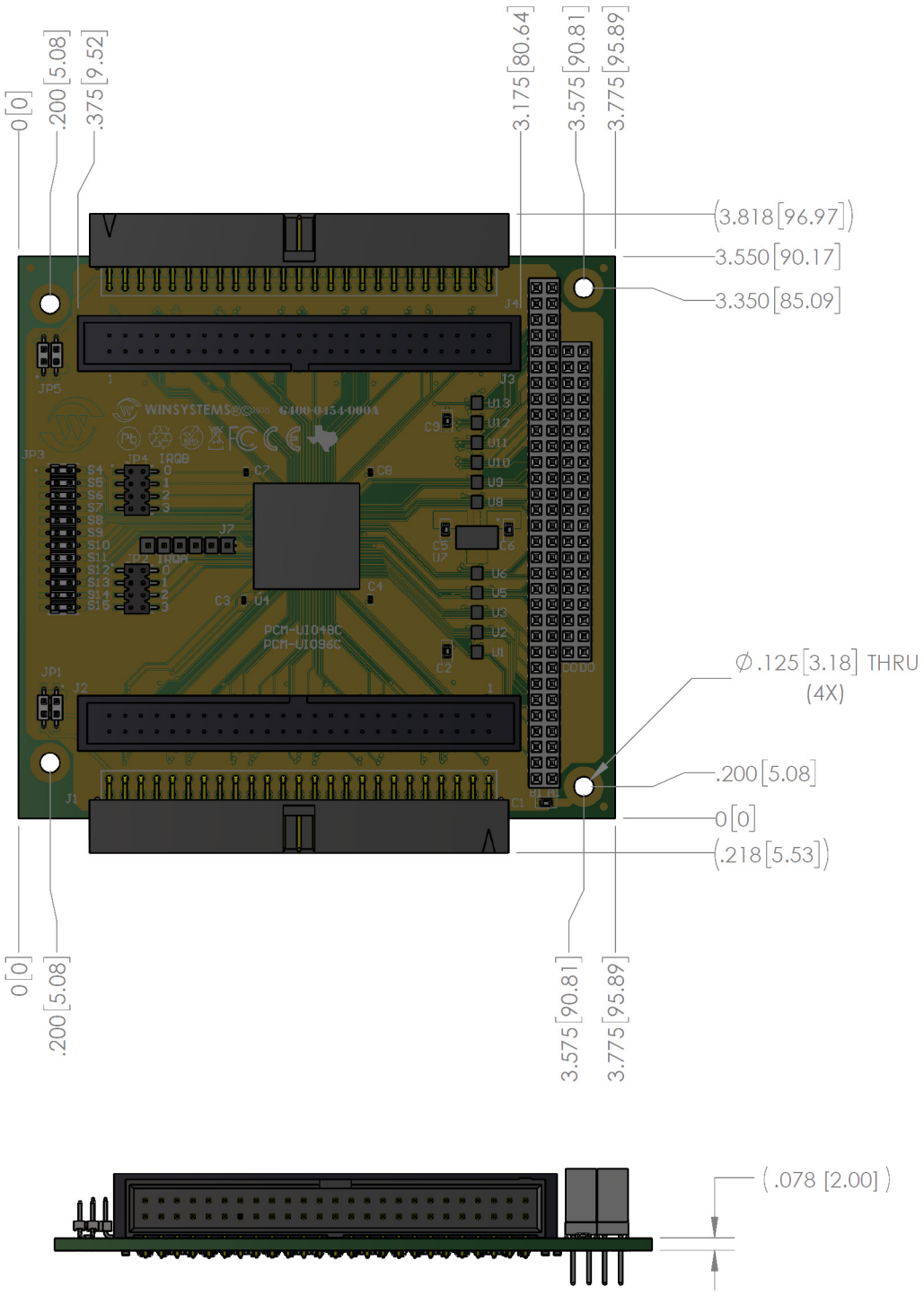
Every WINSYSTEMS product has an Operations manual or Product manual.

Periodic updates—Operations/product manuals are updated often. Periodically check the WINSYSTEMS website (https://www.winsystems.com) for revisions.

Check pinouts—Always check the pinout and connector locations in the manual before plugging in a cable. Many I/O modules have identical headers for different functions and plugging a cable into the wrong header can have disastrous results.

Contact an Applications Engineer—If a diagram or chart in a manual does not seem to match your system, or if you have additional questions, contact a WINSYSTEMS Applications Engineer at +1-817-274-7553.

Appendix B. Mechanical Drawings



Appendix C. Warranty Information

Full warranty information can be found at https://winsystems.com/company-policies/warranty/.