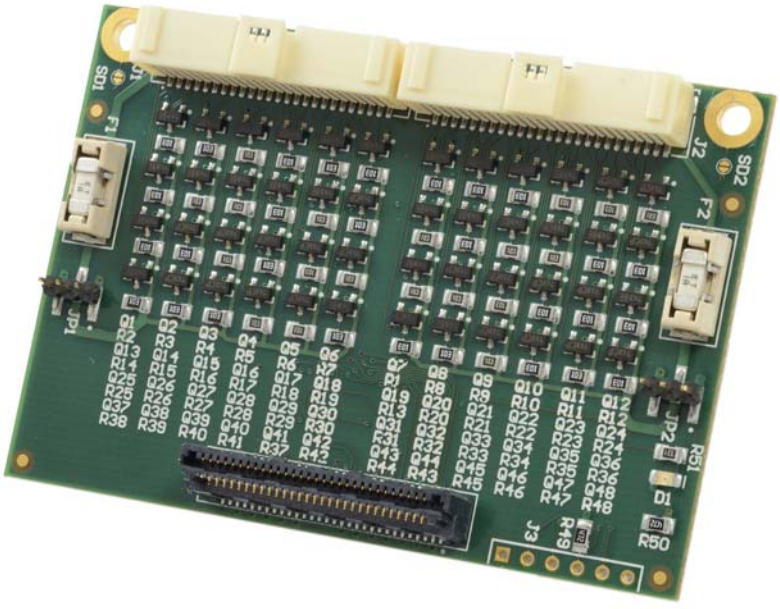
WINSYSTEMS®

IO60-DIO48

Digital Input Output Module

Product Manual



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Revision History

Document Version	Last Updated Date	Brief Description of Change
v1.0	02/2016	Initial release
v1.1	07/29/2025	Updated Conformal Coating, added Warranty link, updated all links

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Trademark Acknowledgments

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Table of Contents

1. Before You Begin

Review the warnings in this section and the best practice recommendations (see Best Practices) when using and handling the WinSystems IO60-DIO48. Following these recommendations provides an optimal user experience and prevents damage. Read through this document and become familiar with the IO60-DIO48 before proceeding.

APPLYING CONFORMAL COATING AFTER PURCHASE WILL VOID YOUR WARRANTY. FAILING TO COMPLY WITH THESE BEST PRACTICES MAY DAMAGE THE PRODUCT AND VOID YOUR WARRANTY.

1.1 Warnings

Only qualified personnel should configure and install the IO60-DIO48. While observing the best practices, pay particular attention to the following:

Avoid Electrostatic Discharge (ESD)
Only handle the circuit board and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

Before supplying voltage to pin 49 of J1 or J2, remove any jumper installed on JP1 (for J1) or JP2 (for J2), respectively. Damage to the board may occur if you apply a voltage to pin 49 of J1 while a jumper is installed on JP1. Damage to the board may occur if you apply a voltage to pin 49 of J2 while a jumper is installed on JP2.

2. Introduction

This manual provides configuration and usage information for the IO60-DIO48. If you still have questions, contact Technical Support at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

Refer to the WinSystems website for other accessories (including cable drawings and pinouts) that can be used with your IO60-DIO48.

3. Functionality

The IO60-DIO48 is a Digital Input Output Module featuring 48 GPIO (General Purpose Input-Output) lines tolerant to 30 VDC. Activity LEDs indicate device communication.

All functions are accessed though the host platform Serial Peripheral Interface (SPI) bus on the IO60 interface connector:

- The Programmable Logic Device (PLD) provides a total of 48 lines of General Purpose Input-Output (GPIO) accessible through two 50-pin Molex® Pico-Clasp™ connectors. On-board level conversion buffer circuits allow driving or receiving signal levels up to 30 VDC. The user must supply the I/O voltage on pin 49 of J1 or J2, respectively.

NOTE WinSystems can provide custom configurations for OEM clients. Please contact an Application Engineer for details.

4. Features

The IO60-DIO48 provides the following features:

Single Serial Peripheral Interface (SPI) chip select

- All functions are accessed through the SPI bus
- Supports future enhancements through firmware

General Purpose Input-Output (GPIO)

- 48 lines are provided within the Lattice Semiconductor Corp., MachXO2™ FPGA (field-programmable gate array)
- Level converters provide support up to 30 VDC
- Each line is configurable as an input or output with event sensing
- I/O greater than 5 V requires an external supply voltage applied to pin 49 of J1 or J2 (respectively)
- Current: 12 mA sink, 5 mA source (dependent on the user provided voltage)
- Programmable interrupts

5. General Operation

The design of the IO60-DIO48 provides 48 bits of general purpose I/O organized in six 8-bit I/O ports (0 through 5). The ports are accessed through two Serial Peripheral Interface (SPI) commands.

The SPI interface is implemented through the MACH XO2 SPI-slave EFB (Embedded Function Block) interface. Each bit of each port is implemented as a bi-directional tri-state driver. Each bit of each port can also be configured and enabled to detect rising and/or falling edge events and generate a system interrupt.

A read only interrupt status register is provided to simplify determination of the interrupt source when multiple simultaneous interrupts are enabled. The circuit is controlled by two simple SPI commands sent from an external SPI master device.

The SPI Master communicates with the Programmable Logic Device (PLD) through the SPI bus comprised of four signals (SLCK, MISO, MOSI, and SCSN). The SPI Chip Select signal (SCSN) must first be driven low prior to a valid SPI operation.

All command, address, and data bytes are transferred Most Significant Bit (MSB) first. SPI master data is captured on the rising clock edge and propagated on the falling clock edge. The SPI bus cycle is terminated by de-asserting SCSN. A SPI bus activity LED is also implemented and driven by Chip Select (CS) signals.

6. Specifications

The IO60-DIO48 adheres to the following specifications and requirements:

Electrical	
GPIO	3 V to 30 VDC
Vcc	3.3 V, 250 mA typical
Mechanical	
Dimensions	length 72 mm, width 50 mm
Weight	1.0 oz (29 gm)
PCB thickness	0.078 inch (1.98 mm)
Environmental	
Temperature	-40 °C to +85 °C
Humidity (RH)	5% to 95% non-condensing
Random Shock Testing	MIL-STD-202G, Method 213B, Condition A, 50g half-sine, 11ms duration per axis, 3 axis
Random Vibration Testing	MIL-STD-202G, Method 214A, Condition D, 01g/Hz (11.95g rms), 20 minutes per axis, 3 axis
RoHS Compliant	Yes
Operating Systems	
Windows and Linux x86/64-bit drivers and sample code are available for single board computers featuring IO60 expansion.	

Additional Accessories

A standoff kit part number, KIT-IO60-STANDOFF-2, is included for use with the IO60-DIO48. The kit contains the following items:

Component	Description	Qty
Standoff	Aluminum, 5 mm HEX,12 mm Long, 3.5 mm THREAD, Male/Female	2
Hex Nut	Zinc Finish, M3-0.5 DIN	2
Screw	Stainless Steel, M3 x 0.5 mm x 6 mm PPH	2

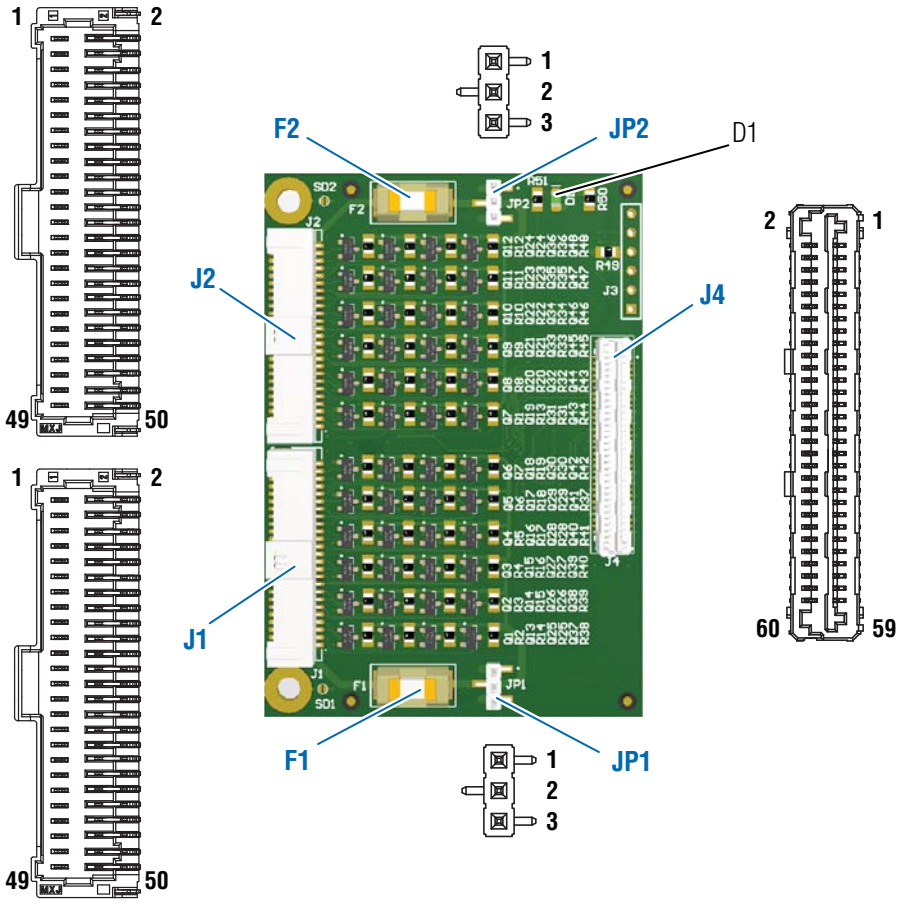
7. Configuration

This section describes the IO60-DIO48 components and configuration.

7.1 Component Layout

The IO60-DIO48 provides components on the top and bottom of the board.

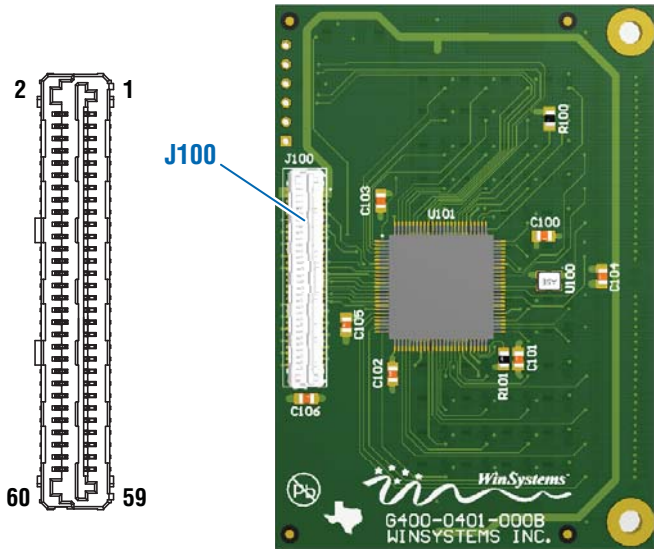
7.1.1 Top View



Top View Components:

Item	Description	Reference
J1	J1 General Purpose Input/Output Connector	page 8
J2	J2 General Purpose Input/Output Connector	page 10
J4	J4 IO60 Top Connector	page 6
JP1	JP1 Jumper	page 9
JP2	JP2 Jumper	page 11
D1	LED indicators	page 12
F1, F2	Fuse	page 5

7.1.2 Bottom View



Bottom View Components:

Item	Description	Reference
J100	J100 IO60 Bottom Connector	page 6

7.2 Power

The IO60-DIO48 draws power through the IO60 connector. It requires 5 VDC and 3.3 VDC and typically operates below 1 A. The power requirement varies depending on how the module is being utilized.

7.2.1 Fuse

Fuses (F1 and F2) have two purposes:

- When sourcing 5 V or 3.3 V power from pin 49 of J1 or J2, respectively, the fuse limits the current drawn by external circuits to 1 A.
- When receiving (3.3V – 30V) power on pin 49 of J1 or J2, respectively, from a user's system (for the purpose of supplying the logic level translation circuits), the fuse limits the current drawn by these circuits to 1 A.

Replace either fuse with only a fuse of the same rating: 1A,SB LITTLEFUSE (replacement part number 0454001). If the fuse repeatedly fails, correct the problem before replacing.

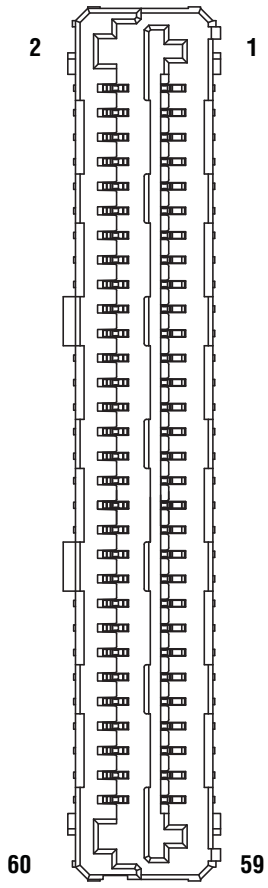
7.3 Embedded Computer Connection

The IO60-DIO48 is connected to a host embedded system through the IO60 interface (above the board through J4 or below the board through J100).

7.3.1 J4 IO60 Top Connector

Purpose: IO60 Expansion Interface Top Connection to host computer

Layout and Pin Reference:



Pin	Name	Pin	Name
1	VCC5	2	VCC5
3	VCC5	4	VCC5
5	TX	6	RX
7	RTS	8	CTS
9	GND	10	MUXCTRL
11	SCLK	12	MISO
13	SPI_CS0	14	MOSI
15	SPI_CS1	16	SPI_CS2
17	SPI_CS3	18	SPI_RDY
19	GND	20	GND
21	SCL	22	SDA
23	GND	24	GND
25	PWM0	26	EPITI
27	GND	28	GND
29	POR	30	GPIO_0
31	GPIO_1	32	GPIO_2
33	GPIO_3	34	GPIO_4
35	GPIO_5	36	GPIO_6
37	GPIO_7	38	NC
39	GND	40	GND
41	RSVD1	42	RSVD2
43	RSVD3	44	RSVD4
45	GND	46	GND
47	RSVD5	48	RSVD6
49	RSVD7	50	RSVD8
51	GND	52	GND
53	RSVD9	54	RSVD10
55	RSVD11	56	RSVD12
57	VCC3	58	VCC3
59	VCC3	60	VCC3

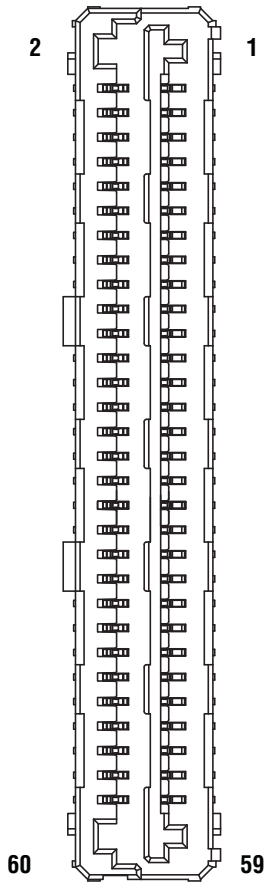
Additional Information

This connection uses a Samtec LSEM-130-06.0-L-DV-A-N-K-TR connector (WinSystems part number: G650-0060-070). Same matching connector.

7.3.2 J100 IO60 Bottom Connector

Purpose: IO60 Expansion Interface Bottom Connection to host computer

Layout and Pin Reference:



Pin	Name	Pin	Name
1	VCC5	2	VCC5
3	VCC5	4	VCC5
5	RX	6	TX
7	CTS	8	RTS
9	MUXCTRL	10	GND
11	MISO	12	SCLK
13	MOSI	14	SPI_CS0
15	SPI_CS2	16	SPI_CS1
17	SPI_RDY	18	SPI_CS3
19	GND	20	GND
21	SDA	22	SCL
23	GND	24	GND
25	EPITI	26	PWM0
27	GND	28	GND
29	GPIO_0	30	POR
31	GPIO_2	32	GPIO_1
33	GPIO_4	34	GPIO_3
35	GPIO_6	36	GPIO_5
37	GPIO_8	38	GPIO_7
39	GND	40	GND
41	RSVD2	42	RSVD1
43	RSVD4	44	RSVD3
45	GND	46	GND
47	RSVD6	48	RSVD5
49	RSVD8	50	RSVD7
51	GND	52	GND
53	RSVD10	54	RSVD9
55	RSVD12	56	RSVD11
57	VCC3	58	VCC3
59	VCC3	60	VCC3

Additional Information

This connection uses a Samtec LSEM-130-06.0-L-DV-A-N-K-TR connector (WinSystems part number: G650-0060-070). Same matching connector.

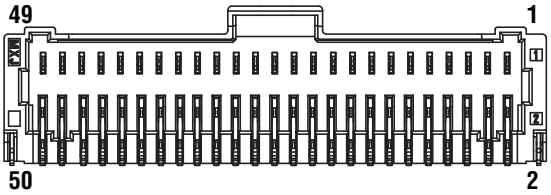
7.4 J1 General Purpose Input/Output Connector

The IO60-DIO48 provides 48 lines of bidirectional general purpose input-output (GPIO) through two connectors (J1 and J2). Jumper JP1 configures either a 5 V or 3.3 V range for the 24 I/O signals through J1 (GPIO0 through GPIO23). See “JP1 Jumper” on page 9.

Purpose: Connections for general purpose input and output functionality for signals GPIO0 through GPIO23. Jumper JP1 (see JP1 Jumper) determines the voltage range of the I/O for this connector.

Before supplying voltage to pin 49 of **J1**, remove any jumper installed on **JP1** (see JP1 Jumper on page 9). Damage to the board may occur if you apply an external voltage to pin 49 of **J1** while a jumper is installed on **JP1**.

Layout and Pin Reference:

Pin	Name	Pin	Name
			
1	Port 2 Bit 7 (GPIO23)	2	GND
3	Port 2 Bit 6 (GPIO22)	4	GND
5	Port 2 Bit 5 (GPIO21)	6	GND
7	Port 2 Bit 4 (GPIO20)	8	GND
9	Port 2 Bit 3 (GPIO19)	10	GND
11	Port 2 Bit 2 (GPIO18)	12	GND
13	Port 2 Bit 1 (GPIO17)	14	GND
15	Port 2 Bit 0 (GPIO16)	16	GND
17	Port 1 Bit 7 (GPIO15)	18	GND
19	Port 1 Bit 6 (GPIO14)	20	GND
21	Port 1 Bit 5 (GPIO13)	22	GND
23	Port 1 Bit 4 (GPIO12)	24	GND
25	Port 1 Bit 3 (GPIO11)	26	GND
27	Port 1 Bit 2 (GPIO10)	28	GND
29	Port 1 Bit 1 (GPIO9)	30	GND
31	Port 1 Bit 0 (GPIO8)	32	GND
33	Port 0 Bit 7 (GPIO7)	34	GND
35	Port 0 Bit 6 (GPIO6)	36	GND
37	Port 0 Bit 5 (GPIO5)	38	GND
39	Port 0 Bit 4 (GPIO4)	40	GND
41	Port 0 Bit 3 (GPIO3)	42	GND
43	Port 0 Bit 2 (GPIO2)	44	GND
45	Port 0 Bit 1 (GPIO1)	46	GND
47	Port 0 Bit 0 (GPIO0)	48	GND
49	VDD_IO	50	GND

Additional Information: This connector uses a 50-pin Molex® Pico-Clasp™ connector: Molex 501571-5007 (WinSystems part number: G650-2050-7HB). Matching connector:

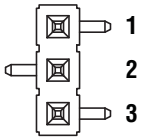
- MOLEX 501189-5010 (Housing)
- MOLEX 501193-2000 (Crimp)

7.4.1 JP1 Jumper

The presence and position of a jumper at JP1 specifies the I/O voltage source or voltage for GPIO of connector J1. The voltage selected sets the upper limit for general purpose input-output (GPIO) logic level translation. If an external voltage is supplied on J1-49 then that voltage must not exceed 30 VDC and no jumpers should be installed on JP1. In position **2-3,** 5 V I/O is selected. In position **1-2**, 3.3 V I/O is selected. When the jumper is removed and the user supplies VIN <30 V on pin 49 of J1, VIN I/O becomes the maximum range of the I/O signals.

Purpose: Determining voltage for General Purpose Input-Output (GPIO) on connector J1, the 24 I/O signals GPIO0 through GPIO23.

Jumper Pin Reference:

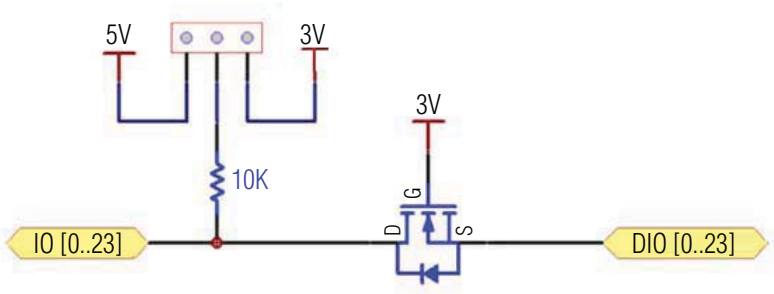
	Jumper	Voltage source
	1-2	3.3 V
	2-3	5 V
	open	External voltage supplied to Pin 49 of J4 (see STOP below)

Before supplying voltage to pin 49 of J1, remove any jumper installed on JP1. Damage to the board may occur if you apply an external voltage to pin 49 of J1 while a jumper is installed on JP1.

Pin Reference:

Pin	Function
1	+3.3 V
2	VDD_IO
3	+5 V

JP1 schematic



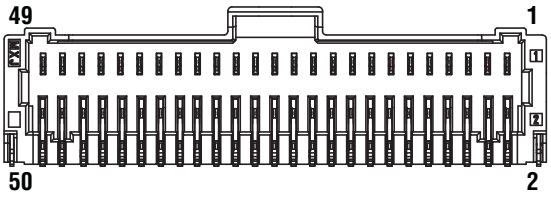
7.5 J2 General Purpose Input/Output Connector

The IO60-DIO48 provides 48 lines of bidirectional general purpose input-output (GPIO) through two connectors (J1 and J2). Jumper JP2 configures either a 5 V or 3.3 V range for the 24 I/O signals through J2 (GPIO24 through GPIO47).

Purpose: Connections for general purpose input and output functionality for signals GPIO24 through GPIO47. Jumper JP2 (see JP2 Jumper) determines the voltage range of the I/O for this connector. See “JP2 Jumper” on page 11.

Before supplying voltage to pin 49 of **J2**, remove any jumper installed on **JP2** (see JP2 Jumper). Damage to the board may occur if you apply an external voltage to pin 49 of **J2** while a jumper is installed on **JP2**.

Layout and Pin Reference:

Pin	Name	Pin	Name
			
1	Port 5 Bit 7 (GPIO47)	2	GND
3	Port 5 Bit 6 (GPIO46)	4	GND
5	Port 5 Bit 5 (GPIO45)	6	GND
7	Port 5 Bit 4 (GPIO44)	8	GND
9	Port 5 Bit 3 (GPIO43)	10	GND
11	Port 5 Bit 2 (GPIO42)	12	GND
13	Port 5 Bit 1 (GPIO41)	14	GND
15	Port 5 Bit 0 (GPIO40)	16	GND
17	Port 4 Bit 7 (GPIO39)	18	GND
19	Port 4 Bit 6 (GPIO38)	20	GND
21	Port 4 Bit 5 (GPIO37)	22	GND
23	Port 4 Bit 4 (GPIO36)	24	GND
25	Port 4 Bit 3 (GPIO35)	26	GND
27	Port 4 Bit 2 (GPIO34)	28	GND

Pin	Name	Pin	Name
29	Port 4 Bit 1 (GPIO33)	30	GND
31	Port 4 Bit 0 (GPIO32)	32	GND
33	Port 3 Bit 7 (GPIO31)	34	GND
35	Port 3 Bit 6 (GPIO30)	36	GND
37	Port 3 Bit 5 (GPIO29)	38	GND
39	Port 3 Bit 4 (GPIO28)	40	GND
41	Port 3 Bit 3 (GPIO27)	42	GND
43	Port 3 Bit 2 (GPIO26)	44	GND
45	Port 3 Bit 1 (GPIO25)	46	GND
47	Port 3 Bit 0 (GPIO24)	48	GND
49	VDD_IO	50	GND

Additional Information: This connector uses a 50-pin Molex® Pico-Clasp™ connector: Molex 501571-5007 (WinSystems part number: G650-2050-7HB). Matching connector:

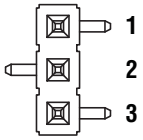
- MOLEX 501189-5010 (Housing)
- MOLEX 501193-2000 (Crimp)

7.5.1 JP2 Jumper

The presence and position of a jumper at JP2 specifies the I/O voltage source or voltage for GPIO of connector J2. The voltage selected sets the upper limit for general purpose input-output (GPIO) logic level translation. If an external voltage is supplied on J2-49 then that voltage must not exceed 30 VDC and no jumpers should be installed on JP1. In position **2-3,** 5 V I/O is selected. In position **1-2**, 3.3 V I/O is selected. When the jumper is removed and the user supplies VIN <30 V on pin 49 of J2, VIN I/O becomes the maximum range of the I/O signals.

Purpose: Determining voltage for General Purpose Input-Output (GPIO) on connector J1, the 24 I/O signals GPIO24 through GPIO47.

Jumper Pin Reference:

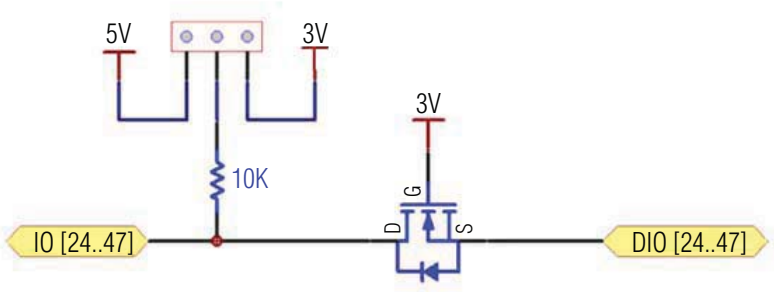
	Jumper	Voltage source
	1-2	3.3 V
	2-3	5 V
	open	External voltage supplied to Pin 49 of J4 (see STOP below)

Before supplying voltage to pin 49 of J2, remove any jumper installed on JP2. Damage to the board may occur if you apply an external voltage to pin 49 of J2 while a jumper is installed on JP2.

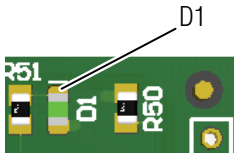
Pin Reference:

Pin	Function
1	+3.3 V
2	VDD_IO
3	+5 V

JP2 schematic



7.6 LED indicators

	LED	Description
	D1	Indicates SPI bus activity. This LED is driven by the buffered SCSN signal.

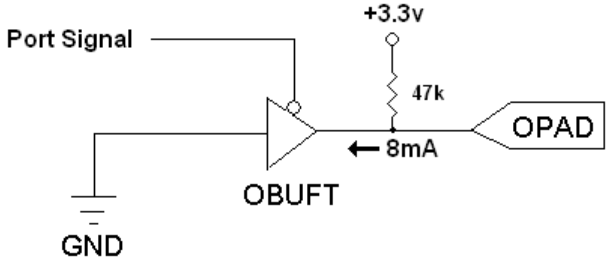
8. GPIO Registers

8.1 Functional Description

The IO60-DIO48 programmable logic device implements 48 bits of 30 V tolerant General Purpose Input-Output (GPIO). The 48-bit GPIO interface is organized as two ports comprised of six 8-bit registers. Each bit of each port is individually configurable as an input or output. Additionally, the general purpose I/O may be pulled up to the system 3.3 V, 5 V, or optionally to an external user supplied voltage (VCC1). This extends the range of signal levels that can be interfaced to the port.

All command, address, and data bytes are transferred Most Significant Bit (MSB) first. Serial Peripheral Interface (SPI) master data is captured on the rising clock edge and propagated on the falling clock edge. The SPI bus cycle is terminated by de-asserting the SPI Chip Select signal (SCSN). The SPI bus activity LED is also implemented and

driven by the one-hot embedded device Chip Select (CS) signals. Valid one-hot embedded chip select bytes are 0x01(GPIO), 0x02 (ADC), 0x04 (DAC).



Interface	Signal	I/O	Description
SPI INTERFACE	CCLK	I	SPI CLOCK
	SO	O	SPI SLAVE DATA OUT
	SI	I	SPI SLAVE DATA IN
	SCSN	I	SPI CHIP SELECT (ACTIVE LOW)
GENERAL SIGNALS	CLK	I	PLD LOGIC CLOCK
	RST_N	I	PLD LOGIC RESET (ACTIVE LOW)
	LED	O	SPI ACTIVITY LED (ACTIVE LOW)
GPIO SIGNALS	GPIO_P0	I/O	8 BITS OF DIGITAL I/O D[0:7]
	GPIO_P1	I/O	8 BITS OF DIGITAL I/O D[8:15]
	GPIO_P2	I/O	8 BITS OF DIGITAL I/O D[16:23]
	GPIO_P3	I/O	8 BITS OF DIGITAL I/O D[24:31]
	GPIO_P4	I/O	8 BITS OF DIGITAL I/O D[32:39]
	GPIO_P5	I/O	8 BITS OF DIGITAL I/O D[40:47]
	INT_N	O	GPIO INTERUPT (ACTIVE LOW)

8.2 GPIO Registers

This device provides 48 lines of general purpose I/O. The 48 bits are organized as six 8-bit ports (Port 0, Port 1, Port 2, Port 3, Port 4, and Port 5). There are 30 unique registers used to configure and control the GPIO.

- Registers 10H through 15H are used to enable rising edge detection interrupts on Ports 0 through 5.
- Registers 20H through 25H are used to enable falling edge detection interrupts on Ports 0 through 5.
- Registers 30H through 35H are used to clear the interrupts from Ports 0 through 5.
- Registers 40H through 45H are used to determine the source of the interrupts from Ports 0 through 5.

GPIO Registers

Address	Type	Description	Default
0x00	R/W	Port 0 - GPIO[7:0]	0xFF
0x01	R/W	Port 1 - GPIO[15:8]	0xFF
0x02	R/W	Port 2 - GPIO[23:16]	0xFF
0x03	R/W	Port 3 - GPIO[31:24]	0xFF
0x04	R/W	Port 4 - GPIO[39:32]	0xFF
0x05	R/W	Port 5 - GPIO[47:40]	0xFF
0x10	R/W	Port 0 - Rising Edge Interrupt Enable (1=Enabled, 0=Disabled)	0x00
0x11	R/W	Port 1 - Rising Edge Interrupt Enable (1=Enabled, 0=Disabled)	0x00
0x12	R/W	Port 2 - Rising Edge Interrupt Enable (1=Enabled, 0=Disabled)	0x00
0x13	R/W	Port 3 - Rising Edge Interrupt Enable (1=Enabled, 0=Disabled)	0x00
0x14	R/W	Port 4 - Rising Edge Interrupt Enable (1=Enabled, 0=Disabled))	0x00
0x15	R/W	Port 5 - Rising Edge Interrupt Enable (1=Enabled, 0=Disabled)	0x00
0x20	R/W	Port 0 - Falling Edge Interrupt Enable (1=Enabled, 0=Disabled)	0x00
0x21	R/W	Port 1 - Falling Edge Interrupt Enable (1=Enabled, 0=Disabled)	0x00
0X22	R/W	Port 2 - Falling Edge Interrupt Enable (1=Enabled, 0=Disabled)	0x00
0X23	R/W	Port 3 - Falling Edge Interrupt Enable (1=Enabled, 0=Disabled)	0x00
0X24	R/W	Port 4 - Falling Edge Interrupt Enable (1=Enabled, 0=Disabled))	0x00
0x25	R/W	Port 5 - Falling Edge Interrupt Enable (1=Enabled, 0=Disabled)	0x00
0X30	R/W	Port 0 - Clear Interrupt (1=Clear,0=Enabled)	0x00
0X31	R/W	Port 1 - Clear Interrupt (1=Clear,0=Enabled)	0x00
0X32	R/W	Port 2 - Clear Interrupt (1=Clear,0=Enabled)	0x00
0X33	R/W	Port 3 - Clear Interrupt (1=Clear,0=Enabled)	0x00
0x34	R/W	Port 4 - Clear Interrupt (1=Clear,0=Enabled)	0x00
0x35	R/W	Port 5 - Clear Interrupt (1=Clear,0=Enabled)	0x00
0x40	R	Port 0 - Interrupt Status (1=interrupt occurred)	0x00
0X41	R	Port 1 - Interrupt Status (1=interrupt occurred)	0x00
0X42	R	Port 2 - Interrupt Status (1=interrupt occurred)	0x00
0x43	R	Port 3 - Interrupt Status (1=interrupt occurred)	0x00
0X44	R	Port 4 - Interrupt Status (1=interrupt occurred)	0x00
0X45	R	Port 5 - Interrupt Status (1=interrupt occurred)	0x00

GPIO Registers (0x00-0x05)—Writing a 0 to any bit in the GPIO registers will drive out a LVCMOS low level on the corresponding output pin. Writing a 1 to any bit in the GPIO registers tri-states the driver allowing an external source to drive the pin. All ports default to inputs.

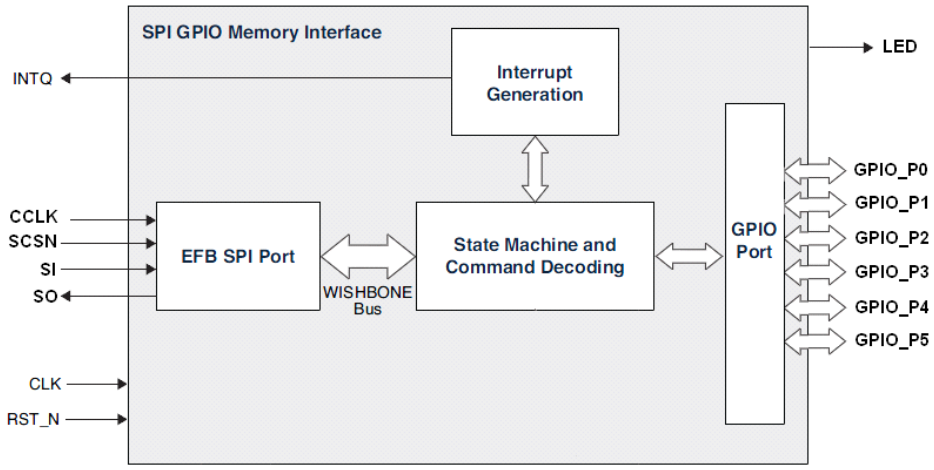
Rising Edge Interrupt Enable Registers (0x10-0x15)—Writing a 1 to any bit in these registers enables interrupts for rising edge events on the corresponding GPIO bit. Writing a 0 disables rising edge interrupts on the same bit. The default value is all rising edge interrupts disabled.

Falling Edge Interrupt Enable Registers (0x20-0x25)—Writing a 1 to any bit in these registers enables interrupts for falling edge events on the corresponding GPIO bit. Writing a 0 disables falling edge interrupts on the same bit. The default value is all falling edge interrupts disabled.

Interrupt Clear Registers (0x30-0x35)—Writing a 0 to any bit in these registers clears the corresponding status register bit and disables the interrupts from the corresponding GPIO pin. Writing a 1 to the same bit then re-enables interrupts for the corresponding channel.

Interrupt Status Registers (0x40-0x45)—These are read only registers. If a bit is set it indicates that the corresponding channel has caused an interrupt.

Erroneous Commands—The IO60-DIO48 design ignores unsupported SPI commands and incorrectly formatted SPI bus cycles.



9. SPI Bus

9.1 Component

The Lattice Semiconductors LCMXO2-4000HC is used on this board to implement a SPI slave to GPIO48 function. This device is part of the MACH XO2 family of Programmable Logic Devices with Embedded Function Blocks (PLDs with EFBs) and is scalable from 4000-N LUTs in a pin compatible BGA256 package.

9.2 Features

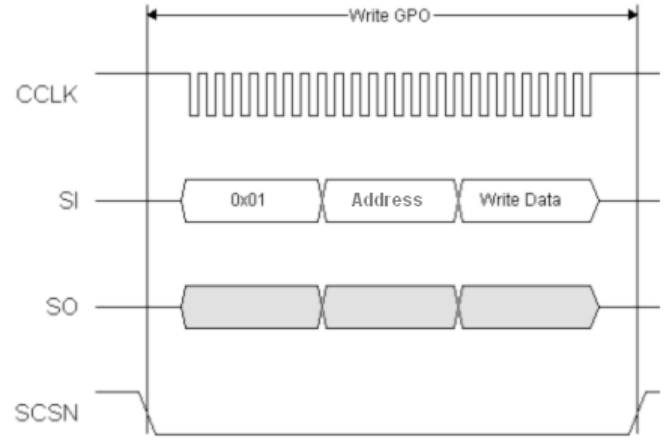
The PLD provides the system programmer an interface to any combination of 48 discrete digital inputs or outputs. Each GPIO signal is implemented as a bidirectional open drain type output with a weak pull-up resistor. The GPIO signal pin sinks the net low (8 mA) when a binary "1" is written to the port and is tri-stated and pulled to 3.3V through a weak 50KΩ pull-up resistor when a binary "0" is written to the port. When the GPIO pin is tri-stated the pin functions as an input and the level is controlled by external system logic. When configured as an input or output a physical interrupt can be detected and generated from the rising edge, falling edge, or both edges of any individual GPIO signal.

9.3 SPI Commands

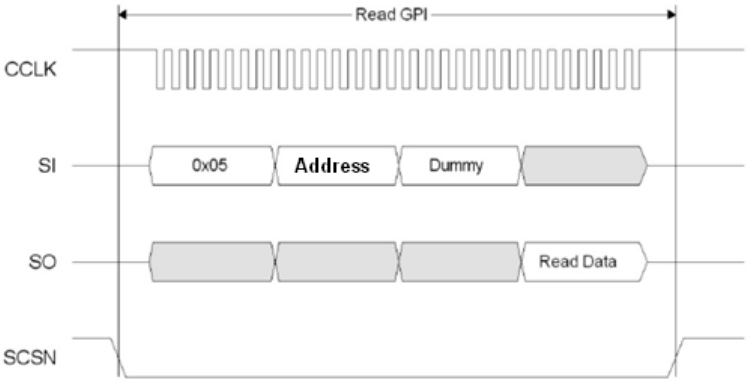
The following table contains supported Serial Peripheral Interface (SPI) commands.

Operation	Command	Address byte	Stuffing byte	Data byte
WRITE REG	0x01	1	-	1
READ REG	0x05	1	1	1
READ REVID	0x9F	-	1	1
LED OFF	0x06	-	-	-
LED ON	0x04	-	-	-

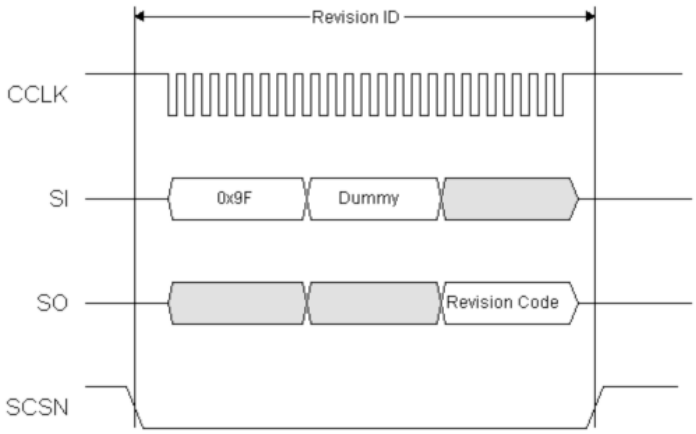
Write REG Command—The Write REG command is a three byte command. The first byte is the command ID 0x01. The second byte is the register address (0x00-0x45). The third and last byte is the Write Data.



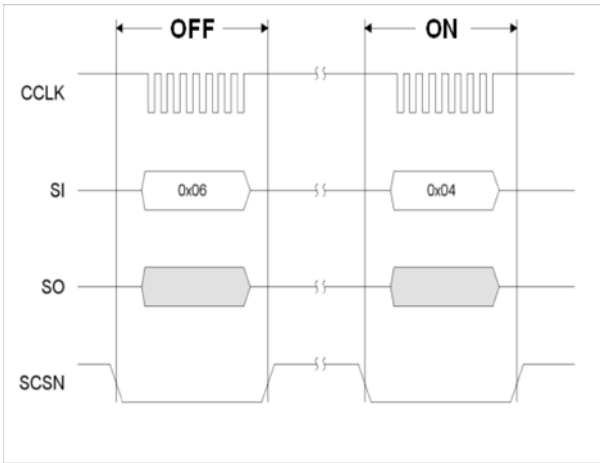
Read REG Command—The Read REG command is a four byte command. The first byte is the command ID 0x05. The second byte is the register address (0x00-0x19). The third byte is a dummy or stuffing byte 0xFF. The fourth and last byte is the Read Data.



Read REVID Command—The Read REVID command is a three byte command. The first byte is the command ID 0x9f. The second byte is a stuffing byte (any 8 bit value). The third byte is the revision ID of the PLD.



LED Commands—These one-byte commands control an on-board LED and are used for diagnostics. The command ID 0x06 turns off the onboard LED, while the command ID 0x04 turns on the LED.The ability to turn ON/OFF the onboard LED can be useful to software developers when trying to initially establish SPI communications.



10. Software Drivers

Go to www.winsystems.com for information on available software drivers.

Appendix A. Best Practices

The following paragraphs outline the best practices for operating the IO60-DIO48 in a safe, effective manner, that will not damage the board. Please read this section carefully.

Avoid Electrostatic Discharge (ESD)—Only handle the circuit board and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

Power Down

Make sure that power has been removed from the system before making or breaking any connections.

Power Supply OFF—The power supply should always be off before it is connected to the I/O Module. Do not hot-plug the IO60-DIO48 on a host platform that is already powered.

I/O Connections OFF—I/O Connections should also be off before connecting them to the embedded computer modules or any I/O cards. Connecting hot signals can cause damage whether the embedded system is powered or not.

Mounting and Protecting the Digital Input Output Module

The IO60-DIO48 must be mounted properly to avoid damage. You can order additional standoff kits from WinSystems, part number KIT-IO60-STANDOFF-2. The kit contains the following items:

Component	Description	Qty
Standoff	Aluminum, 5 mm HEX,12 mm Long, 3.5 mm THREAD, Male/Female	2
Hex Nut	Zinc Finish, M3-0.5 DIN	2
Screw	Stainless Steel, M3 x 0.5 mm x 6 mm PPH	2

Placing the IO60-DIO48 on Mounting Standoffs—Be careful when placing the IO60-DIO48 on the mounting standoffs. Sliding the board around until the standoffs are visible from the top can cause component damage on the bottom of the board.

Do Not Bend or Flex the IO60-DIO48—Bending or flexing can cause irreparable damage. Embedded computer modules are especially sensitive to flexing or bending around Ball Grid Array (BGA) devices. BGA devices are extremely rigid by design and

flexing or bending the embedded computer module can cause the BGA to tear away from the printed circuit board.

Mounting Holes—The mounting holes are plated on the top, bottom and through the barrel of the hole and are connected to the embedded computer module's ground plane. Traces are often routed in the inner layers right below, above or around the mounting holes.

- Never use a drill or any other tool in an attempt to make the holes larger.
- Never use screws with oversized heads. The head could come in contact with nearby components causing a short or physical damage.
- Never use self-tapping screws; they will compromise the walls of the mounting hole.
- Never use oversized screws that cut into the walls of the mounting holes.
- Always use all of the mounting holes. By using all of the mounting holes you will provide the support the embedded computer module needs to prevent bending or flexing.

Plug or Unplug Connectors Only on Fully Mounted Boards—Never plug or unplug connectors on a board that is not fully mounted. Many of the connectors fit rather tightly and the force needed to plug or unplug them could cause the embedded computer module to be flexed.

Avoid Cutting the IO60-DIO48—Never use star washers or any fastening hardware that will cut into the IO60-DIO48.

Avoid Over-tightening of Mounting Hardware—Causing the area around the mounting holes to compress could damage interlayer traces around the mounting holes.

Use Appropriate Tools—Always use tools that are appropriate for working with small hardware. Large tools can damage components around the mounting holes.

Avoid Conductive Surfaces—Never allow the embedded computer module to be placed on a conductive surface. Many embedded systems use a battery to back up the clock-calendar and CMOS memory. A conductive surface such as a metal bench can short the battery causing premature failure.

Conformal Coating

Conformal coating by any source other than WINSYSTEMS voids the product warranty and will not be accepted for repair by WINSYSTEMS. If such a product is sent to WINSYSTEMS for repair, it will be returned at customer expense and no service will be performed. A WINSYSTEMS product conformally coated by WINSYSTEMS will be subject to regular WINSYSTEMS warranty terms and conditions.

Operations/Product Manuals

Every single board computer has an Operations manual or Product manual.

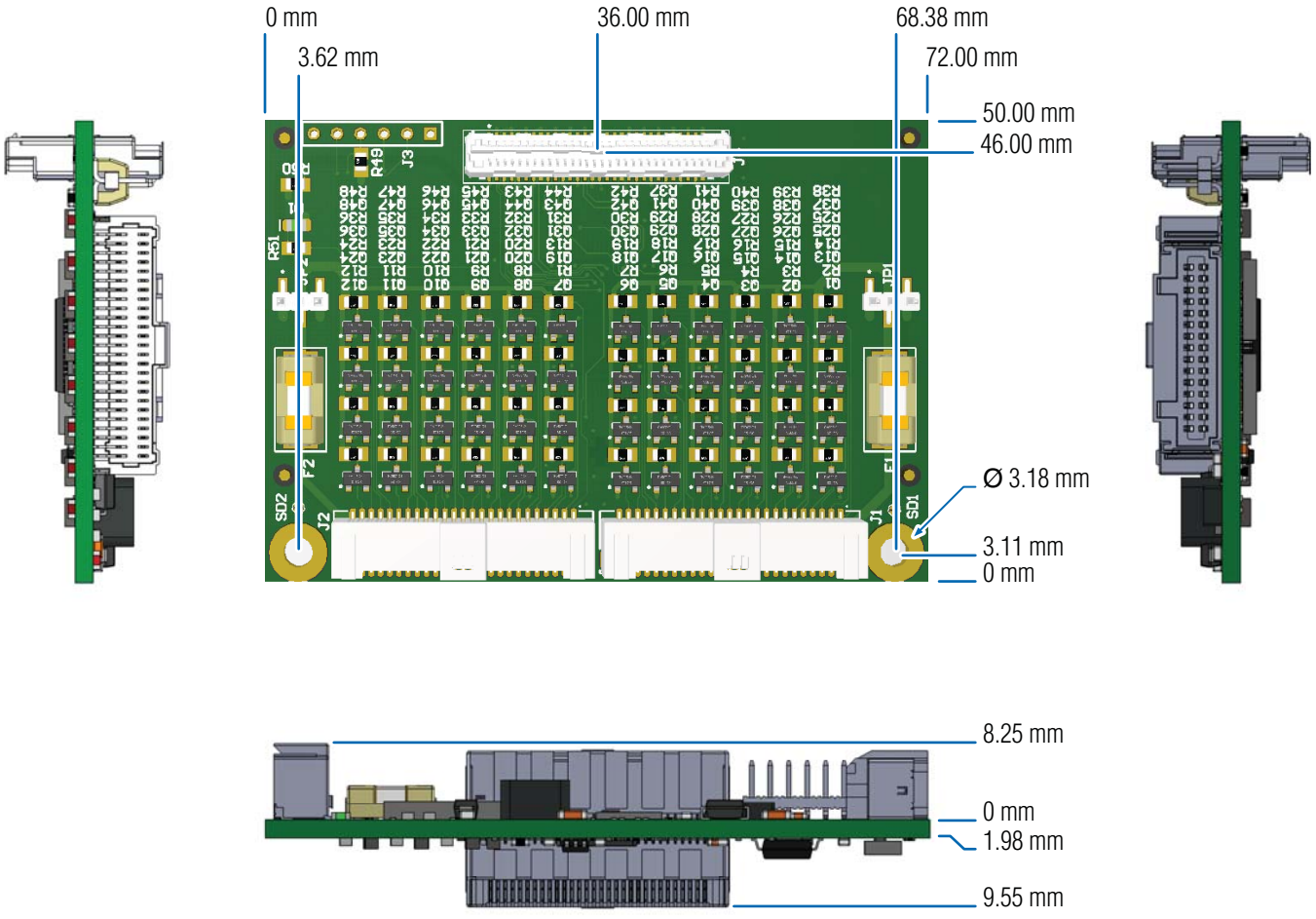
Periodic Updates—Operations/Product manuals are updated often. Periodically check the WinSystems website (https://www.winsystems.com) for revisions.

Check Pinouts—Always check the pinout and connector locations in the manual before plugging in a cable. Many I/O modules will have identical headers for different functions and plugging a cable into the wrong header can have disastrous results.

Contact an Applications Engineer—If a diagram or chart in a manual does not seem to match your board, or if you have additional questions, contact a WinSystems Applications Engineer at: +1-817-274-7553.

Appendix B. Mechanical Drawings

IO60-DIO48 Digital Input Output Module



Appendix C. Warranty Information

Full warranty information can be found at https://winsystems.com/company-policies/warranty/.