WINSYSTEMS®

EBC-C413

Industrial EBX Single Board Computer with Intel® Atom™ E3800 processor, PC104-Plus, and Digital I/O

Product Manual

WINSYSTEMS, Inc. | 2890 112th Street, Grand Prairie, Texas 75050 | 817-274-7553 | info@winsystems.com | www.winsystems.com

Revision History

Document Version	Last Updated Date	Brief Description of Change
v1.0	11/2016	Initial release
v1.1	5/2017	Added DIO jumpers
v1.2	11/2018	Added FPGA Configuration EEPROM
v2,0	11/2019	Rebranded manual, updated graphics, fixed jumper name JPSATA to JPMSATA under section 7.1.3, fixed various typos
V2.1	8/2020	Added MTBF information in specifications table
V2.2	7/29/2025	Updated Conformal Coating, added Warranty link, updated all links

Copyright and Trademarks

Trademark Acknowledgments

Table of Contents

1. Introduction

This manual provides configuration and usage information for the EBC-C413. The EBC-C413 is a full-featured embedded single board computer (SBC) with digital I/O. If you still have questions after reviewing this manual, contact WINSYSTEMS Technical Support at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

Refer to the WINSYSTEMS website for other accessories (including cable drawings and pinouts) that can be used with your EBC-C413.

2. Functionality

The EBC-C413 is a full-featured, EBX-compatible, embedded single board computer (SBC) that supports Linux, Windows® 10 desktop, Windows 10 IoT, and other x86-compatible real-time operating systems. Refer to "Features" on page 6 and "General Operation" on page 9 for additional information.

NOTE WINSYSTEMS can provide custom configurations for Original Equipment Manufacturer (OEM) clients. Contact an Application Engineer through technical support for details (see the Introduction paragraph on this page for details).

3. Features

This section describes the features of the EBC-C413.

Single Board Computer

- EBX-compatible single board computer (SBC) with stacked PC104-Plus connectors
- Soldered-down multi-core Intel® Atom™ E3800 processor. Available options:
  - E3815 single-core, 1.46 GHz
  - E3827 dual-core, 1.33 GHz
  - E3845 quad-core, 1.91 GHz

Operating Systems (compatible)

- Windows Embedded 7, 8, and 8.1
- Windows 7, 8, and 10 (32/64-bit)
- Linux
- Other x86-compatible systems

Memory

- SODIMM 204-pin DDR3L compatible socket (one socket, maximum of 8 GB RAM)

BIOS

- InsydeH2O®

Video Interfaces (one or two simultaneously active displays)

- Dual video with simultaneous CRT, DisplayPort or LVDS with PWM backlight support

Ethernet

- Intel i210 Gigabit Ethernet (1 gigabit per second, GbE) with surge suppression (2 ports)

Storage

- mSATA socket (multiplexed with the MiniCard connector MC2)
- SATA 2.0 connector
- CFast
- USB

Digital Input/Output (General Purpose Input/Output - GPIO)

- 48 (bidirectional) I/O lines with 24 lines capable of event sense interrupt generation (DIO1)
- External voltage translators allow the signals to drive or sink up to 5 VDC

Bus Expansion

- PC104-Plus (PC104 and PCI-104)
- MiniCard sockets (two sockets, MC2 multiplexed with mSATA)

Serial Interface

- Eight USB 2.0 ports with ESD suppression
- Four serial ports (RS232 and RS422/485 configurable)

Audio

- 7.1 HD audio including connections for line-in, line-out, rear, side, center, low frequency effects (LFE), two microphones, and CD

Power

- +5 VDC power input (main supply to EBC-C413)

- If provided, the +12 VDC and -12 VDC supplies the PC104 and PC104-Plus connector. Also, some flat-panel displays require +12 VDC.

Industrial Operating Temperature

- Fanless -40°C to +85°C (-40°F to +185°F)
- Fan control provided (fan powered from FAN connector, +12 VDC)

Additional Features

- Watchdog timer from 1 second to 255 minutes
- Real-Time Clock (RTC) with optional battery back up
- Software controlled activity LED
- BIOS buzzer alerts (beeps) to indicate POST failure

4. Before You Begin

Review the warnings in this section and the best practice recommendations (see “Best Practices” on page 71) when using and handling the WINSYSTEMS EBC-C413. Adherence to these recommendations provides an optimal user experience and prevents damage. Read this document and become familiar with the EBC-C413 before proceeding.

APPLYING CONFORMAL COATING AFTER PURCHASE WILL VOID YOUR WARRANTY. FAILING TO COMPLY WITH THESE BEST PRACTICES MAY DAMAGE THE PRODUCT AND VOID YOUR WARRANTY.

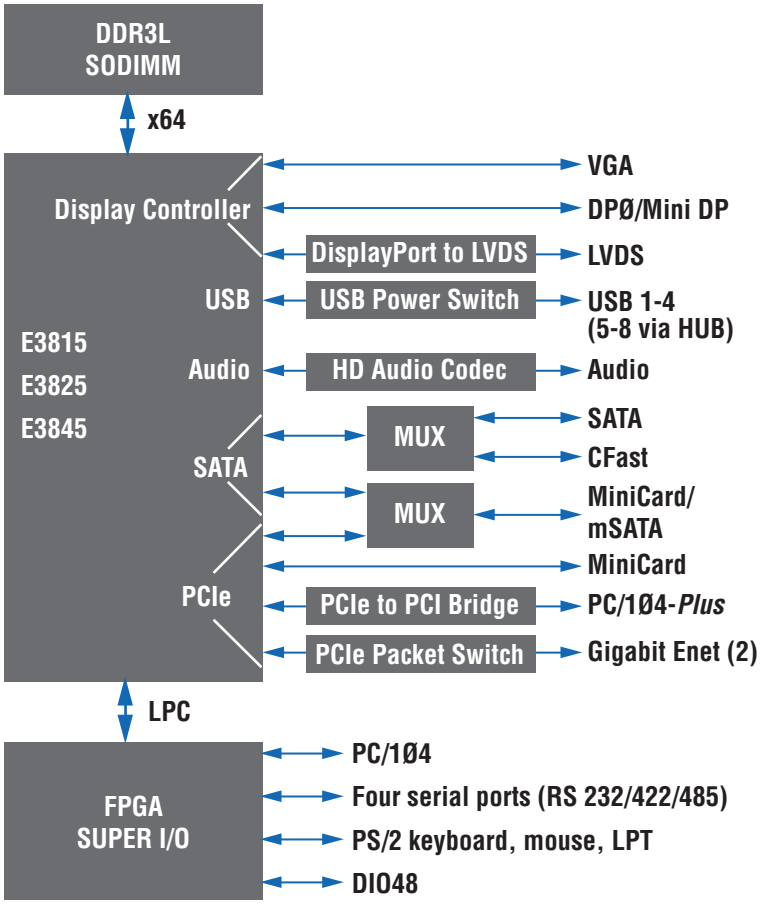
4.1 Warnings

Only qualified personnel should configure and install the EBC-C413. While observing the best practices, pay particular attention to the following:

Avoid Electrostatic Discharge (ESD)
Only handle the circuit board and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

5. General Operation

The EBC-C413 is a single board computer (SBC). It is a full-featured embedded system with a variety of onboard I/O options. The following figure is a simplified system block diagram of the EBC-C413.



Three display interfaces (VGA, DP Mini DisplayPort, and LVDS) support dual video (up to two simultaneous independent displays) along with stereo audio. Communication interfaces include two Gigabit Ethernet ports, eight USB 2.0 ports with ESD suppression, four serial, 48 digital I/O lines with event sense, a watchdog timer, a PS/2 keyboard and mouse controller, and a parallel port (LPT).

The EBC-C413 can provide an upgrade for an existing EBX-compatible SBC. It is designed for harsh environments and reliability, featuring added shock and vibration resistance, and provides a fanless solution for operating temperatures between -40°C and +85°C (-40°F and +185°F).

The EBC-C413 processor options provide single, dual, or quad-core processing. Each soldered-processor option can support up to 8 GB of DDR3L memory and optional stackable PC104-Plus connectors.

Operating systems such as Linux or Windows can be initialized from the SATA, mSATA, or USB interfaces. This provides flexible data storage options.

6. Specifications

The EBC-C413 adheres to the following specifications and requirements.

Electrical	
V_{CC}	+5 VDC ±5%, 1.7 A typical, 2.2 A maximum
Processor	**3815:** E3815 single-core 1.46 GHz, 512 K cache (MOQ required) **3825:** E3825 dual-core 1.33 GHz, 1 MB cache **3845:** E3845 quad-core 1.91 GHz, 2 MB cache
Mechanical	
Dimensions	5.75 x 8.00 in. (146 x 203 mm)
Weight	1.19 lb. (0.540 kg) with heatsink
PCB Thickness	0.078 in. (1.98 mm)
Environmental	
Temperature	-40°C to +85°C (-40°F to +185°F)
Humidity (RH)	5% to 95% non-condensing
Mechanical Shock Testing	MIL-STD-202G, Method 213B, Condition A 50g half-sine, 11 ms duration per axis, 3 axis
Random Vibration Testing	MIL-STD-202G, Method 214A, Condition D .1g/Hz (11.95g rms), 20 minutes per axis, 3 axis
Mean time between failure (MTBF) [a]	Prediction Method: Bellcore TR-332 Issue 6 MTBF (hours) 91457.85 MTBF (years) 10.44
RoHS Compliant	Yes
Operating Systems	
Runs 32/64-bit Windows, Linux, and other x86-compatible operating systems.	

a. A MTBF measurement is based on a statistical sample and is not intended to predict any one specific unit's reliability; thus MTBF is not, and should not be construed as, a warranty measurement.

7. Configuration

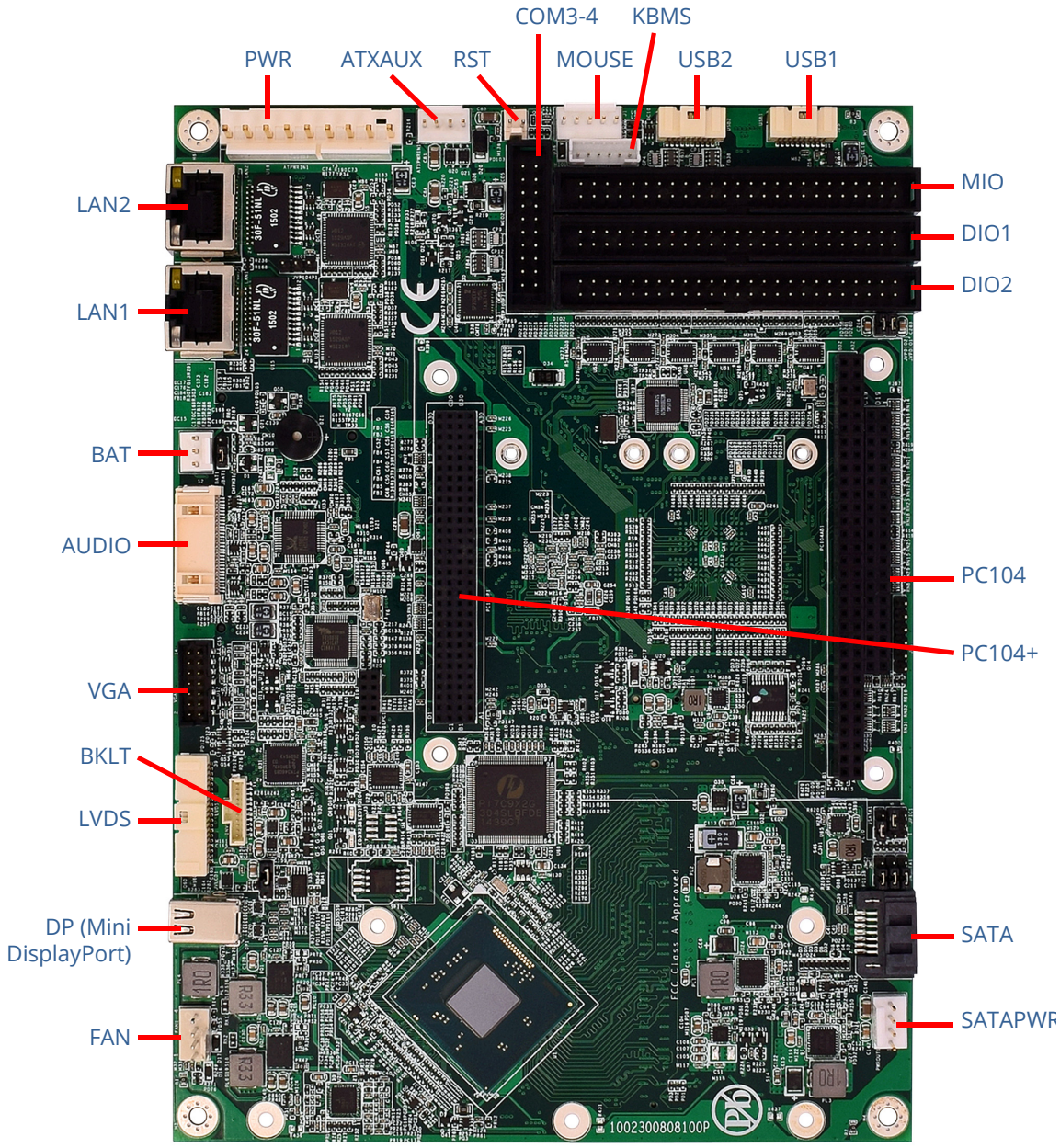
This section describes the EBC-C413 components and configuration.

7.1 Component Layout

The EBC-C413 provides components on the top and bottom of the board.

7.1.1 Top View Connectors

The following figure illustrates the location of each connector on the top of the EBC-C413.

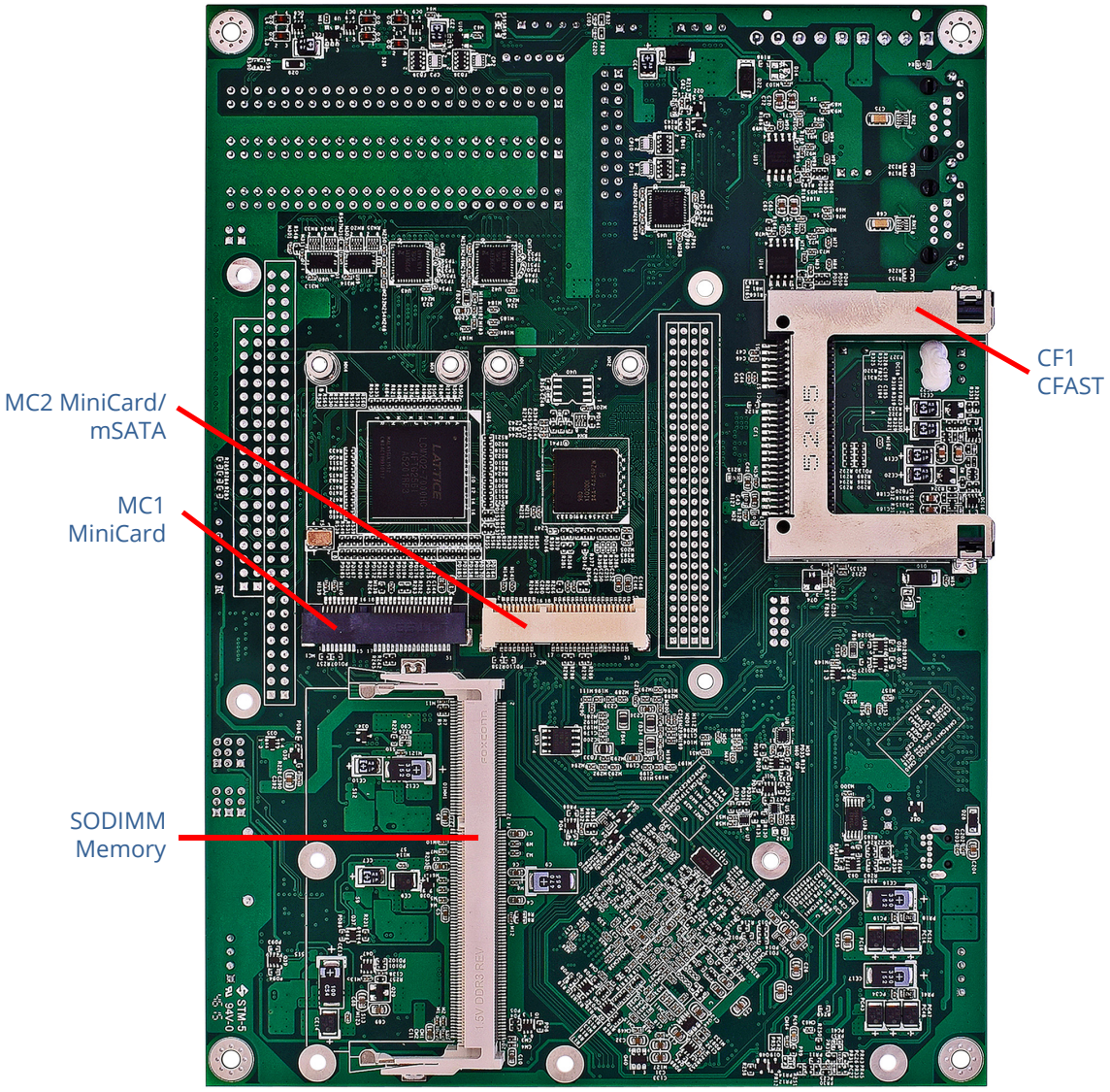


The following table provides connector descriptions and references for the figure above.

Item	Connector and Description	Page
PWR	PWR - Power Connector	page 23
ATXAUX	ATXAUX - ATX/Auxiliary Power Connector	page 24
COM3-4	COM3-4 - COM3 and COM4 Serial Ports	page 25
MIO	MIO - PS/2 Keyboard, Serial 1/2, and LPT	page 26
RST	RST - Reset Connector (Reset)	page 28
MOUSE	MOUSE - PS/2 Mouse Connector	page 28
KBMS	KBMS - Reserved	page 29
USB1	USB1 - USB Connector for Ports 0-3	page 29
USB2	USB2 - USB Connector for Ports 4-7	page 30
DIO1	DIO1 - Digital I/O Connector with Event Sense	page 31
DIO2	DIO2 - Digital I/O Connector	page 33
PC104AB PC104CD	PC104AB - PC104 8-bit Bus Connector PC104CD - PC104 16-bit (Includes PC104AB) Bus Connector	page 34
PC104P	PC104P - PC104-Plus/PC104 Bus Connector	page 36
SATA1	SATA1 - Serial ATA Connector	page 38
SATAPWR	SATAPWR - Serial ATA Power Connector	page 38
FAN	FAN - Connector for Optional Fan	page 39
LVDS	LVDS - LVDS Display Output Connector	page 39
BKLT	BKLT - Backlight Power and Control Connector	page 41
VGA	VGA - Analog VGA Display Connector	page 41
DP	DP - Mini DisplayPort Connector	page 42
BAT	BAT - External Battery Connector	page 43
AUDIO	AUDIO - HD Audio Connector	page 44
LAN1/LAN2	LAN1/LAN2 - Ethernet LAN Connectors	page 45

7.1.2 Bottom View Components

The following figure illustrates the location of each connector on the bottom of the EBC-C413.

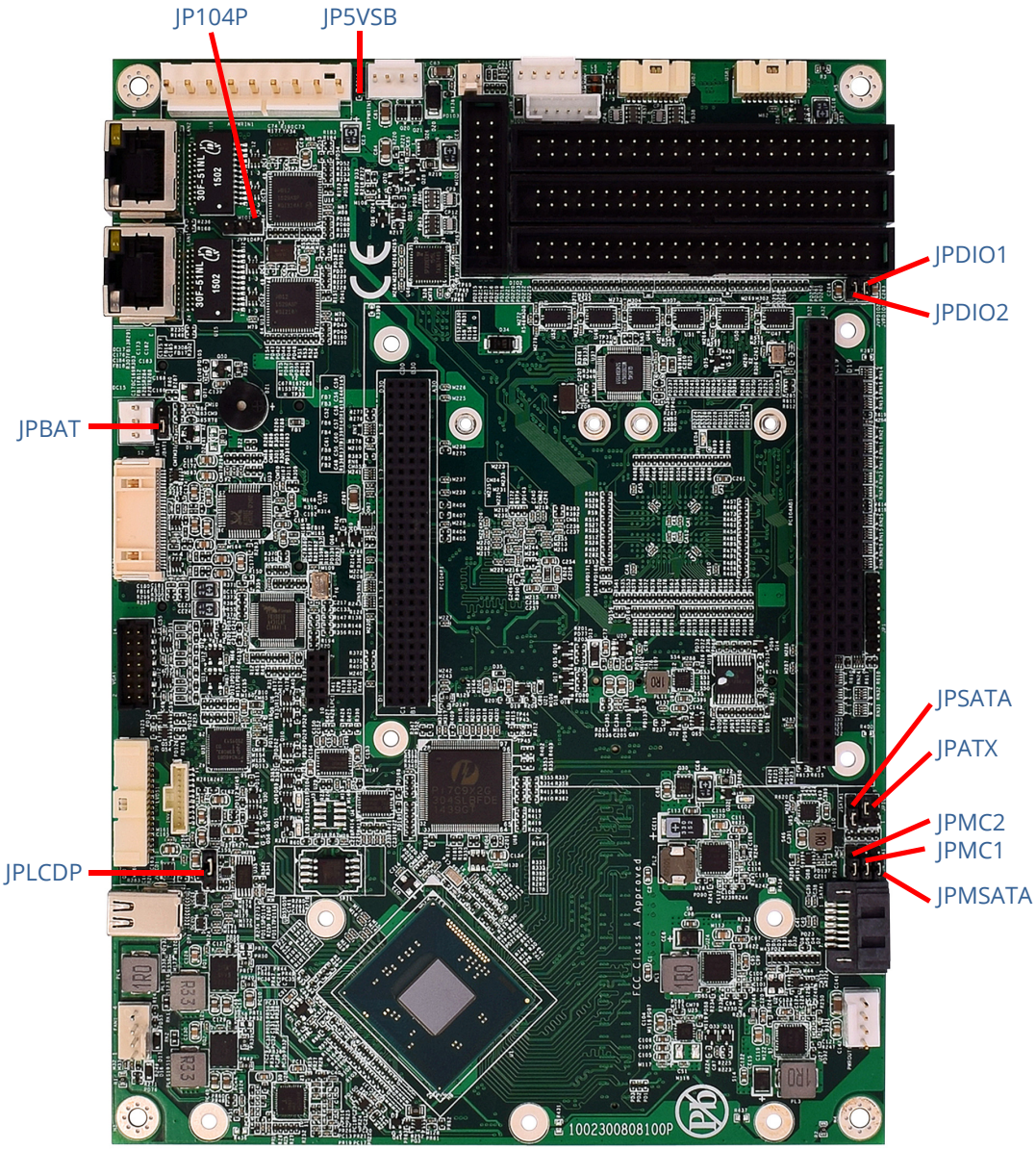


The following table provides connector descriptions and references for the figure above.

Item	Connector and Description	Page
MC1	MC1 - MiniCard Connector with PCI-Express and USB	page 46
MC2	MC2 - MiniCard/mSATA Connector with PCI-Express, USB, and SATA	page 47
CF1	CF1 - CFast SSD Connector	page 50
SODIMM0	204-pin SODIMM Socket for System Memory	page 51

7.1.3 Jumpers

The following figure illustrates the location of each jumper on the EBC-C413.



The following table provides jumper descriptions and references for the figure above.

Item	Jumper and Description	Reference
JP104P	JP104P - PCI-104 Power Source Select	page 51
JP5VSB	JP5VSB - 5V Standby Power Select	page 51
JPDIO1	JPDIO1 - Power Enable (+5 VDC) to Pin 49 of DIO1	page 51

Item	Jumper and Description	Reference
JPDIO2	JPDIO2 - Power Enable (+5 VDC) to Pin 49 of DIO2	page 52
JPSATA	JPSATA - Serial ATA Device Select	page 52
JPATX	JPATX - AT/ATX Power Supply Select	page 52
JPMC1	JPMC1 - MC1 Wireless LAN Enable	page 52
JPMC2	JPMC2 - MC2 Wireless LAN Enable	page 53
JPMSATA	JPMSATA - MC2 mSATA/MiniCard Select	page 53
JPLCDP	JPLCDP - LCD Panel Power Configuration	page 53
JPBAT	JPBAT - RTC Battery Enable	page 53

7.2 I/O Port Map

The EBC-C413 uses plug-and-play (PnP) BIOS resource allocation. Take care to avoid contention with resources allocated by the BIOS.

The EBC-C413 utilizes a Low Pin Count to Industry Standard Architecture bridge (LPC to ISA bridge) to address the PC104 bus. Most legacy PC104 modules are I/O mapped and function as expected. The LPC controller is the subtractive agent of the Intel Legacy Block. All transactions that are not claimed elsewhere are sent to the LPC controller. The LPC to ISA bridge does not implement bus mastering cycles or direct memory access (DMA).

The following tables contain the I/O ports used on the EBC-C413.

PCU I/O Address	Device
0000h-001Fh	DMA Controller 82C37
0020h-0021h	Interrupt Controller PIC 8259
0024h-0025h	Interrupt Controller
0028h-0029h	Interrupt Controller
002Ch-002Dh	Interrupt Controller
002Eh-002Fh	Forward to Super IO
0030h-0031h	Interrupt Controller
0034h-0035h	Interrupt Controller
0038h-0039h	Interrupt Controller
003Ch-003Dh	Interrupt Controller
0040h-0043h	Timer Counter 8254
004Eh-004Fh	Forward to Super IO
0050h-0053h	Timer Counter 8254
0060h	Keyboard Data Port
0061h	NMI Controller
0062h	8051 download 4K address counter
0064h	Keyboard Status Port
0066h	8051 Download 8-bit Data Port

PCU I/O Address	Device
0070h-0077h	RTC Controller
0080h-0091h	DMA Controller
0092h	Reset Generator
0093h-009Fh	DMA Controller
00A0h-00A1h	Interrupt Controller PIC 8259
00A4h-00A5h	Interrupt Controller
00A8h-00A9h	Interrupt Controller
0ACh-00ADh	Interrupt Controller
00B0h-00B1h	Interrupt Controller
00B2h-00B3h	Power Management
00B4h-00B5h	Interrupt Controller
00B8h-00B9h	Interrupt Controller
00C0h-00DFh	DMA Controller 82C37
00F0h	FERR#/IGNNE/Interrupt Controller
0120h-012Fh	Digital I/O (Default)
0140h-01FFh	Reserved
0170h-0177h	IDE1 Controller
0180h-01FFh	Reserved
0270h-0277h	FPGA Configuration EEPROM
0298h-029Bh	Reserved for Super I/O Configuration
029Ch	Interrupt Status Register
029Dh	Status LED Register
029Eh-029Fh	Watchdog Timer Control
02E8h-02EFh	COM4 (Default)
02F8h-02FFh	COM2 (Default)
0340h-03E7h	Reserved
0376h	IDE1 Controller
0378h-037Bh	LPT (Default)
03E8h-03EFh	COM3 (Default)
03F0h-03F5h	Reserved
03F6h	IDE0 Controller
03F8h-03FFh	COM1 (Default)
0400h-047Fh	Reserved ACPI
0564h-0568h	Advanced Watchdog
0800h-08FFh	Reserved
0CF9h	Reset Generator
2000-201Fh	Reserved SMBus
FED1C000h-FED1C3FFh	Reserved RCBA

7.3 Interrupt Map

The EBC-C413 supports hardware interrupts (IRQs) for PC104 (ISA), PCI, and PCIe devices. The user must reserve IRQs in the BIOS CMOS configuration for use by legacy devices. The PCIe/PnP BIOS uses unreserved IRQs when allocating resources during the boot process. The following tables outline the EBC-C413 IRQ resource allocations.

IRQ Resources

IRQ	Device
IRQ0	18.2 Hz Heartbeat
IRQ1	Keyboard
IRQ2	Chained to Slave Controller (IRQ9)
IRQ3	COM2 *
IRQ4	COM1 *
IRQ5	COM3 *
IRQ6	COM4 *
IRQ7	LPT Port
IRQ8	Real Time Clock
IRQ9	FREE **
IRQ10	Digital I/O
IRQ11	PCI Interrupts
IRQ12	Mouse
IRQ13	Floating Point Processor
IRQ14	SATA Controller
IRQ15	SATA Controller ***

Some IRQs can be freed for other uses if the hardware features they are assigned to are not being used. To free an interrupt, use the CMOS setup screens to disable any unused board features or their IRQ assignments.

*These IRQ references are default settings that can be changed by the user in the CMOS Settings utility. Reference the Super I/O Control section under Intel.

**IRQ9 is commonly used by ACPI when enabled and may be unavailable (depending on operating system) for other uses.

***IRQ15 is currently unavailable under the Windows operating systems.

Interrupt Status Register - 29CH

Bit	Name
Bit 0	COM1
Bit 1	COM2
Bit 2	COM3
Bit 3	COM4
Bit 4	N/A
Bit 5	N/A
Bit 6	N/A
Bit 7	N/A
WINSYSTEMS does not provide software support for implementing the Interrupt Status Register to share interrupts. Some operating systems, such as Windows XP and Linux, have support for sharing serial port interrupts (see your specific operating system's documentation for any available examples). You need to implement the appropriate software to share interrupts for the other devices.	

NOTE A **1** is read for devices with an interrupt pending.

7.4 Digital I/O

The EBC-C413 uses the WINSYSTEMS exclusive application-specific integrated circuit (ASIC), the WS16C48. This device provides 48 lines of digital I/O. There are 16 unique registers within the WS16C48. The following table summarizes the registers.

I/O Address Offset	Page 0	Page 1	Page 2	Page 3
00h	Port 0 I/O	Port 0 I/O	Port 0 I/O	Port 0 I/O
01h	Port 1 I/O	Port 1 I/O	Port 1 I/O	Port 1 I/O
02h	Port 2 I/O	Port 2 I/O	Port 2 I/O	Port 2 I/O
03h	Port 3 I/O	Port 3 I/O	Port 3 I/O	Port 3 I/O
04h	Port 4 I/O	Port 4 I/O	Port 4 I/O	Port 4 I/O
05h	Port 5 I/O	Port 5 I/O	Port 5 I/O	Port 5 I/O
06h	Int_Pending	Int_Pending	Int_Pending	Int_Pending
07h	Page/Lock	Page/Lock	Page/Lock	Page/Lock
08h	Reserved	Pol_0	Enab_0	Int_ID0
09h	Reserved	Pol_1	Enab_1	Int_ID1
0Ah	Reserved	Pol_2	Enab_2	Int_ID2

The following sections provide details on each of the internal registers.

7.4.1 Ports 0 through 5 I/O

Each I/O bit in each of the six ports can be individually programmed for input or output. Writing a **0** to a bit position causes the corresponding

output pin to go to a high-impedance state (pulled high by external 10 KΩ resistors). This allows it to be used as an input. When used in the input mode, a read reflects the inverted state of the I/O pin, such that a high on the pin reads as a **0** in the register. Writing a **1** to a bit position causes that output pin to sink current (up to 12 mA), effectively pulling it low.

7.4.2 INT_PENDING

This read-only register reflects the combined state of the INT_ID0 through INT_ID2 registers. When any of the lower three bits are set, it indicates that an interrupt is pending on the I/O port corresponding to the bit positions that are set.

Reading this register allows an Interrupt Service Routine to quickly determine if any interrupts are pending and which I/O port has a pending interrupt.

7.4.3 PAGE/LOCK

This register serves two purposes. The upper two bits (D6 and D7) select the register page, and bits 0-5 allow for locking the I/O ports. Write a **1** to the I/O port position to prohibit further writes to the corresponding I/O port.

Page	D7	D6	D5-D0
Page 0	0	0	1/0
Page 1	0	1	1/0
Page 2	1	0	1/0
Page 3	1	1	1/0

7.4.4 POL0 through POL2

These registers are accessible when Page 1 is selected. They allow interrupt polarity selection on a port-by-port and bit-by-bit basis. Writing a **1** to a bit position selects the rising edge detection interrupts while writing a **0** to a bit position selects falling edge detection interrupts.

7.4.5 ENAB0 through ENAB2

These registers are accessible when Page 2 is selected. They allow for port-by-port and bit-by-bit enabling of the edge detection interrupts. When set to a **1**, the edge detection interrupt is enabled for the corresponding port and bit. When cleared to **0**, the bit's edge detection interrupt is disabled.

NOTE You can use these registers to individually clear a pending interrupt by disabling and re-enabling the pending interrupt.

7.4.6 INT_ID0 through INT_ID2

These registers are accessible when Page 3 is selected. They are used to identify currently pending edge interrupts. A bit when read as a **1** indicates that an edge of the polarity programmed into the corresponding polarity register has been recognized. A write to this register (value ignored) clears ALL of the pending interrupts in this register.

7.5 Watchdog Timer

The EBC-C413 features an advanced watchdog timer that can be used to guard against software lockups.

7.5.1 Enable and Set the Timer

The watchdog timer can be enabled in the BIOS Settings by entering a value for **Watchdog Timeout** on the **Advanced/SIO** > **FPGA G639** screen. Any non-zero value represents the number of minutes prior to reset during system boot. When the operating system is loaded, the watchdog can be disabled or reconfigured in the application software.

NOTE Use a longer reset interval if the watchdog is enabled and the operating system restarts.

The watchdog can also be enabled, disabled, or reset by writing the appropriate values to the configuration registers located at I/O addresses 565h and 566h. To enable the watchdog, write a timeout value other than zero to 566h. To disable the watchdog, write a zero (00h) to 566h. The watchdog timer is serviced by writing the desired timeout value to I/O port 566h. If the watchdog has not been serviced within the allotted time, the circuit resets the CPU.

The timeout value (specified by I/O address 566h) can be set from 1 to 255 and specified in seconds or minutes through I/O address 565h. Set bit 7 of address 565h to **1** for seconds, and clear to **0** for minutes. See the following table for examples.

Watchdog Timer Examples

Port Address	Port Bit 7 Value	Port Address	Value	Reset Interval
565h	x	566h	00h	DISABLED
	1		01h	1 second (minimum)
	1		03h	3 seconds
	1		1Eh	30 seconds
	1		3Ch	60 seconds
	0		01h	1 minute
	0		04h	4 minutes
	0		05h	5 minutes
	0		FFh	255 minutes (maximum)
To reset the watchdog timer, rewrite the timeout value to PORT 566h.				

7.6 Real-Time Clock/Calendar

A real-time clock (RTC) is used as the AT-compatible clock/calendar. The RTC supports a number of features, including periodic and alarm interrupt capabilities. In addition to the time and date keeping functions, the system configuration is kept in CMOS RAM contained within the clock section. A battery must be connected for the real-time clock to retain time and date during a power down.

7.7 Buzzer

The BIOS activates the buzzer during a POST failure. The beep code is specific to each type of error. Refer to “Power-on Self-Test (POST) Codes” on page 77 for details.

7.8 Activity Light

The system includes a programmable green activity LED on the board. To control it, write to I/O address 0x29Dh. Write a 0x01h to turn it on; write a 0x00h to turn it off. See “LED4 User LED” on page 54.

7.9 Clear CMOS Settings Jumper

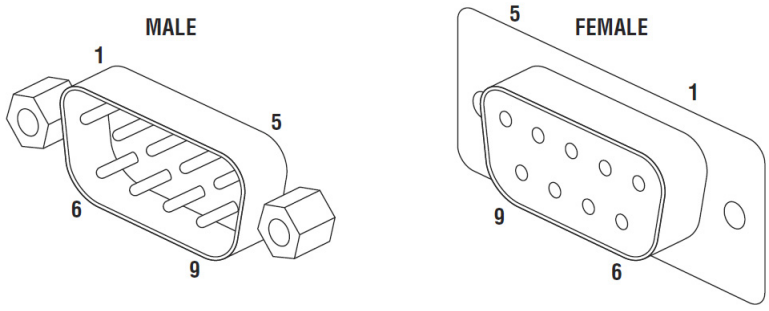
This jumper can be used to reset the BIOS CMOS settings to the factory default settings. This jumper ties a specific pin on the FPGA to ground. The BIOS reads this pin during system startup and if grounded, forces the settings reset. See “JPBAT - RTC Battery Enable” on page 53.

7.10 Serial Ports

The EBC-C413 provides four 16C550-compatible UARTs serial ports. Connect to COM1 and COM2 through the "MIO - PS/2 Keyboard, Serial 1/2, and LPT" on page 26 and COM3 and COM4 through the "COM3-4 - COM3 and COM4 Serial Ports" on page 25. Each port is configured as data terminal equipment (DTE). Both the send and receive registers of each port have a 16-byte FIFO.

The RS232 has a charge pump to generate the plus and minus voltages so that the EBC-C413 only requires +5 VDC to operate. An independent, software programmable baud-rate generator is selectable from 50 through 115.2 kbps. Individual modem handshake control signals are supported for all ports.

COM1, COM2, COM3, and COM4 (DB-9 Male and Female)



NOTE The following table contains standard pinouts of the EBC-C413 COM ports (COM1 through COM4) when connected to DB-9 connectors.

Pin	RS232	RS422	RS485
1	DCD	TX-	RX/TX-
2	RX	TX+	TX/RX+
3	TX	RX+	N/A
4	DTR	RX-	N/A
5	GND	GND	GND
6	DSR	N/A	N/A
7	RTS	N/A	N/A
8	CTR	N/A	N/A
9	RI	N/A	N/A

7.11 Power

The EBC-C413 draws power through the PWR connector (see "PWR - Power Connector" on page 23). The computer requires 5 VDC to operate. The +12 VDC and -12 VDC power inputs are passed through to the PC104 and PC104-Plus connectors, and LVDS backlight, but are not used to

power the main board. 5 VDC stand-by is only required to supply the power connector for ATX mode operation.

The EBC-C413 supports AT or ATX type power supplies. Jumper JP1 (see "PWR - Power Connector" on page 23) specifies the type of supply connected to the single board computer. AT power is a simple on/off power supply with no interaction with the single board computer. ATX mode sends a signal to the single board computer to control the power (default setting).

7.11.1 Fan

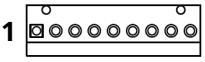
Optional fan power and control is provided through 12 V and control pins at FAN1 (see "FAN - Connector for Optional Fan" on page 39).

7.12 Connectors

7.12.1 PWR - Power Connector

Use this connection to supply power to the EBC-C413. If available, the +12 V and -12 V supply the PC104 and PC104-Plus connectors. When using an AT power supply, install jumper JP5VSB to short 5 V and 5 V Stand_by (see "JP5VSB - 5V Standby Power Select" on page 51).

Layout and Pin Reference



Pin	Name
1	VCC
2	GND
3	GND
4	+12 V
5	PC104Plus_3.3 V
6	GND
7	VCC
8	-12 V
9	PWRGOOD

Additional Information

This power connection is a 9-pin Molex 26-60-6092, 1 x 9, 0.1 inch locking header connector (or equivalent).

Matching connectors:

- Molex 09-50-8093
- Molex 06-58-0189

WINSYSTEMS cable CBL-236-G-2-1.5 simplifies this connection to the board.

7.12.2 ATXAUX - ATX/Auxiliary Power Connector

Connect to the ATX signals for the power button, 5 V standby, and power good through this connector.

The EBC-C413 supports either AT (standard power supply) or ATX type power supplies. Zero-load supplies are recommended. An AT power supply is a simple on/off supply with no interaction with the single board computer. Most embedded systems use this type of power supply and it is the default setting. The EBC-C413 power circuit detects an AT power supply if +5 VSB is not present at startup.

ATX type power supplies function with a “soft” on/off power button and a +5 VSB (standby). If an ATX-compatible power supply is connected, connect a power switch (momentary contact) between pin 2 (power button) and pin 1 (ground) of ATXAUX. The +5 VSB signal provides the standby voltage to the EBC-C413, but does not power any other features of the board. When the power button is pressed, the EBC-C413 pulls PSON (Power Supply On) low and the power supply turns on all voltages to the single board computer. When the power button is pressed again, the BIOS signals the event so ACPI-compliant operating systems can be shutdown before the power is turned off. In ATX mode, if the power button is held for 4 seconds, the power supply is forced off, regardless of ACPI. Because this is software driven, it is possible that a software lockup could prevent the power button from functioning properly. The EBC-C413 detects an ATX power supply, if +5 VSB is present at startup.

Layout and Pin Reference

Pin	Name	Description
1	GND	Ground
2	FRT_PWRON# (PWRBTN)	Power button
3	+5VSB	+5 V Standby Input
4	ATX_PSON# (PSON)	Momentary contact (normally open)

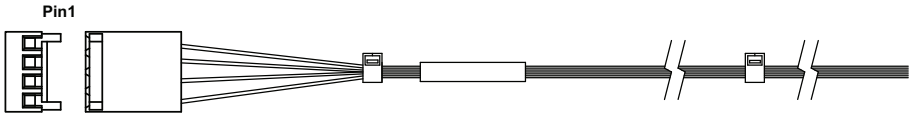
Additional Information

This connection is a Molex 22-11-2042 (or equivalent).

Matching connectors:

- Molex 22-01-2045 (housing)
- Molex 08-55-0110 or 08-55-0111 (crimp)

WINSYSTEMS cable CBL-PWR-600-14 simplifies this connection to the board.

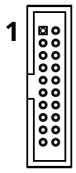


WIRE LIST	
J1	WIRE
1	W3 - RED
2	W2 - BROWN
3	W4 - ORANGE
4	W1 - BLACK

7.12.3 COM3-4 - COM3 and COM4 Serial Ports

Connect to COM3 and COM4 through this connector.

Layout and Pin Reference



Pin	Name	Pin	Name
1	COM3_DCD	2	COM3_DSR
3	COM3_RX	4	COM3_RTS
5	COM3_TX	6	COM3_CTS
5	COM3_DTR	8	COM3_RI
9	GND	10	N/C
11	COM4_DCD	12	COM4_DSR
13	COM4_RX	14	COM4_RTS
15	COM4_TX	16	COM4_CTS
17	COM4_DTR	18	COM4_RI
19	GND	20	N/C

Additional Information

This connection is a 20-pin Teka SVC210B3580135-0, 2 x 10, 0.1-inch box header connector (or equivalent).

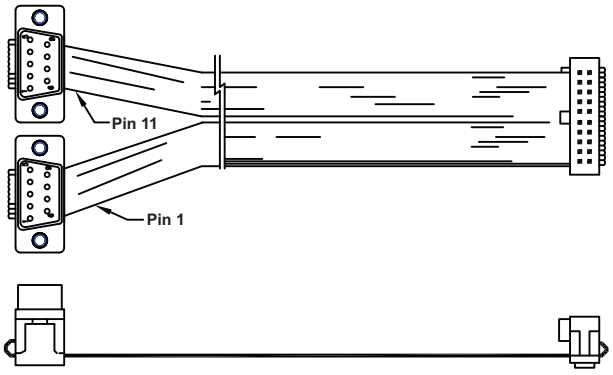
NOTE See “Serial Ports” on page 22 for more information on EBC-C413 serial ports.

NOTE Refer to “MIO - PS/2 Keyboard, Serial 1/2, and LPT” on page 26 for the connection to COM1 and COM2.

Matching connector:

- 20-pin IDC 0.1 inch TE1658622-4

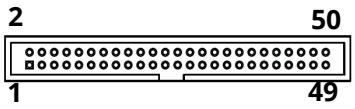
WINSYSTEMS cable CBL-173-G-1-1.0 simplifies this connection to the board.



7.12.4 MIO - PS/2 Keyboard, Serial 1/2, and LPT

Connect to the primary serial channels (COM1 and COM2), the printer port, and keyboard through this connector.

Layout and Pin Reference



Pin	Name	Pin	Name
1	COM1_DCD	2	COM1_DSR
3	COM1_RX	4	COM1_RTS
5	COM1_TX	6	COM1_CTS
7	COM1_DTR	8	COM1_RI
9	GND	10	COM2_DCD
11	COM2_DSR	12	COM2_RX
13	COM2_RTS	14	COM2_TX
15	COM2_CTS	16	COM2_DTR
17	COM2_RI	18	GND
19	LPT_STROBE	20	LPT_AUTOFD
21	LPT_PD0	22	LPT_ERROR
23	LPT_PD1	24	LPT_INIT
25	LPT_PD2	26	LPT_SLCTIN
27	LPT_PD3	28	LPT_GND
29	LPT_PD4	30	LPT_ GND
31	LPT_PD5	32	LPT_ GND
33	LPT_PD6	34	LPT_ GND
35	LPT_PD7	36	LPT_ GND
37	LPT_ACK	38	LPT_ GND
39	LPT_BUSY	40	LPT_ GND
41	LPT_PE	42	LPT_ GND
43	LPT_SLCT	44	KBMS_GND
45	KBMS_GND	46	KBMS_GND
47	KBDAT	48	KBCLK
49	+V5S_KBMS	50	+V5S_KBMS

Additional Information

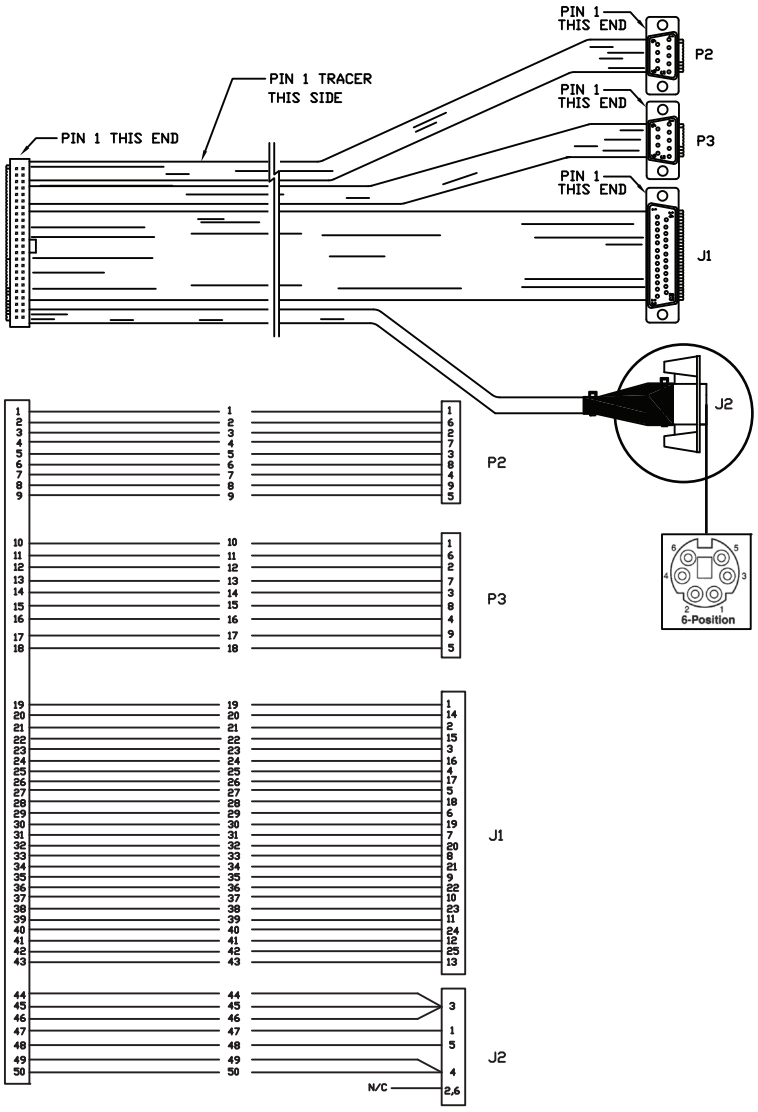
This connection is a 50-pin Teka SVC225B3580135-0, 2 x 25, 0.1-inch boxed header connector (or equivalent).

NOTE See “Serial Ports” on page 22 for more information on EBC-C413 serial ports.

Matching connector:

- 50-pin IDC 0.1 inch TE 1-1658622-2 or equivalent

WINSYSTEMS cable CBL-247-G-1-1.0 simplifies this connection to the board.



7.12.5 RST - Reset Connector

This connector resets the CPU and all peripherals. Connect it to a normally open monetary contact switch.

Layout and Pin Reference

	Pin	Name
2 1	1	RSTBTN#
	2	GND

WINSYSTEMS CBL-RST-402-18 simplifies this connection to the board.

7.12.6 MOUSE - PS/2 Mouse Connector

Connect mouse signals to this connection.

Layout and Pin Reference

1		
Pin	**Name**	**Description**
1	MCLK	Clock
2	KBMS_5V	Power
3	GND	Ground
4	N.C.	No Connection
5	MDAT	Data

Additional Information

This connection is a Molex 22-11-2052 (or equivalent).

Matching connectors:

- Molex 22-01-2057
- Molex 08-55-0102

WINSYSTEMS cable CBL-343-G-1-1.375 simplifies this connection to the board.

7.12.7 KBMS - Reserved

This connection is for factory use only.

7.12.8 USB1 - USB Connector for Ports 0-3

Connect to the USB signals provided at the USB1 connector.

NOTE The EBC-C413 provides eight USB2.0 ports with ESD suppression (four ports at USB1 and four at USB2).

Layout and Pin Reference

Pin	Name	Pin	Name
1	USB1_PWR	2	USB1_PWR
3	USBD0-	4	USBD1-
5	USBD0+	6	USBD1+
7	USB_GND	8	USB_GND
9	USB_GND	10	USB_GND
11	USB_GND	12	USB_GND
13	USB2_PWR	14	USB2_PWR
15	USBD2-	16	USBD3-
17	USBD2+	18	USBD3+
19	USB_GND	20	USB_GND

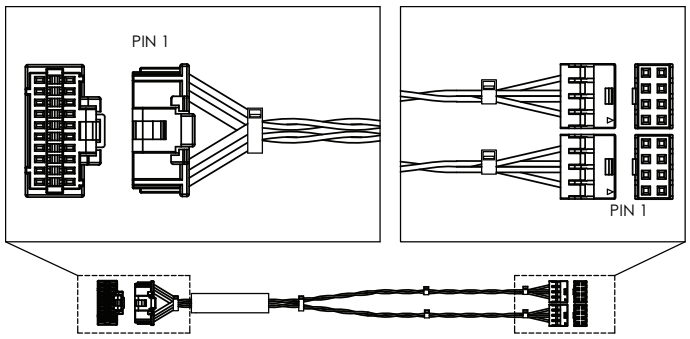
Additional Information

This connection is a Molex 501571-2007, 2 x 10, 1 mm pitch (Pico-Clasp™ or equivalent) right angle locking header connector (WS G650-2020-7HB).

Matching connector: Molex 501189-2010 housing with Molex 501193-2000 crimp pins. WINSYSTEMS cables simplify connections to the board:

- CBL-USB4-000-14: Pico-Clasp to unterminated
- CBL-USB4-001-12: Pico-Clasp to Pico-Clasp

- CBL-USB4-002-12: Pico-Clasp to 2 each, 2 x 4, 2 mm pitch housing (shown)



7.12.9 USB2 - USB Connector for Ports 4-7

Connect to the USB signals provided at the USB2 connector.

NOTE The EBC-C413 provides eight USB2.0 ports with ESD suppression (four ports at USB1 and four at USB2).

Layout and Pin Reference

Pin	Name	Pin	Name
1	+V5S_USB3	2	+V5S_USB3
3	USBD4-	4	USBD5-
5	USBD4+	6	USBD5+
7	GND	8	GND
9	GND	10	GND
11	GND	12	GND
13	+V5S_USB4	14	+V5S_USB4
15	USBD6-	16	USBD7-
17	USBD6+	18	USBD7+
19	GND	20	GND

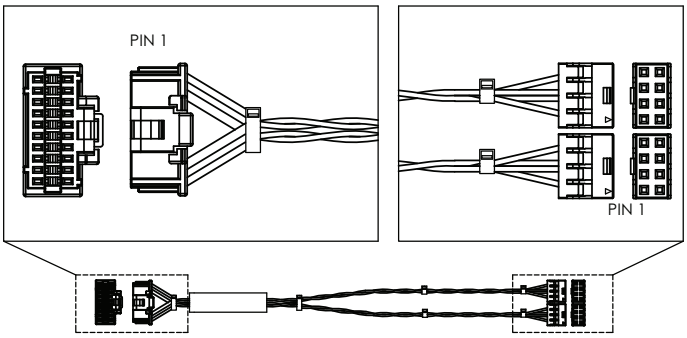
Additional Information

This connection is a Molex 501571-2007, 2 x 10, 1 mm pitch (Pico-Clasp™ or equivalent) right-angle locking header connector (WS G650-2020-7HB).

Matching connector: Molex 501189-2010 housing with Molex 501193-2000 crimp pins. WINSYSTEMS cables simplify connections to the board:

- CBL-USB4-000-14: Pico-Clasp to unterminated
- CBL-USB4-001-12: Pico-Clasp to Pico-Clasp

- CBL-USB4-002-12: Pico-Clasp to 2 each, 2 x 4, 2 mm pitch housing (shown)

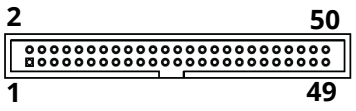


7.12.10 DIO1 - Digital I/O Connector with Event Sense

Connector DIO1 provides 24 bidirectional I/O lines. Each pin is capable of either rising or falling edge detect interrupt generation. These I/O lines can sink 12 mA each, but source current is limited to 5 mA when shorted to ground. +5 volts is provided on Pin 49 through JPDIO1(see “JPDIO1 - Power Enable (+5 VDC) to Pin 49 of DIO1” on page 51) to power external devices. The user must ensure that current does not exceed 1 A or damage may result.

NOTE The EBC-C413 provides 48 bidirectional I/O lines (24 lines at DIO1 and 24 lines at DIO2).

Layout and Pin Reference



Pin	Name	Pin	Name
1	Bit C7	2	GND
3	Bit C6	4	GND
5	Bit C5	6	GND
7	Bit C4	8	GND
9	Bit C3	10	GND
11	Bit C2	12	GND
13	Bit C1	14	GND
15	Bit C0	16	GND
17	Bit B7	18	GND
19	Bit B6	20	GND
21	Bit B5	22	GND
23	Bit B4	24	GND
25	Bit B3	26	GND
27	Bit B2	28	GND
29	Bit B1	30	GND
31	Bit B0	32	GND
33	Bit A7	34	GND
35	Bit A6	36	GND
37	Bit A5	38	GND
39	Bit A4	40	GND
41	Bit A3	42	GND
43	Bit A2	44	GND
45	Bit A1	46	GND
47	Bit A0	48	GND
49	VCC1	50	GND

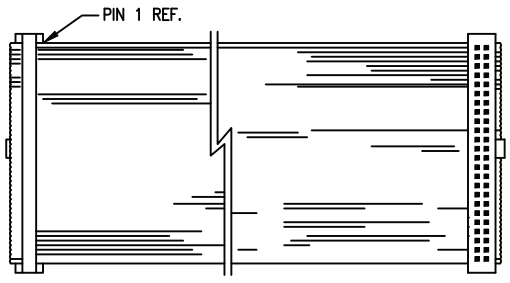
Additional Information

This connection is a Teka SVC225B3580135-0, 2 x 25, 0.1 inch box header (or equivalent).

Matching connector:

- 50-pin IDC 0.1 inch TE 1-1658622-2 or equivalent

WINSYSTEMS cable CBL-129-4 simplifies this connection to the board.

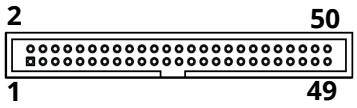


7.12.11 DIO2 - Digital I/O Connector

Connector DIO2 provides 24 bidirectional I/O lines. These I/O lines can sink 12 mA each, but source current is limited to 5 mA when shorted to ground. +5 volts is provided on Pin 49 through JPDIO1(see “JPDIO2 - Power Enable (+5 VDC) to Pin 49 of DIO2” on page 52) to power external devices. The user must ensure that current does not exceed 1 A or damage may result.

NOTE The EBC-C413 provides 48 bidirectional I/O lines (24 lines at DIO1 and 24 lines at DIO2).

Layout and Pin Reference



Pin	Name	Pin	Name
1	Bit F7	2	GND
3	Bit F6	4	GND
5	Bit F5	6	GND
7	Bit F4	8	GND
9	Bit F3	10	GND
11	Bit F2	12	GND
13	Bit F1	14	GND
15	Bit F0	16	GND
17	Bit E7	18	GND
19	Bit E6	20	GND
21	Bit E5	22	GND
23	Bit E4	24	GND
25	Bit E3	26	GND
27	Bit E2	28	GND
29	Bit E1	30	GND
31	Bit E0	32	GND
33	Bit D7	34	GND
35	Bit D6	36	GND
37	Bit D5	38	GND
39	Bit D4	40	GND
41	Bit D3	42	GND
43	Bit D2	44	GND
45	Bit D1	46	GND
47	Bit D0	48	GND
49	VCC2	50	GND

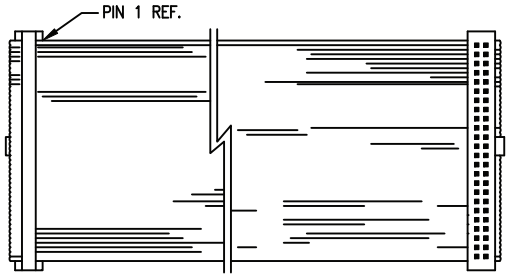
Additional Information

This connection is a Teka SVC225B3580135-0, 2 x 25, 0.1 inch box header (or equivalent).

Matching connector:

- 50-pin IDC 0.1 inch TE 1-1658622-2 or equivalent

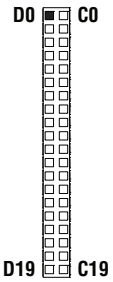
WINSYSTEMS cable CBL-129-4 simplifies this connection to the board.



7.12.12 PC104AB - PC104 8-bit Bus Connector
PC104CD - PC104 16-bit (Includes PC104AB) Bus Connector

The PC104 bus is electrically equivalent to the 16-bit ISA bus. Standard PC104 I/O cards can be populated on the EBC-C413 connectors, located at J2 and J3. The interface does not support hot-swap capability.

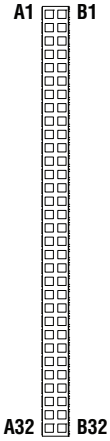
Layout and Pin Reference



Pin	Name	Pin	Name
D0	GND	C0	GND
D1	MEMCS16#	C1	SBHE#
D2	IOCS16#	C2	LA23
D3	IRQ10	C3	LA22
D4	IRQ11	C4	LA21
D5	IRQ12	C5	LA20
D6	IRQ15	C6	LA19
D7	IRQ14	C7	LA18
D8	DACK0#	C8	LA17
D9	DRQ0	C9	MEMR#
D10	DACK5#	C10	MEMW#
D11	DRQ5	C11	SD8
D12	DACK6#	C12	SB9
D13	DRQ6	C13	SD10
D14	DACK7#	C14	SD11
D15	DRQ7	C15	SD12
D16	+5V	C16	SD13
D17	MASTER#	C17	SD14
D18	GND	C18	SD15
D19	GND	C19	KEY1

= Active Low Signal

B10 and C19 are key locations. WINSYSTEMS uses key pins as connections to GND.



Pin	Name	Pin	Name
A1	IOCHK#	B1	GND
A2	SD7	B2	RESETDRV
A3	SD6	B3	+5V
A4	SD5	B4	IRQ
A5	SD4	B5	-5V
A6	SD3	B6	DRQ2
A7	SD2	B7	-12V
A8	SD1	B8	ENDXFR#
A9	SD0	B9	+12V
A10	IOCHRDY	B10	KEY
A11	AEN	B11	SMEMW#
A12	SA19	B12	SMEMR#
A13	SA18	B13	IOW#
A14	SA17	B14	IOR#
A15	SA16	B15	DACK3#
A16	SA15	B16	DRQ3
A17	SA14	B17	DACK1#
A18	SA13	B18	DRQ1
A19	SA12	B19	REFRESH#
A20	SA11	B20	SYSCLK
A21	SA10	B21	IRQ7
A22	SA9	B22	IRQ6
A23	SA8	B23	IRQ5
A24	SA7	B24	IRQ4
A25	SA6	B25	IRQ3
A26	SA5	B26	DACK2#
A27	SA4	B27	TC
A28	SA3	B28	BALE
A29	SA2	B29	+5V
A30	SA1	B30	OSC
A31	SA0	B31	GND
A32	GND	B32	GND

Additional Information

The standard EBC-C413 uses a stackable PC104 expansion connector. The standard EBC-C413 is not a “stack-through” type, meaning PC104 cards must “stackup.” A stack-through version may be special ordered (minimum quantities apply). The standard EBC-C413 connectors are:

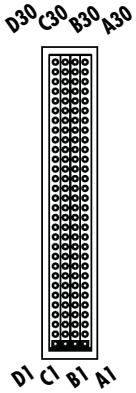
- J2 (40-pin) connector: SAMTEC type ESQ-120-12-G-D (non-stack-through)
- J3 (64-pin) connector: SAMTEC type ESQ-132-12-G-D (non-stack-through)

NOTE There are no keys in the connector and also no cut pins.

7.12.13 PC104P - PC104-Plus/PC104 Bus Connector

The PC104-Plus is electrically equivalent to the 33 MHz PCI bus. The interface is PC104-Plus version 2.0 compliant. The position of Jumper JP104P configures the 3.3 VDC to be sourced from on-board 3.3 V if not provided at the power input connector (see “JP104P - PCI-104 Power Source Select” on page 51). The interface does not support hot-swap capability.

Layout and Pin Reference

	Pin	A	B	C	D
	1	GND	RESERVED	+5V	AD00
	2	VI/O	AD02	AD01	+5V
	3	AD05	GND	AD04	AD03
	4	C/BE0#	AD007	GND	AD06
	5	GND	AD009	AD08	GND
	6	AD11	VI/O	AD10	M66EN
	7	AD14	AD13	GND	AD12
	8	+3.3V	C/BE1#	AD15	+3.3V
	9	SERR#	GND	RESERVED	PAR
	10	GND	PERR#	+3.3V	RESERVED
	11	STOP#	+3.3V	LOCK#	GND
	12	+3.3V	TRDY#	GND	DEVSEL#
	13	FRAME#	GND	IRDY#	+3.3V
	14	GND	AD16	+3.3V	C/BE2#
	15	AD18	+3.3V	AD17	GND
	16	AD21	AD20	GND	AD19
	17	+3.3V	AD23	AD22	+3.3V
	18	IDSEL0	GND	IDSEL1	IDSEL2
	19	AD24	C/BE3#	VI/O	IDSEL3
	20	GND	AD26	AD25	GND
	21	AD29	+5V	AD28	AD27
	22	+5V	AD30	GND	AD31
	23	REQ0#	GND	REQ1#	VI/O
	24	GND	REQ2#	+5V	GNT0#
	25	GNT1#	VI/O	GNT2#	GND
	26	+5V	CLK0	GND	CLK1
	27	CLK2	+5V	CLK3	GND
	28	GND	INTD#	+5V	RST#
	29	+12V	INTA#	INTB#	INTC#
	30	-12V	REQ3#	GNT3#	GND
	# = Active Low Signal				
	Shaded cells indicate power pins.				

Additional Information

This connection is a 120-pin, Teka 2MR430-BDWM-368-00 (non-stack-through, solder bearing), WS G650-0120-0BA (or equivalent).

NOTE There are no keys in the connector and also no cut pins.

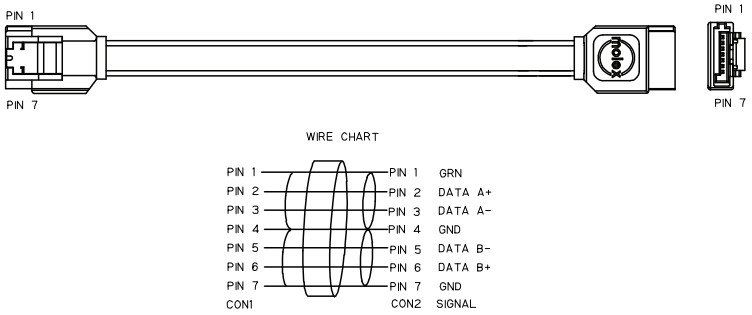
7.12.14 SATA1 - Serial ATA Connector

The EBC-C413 provides a SATA interface to support connection with a variety of SATA devices.

Layout and Pin Reference

	Pin	Name
	1	GND
	2	A+
	3	A-
	4	GND
	5	B-
	6	B+
	7	GND

The SATA interface is an industry standard 7-pin, right angle SATA connector Molex 47080-4005 (WS G650-7007-600). WINSYSTEMS cable CBL-SATA-701-20 simplifies connection to the board.



7.12.15 SATAPWR - Serial ATA Power Connector

The SATAPWR connector provides output power for the hard drive.

Layout and Pin Reference

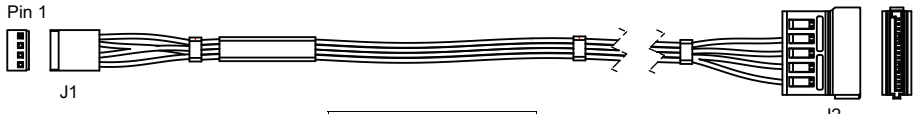
	Pin	Name
	1	+5 V
	2	GND (Ground)
	3	GND (Ground)
	4	+12 V

This connection is a Molex 22-11-2042 (or equivalent).

Matching connectors:

- Molex 22-01-2045 (housing)
- Molex 08-55-0110 or 08-55-0111 (crimp)

WINSYSTEMS cable CBL-PWR-117-12 simplifies this connection to the board.



WIRE LIST			
J1	J2	COLOR	SIGNAL
	1	NC	
1	5	YELLOW	+12 V
2	2	BLACK	GND
3	4	BLACK	GND
4	3	RED	+ 5 V

7.12.16 FAN - Connector for Optional Fan

The FAN connector provides output power and control for an optional fan.

Layout and Pin Reference

	Pin	Name
1	1	GND (Ground)
	2	12 V
	3	RPM
	4	CTRL

This connection is a Molex 22-11-2042 (or equivalent).

Matching connectors:

- Molex 22-01-2045 (housing)
- Molex 08-55-0110 or 08-55-0111 (crimp)

The FAN connector is pin compatible with Standard PC chassis 3-pin or 4-pin fans.

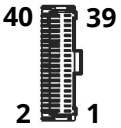
7.12.17 LVDS - LVDS Display Output Connector

The EBC-C413 supports low-voltage differential signaling (LVDS) for flat-panel displays with resolutions up to 1920 x 1200 at 24 bpp.

NOTE The EBC-C413 has one VGA, one Mini DisplayPort and one Low-Voltage Differential Signaling (LVDS) interface. Only two of the three outputs may be active simultaneously.

The power (SWVDD) portion of this connector can be configured (see “JPLCDP - LCD Panel Power Configuration” on page 53). Connect to the LVDS interface through the LVDS connector.

Layout and Pin Reference



Pin	Name	Pin	Name
1	LVDS1_VDD	2	GND
3	LVDS_A0-	4	LVDS_A0+
5	LVDS_A1-	6	LVDS_A1+
7	LVDS1_VDD	8	GND
9	LVDS_A2-	10	LVDS_A2+
11	LVDS_A3-	12	LVDS_A3+
13	LVDS1_VDD	14	GND
15	LVDS_A_CLK-	16	LVDS_A_CLK+
17	LVDS_I2C_CLK	18	GND
19	LVDS_I2C_DAT	20	GND
21	LVDS1_VDD	22	GND
23	LVDS_B0-	24	LVDS_B0+
25	LVDS_B1-	26	LVDS_B1+
27	LVDS1_VDD	28	GND
29	LVDS_B2-	30	LVDS_B2+
31	LVDS_B3-	32	LVDS_B3+
33	LVDS1_VDD	34	GND
35	LVDS_B_CLK	36	LVDS_B_CLK+
37	NC	38	NC
39	NC	40	NC

Additional Information

This connection is a Molex 501571-4007, 2 x 20, 1 mm box header (or equivalent).

Matching connectors:

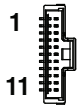
- Molex 501189-4010 (housing)
- Molex 501193-2000 (crimp)

WINSYSTEMS LVDS cables are panel specific. Contact an Application Engineer through technical support for details (see the “Introduction” on page 6 for details).

7.12.18 BKLT - Backlight Power and Control Connector

The BLKLT connector provides PWM backlight support for the LVDS display.

Layout and Pin Reference



Pin	Name	Description
1	+5VDC	INV_VDD5
2	LBKLT_EN-	Low Active Backlight Enable
3	LBKLT_EN+	High Active Backlight Enable
4	GND	Ground
5	+12VDC	INV_VDD12
6	PWM	Backlight Control
7	NC	No Connection
8	NC	No Connection
9	NC	No Connection
10	LCTLB_DATA	Data
11	LCTLA_CLK	Clock

Additional Information

This connection is a Molex 501331-1107, 1 x 11, 1 mm vertical box header (or equivalent).

Matching connectors:

- Molex 501330-1100 (housing)
- Molex 501334-0000 (crimp)

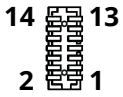
WINSYSTEMS backlight cables are panel specific. Contact an Application Engineer through technical support for details (see the “Introduction” on page 6 for details).

7.12.19 VGA - Analog VGA Display Connector

The EBC-C413 supports analog VGA.

NOTE The EBC-C413 has one VGA, one Mini DisplayPort and one Low-Voltage Differential Signaling (LVDS) interface. Only two of the three outputs may be active simultaneously.

Layout and Pin Reference



Pin	Name	Pin	Name
1	VGA_RED	2	GND
3	VGA_GREEN	4	GND
5	VGA_BLUE	6	GND
7	VGA_HSYNC	8	GND
9	VGA_VSYNC	10	GND
11	DDC_SDA	12	GND
13	DDC_SCL	14	VCC

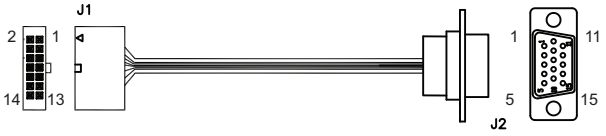
Additional Information

This connection is a Molex 87832 series, 2 x 7, 1 mm box header (or equivalent).

Matching connectors:

- Molex 51110-1451
- Molex 50394-8051

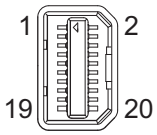
WINSYSTEMS cable CBL-234-G-1-1-375 simplifies this connection to the board.



7.12.20 DP - Mini DisplayPort Connector

NOTE The EBC-C413 has one VGA, one Mini DisplayPort and one Low-Voltage Differential Signaling (LVDS) interface. Only two of the three outputs may be active simultaneously.

Layout and Pin Reference

	Pin	Name	Description	Pin	Name	Description
	1	GND	Ground	2	Hot Plug Detect	Hot Plug Detect
	3	ML_Lane 0 (p)	Lane 0 (positive)	4	CONFIG1	CONFIG1
	5	ML_Lane 0 (n)	Lane 0 (negative)	6	CONFIG2	CONFIG2
	7	GND	Ground	8	GND	Ground
	9	ML_Lane 1 (p)	Lane 1 (positive)	10	ML_Lane 3 (p)	Lane 3 (positive)
	11	ML_Lane 1 (n)	Lane 1 (negative)	12	ML_Lane 3 (n)	Lane 3 (negative)
	13	GND	Ground	14	GND	Ground
	15	ML_Lane 2 (p)	Lane 2 (positive)	16	AUX_CH (p)	Auxiliary Channel (positive)
	17	ML_Lane 2 (n)	Lane 2 (negative)	18	AUX_CH (n)	Auxiliary Channel (negative)
	19	GND	Ground	20	DP_PWR	Power for connector

7.12.21 BAT - External Battery Connector

An optional external battery, connected to BAT, supplies the EBC-C413 board with standby power for the real-time clock and CMOS setup RAM. Extended temperature lithium batteries are available from WINSYSTEMS, part numbers:

- BAT-LTC-E-36-16-1
- BAT-LTC-E-36-27-1

A power supervisory circuit contains the voltage sensing circuit and an internal power switch to route the battery or standby voltage to the circuits selected for backup. The battery automatically switches on when the VCC of the systems drops below the battery voltage and off when VCC returns to normal.

Layout and Pin Reference

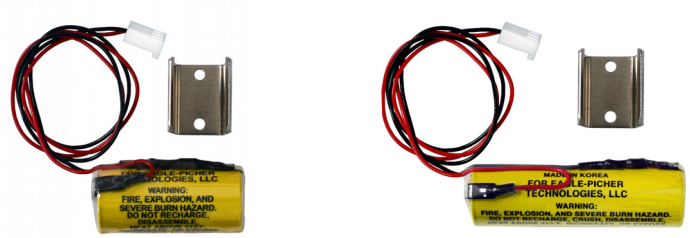
	Pin	Name	Description
	1	NC	No Connect
	2	VBAT (BAT+)	Battery Voltage Input
	3	GND	Ground

Additional Information

This connection uses Molex part number 22-11-2032.

WINSYSTEMS battery BAT-LTC-E-36-16-1 and BAT-LTC-E-36-27-1 (connected to J3) simplify these connections to the board.

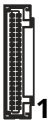
ꓕT-LTC-E-36-16-1 BAT-LTC-E-36-27-1



7.12.22 AUDIO - HD Audio Connector

Connect to the high-definition audio interface through this connector.

Layout and Pin Reference

	Pin	Name	Pin	Name
	1	OUT_R	2	MIC1_R
	3	OUT_L	4	MIC1_L
	5	AUDIO_ GND	6	AUDIO_GND
	7	SUR_R	8	MIC2_R
	9	SUR_L	10	MIC2_L
	11	AUDIO_ GND	12	AUDIO_GND
	13	CENTER	14	LINE_R
	15	LFE	16	LINE_L
	17	AUDIO_ GND	18	AUDIO_GND
	19	SIDE_R	20	CD_R
	21	SIDE_L	22	CD_L
	23	AUDIO_ GND	24	CD_GND
	25	HEAD_R	26	AUDIO_GND
	27	HEAD_L	28	AUDIO_GND
	29	AUDIO_ GND	30	AUDIO_GND

Additional Information

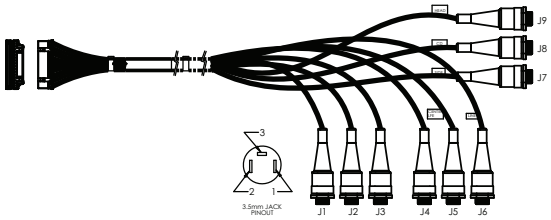
This connection is a Molex 502046-3070 (Duo-Clasp™), 2 x 15, 1.25 mm box header (or equivalent).

Matching connectors:

- Molex 503110-3000
- Molex 501930-1100

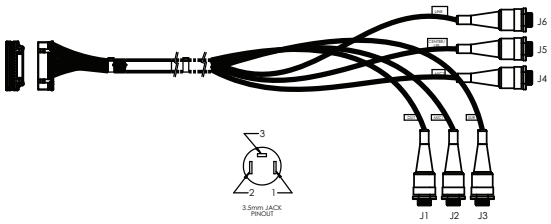
WINSYSTEMS has four cables for this connector:

- CBL-AUDIO7-102-12

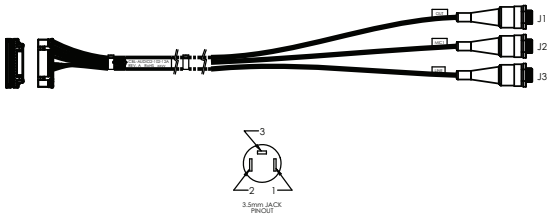


- CBL-AUDIO7-100-14

- CBL-AUDIO5-102-12



- CBL-AUDIO2-102-12



7.12.23 LAN1/LAN2 - Ethernet LAN Connectors

The EBC-C413 uses two Intel i210 Gb/s Ethernet controller that includes ESD suppression.

Additional Information

The connection is a RJ45 with activity LEDs.

Matching connector:

- Ethernet standard CAT5 (or better) cables

7.12.24 MC1 - MiniCard Connector with PCI-Express and USB

Connect to the MC1 MiniCard socket that supports a variety of peripherals available in this format.

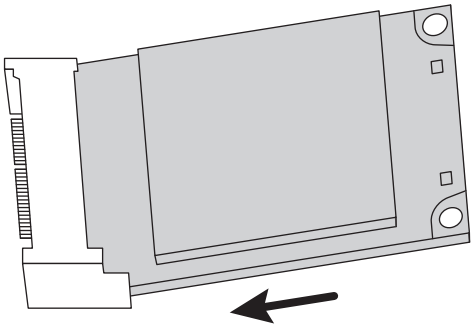
Pin	Name	Pin	Name
1	WAKE#	2	3.3Vaux
3	COEX1	4	GND
5	COEX2	6	1.5V
7	CLKREQ#	8	UIM_PWR
9	GND	10	UIM_DATA
11	REFCLK-	12	UIM_CLK
13	REFCLK+	14	UIM_RST
15	GND	16	UIM_VPP
17	RSVD(UIM_C8)	18	GND
19	RSVD(UIM_C4)	20	W_DISABLE#
21	GND	22	PERST#
23	PETn0	24	3.3Vaux
25	PETp0	26	GND
27	GND	28	1.5V
29	GND	30	SMB_CLK
31	PETn0	32	SMB_DATA
33	PETp0	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	3.3Vaux	40	GND
41	3.3Vaux	42	LED_WWAN#
43	GND	44	LED_WLAN#
45	RSVD	46	LED_WPAN#
47	RSVD	48	1.5V
49	RSVD	50	GND
51	RSVD	52	3.3Vaux
Shaded cells indicate unconnected signals.			

Additional Information

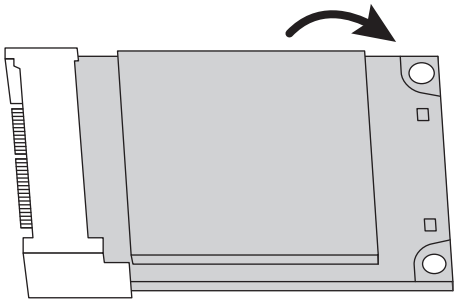
This connection is a Tyco 1775838-2 (or equivalent).

To install a MiniCard into the MC1 socket:

1. Insert the MiniCard/mSATA.



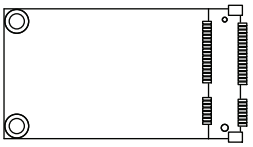
2. Push the free end of the card toward the circuit board, and then secure it with two 2 mm screws (WINSYSTEMS P/N G527-0000-400).



7.12.25 MC2 - MiniCard/mSATA Connector with PCI-Express, USB, and SATA

The EBC-C413 provides a second MiniCard socket (also see “MC1 - MiniCard Connector with PCI-Express and USB” on page 46) that supports a variety of peripherals available in this format. The socket alternatively supports an mSATA device in this socket. A sense circuit identifies the type of device present in the socket and auto-switches to handle either type.

Layout and Pin Reference



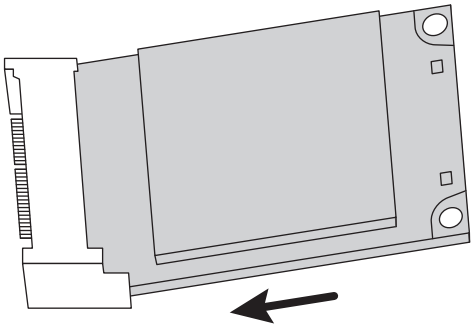
Pin	Name	Pin	Name
1	WAKE#	2	+3.3 Vaux
3	RESERVED	4	GND
5	RESERVED	6	+1.5 V
7	CLKREQ#	8	UIM_PWR
9	GND	10	UIM_DATA
11	REFCLK-	12	UIM_CLK
13	REFCLK+	14	UIM_RST
15	GND	16	UIM_VPP
17	RSVD(UIM_C)	18	GND
19	RSVD(UIM_C)	20	W_DISABLE#
21	GND	22	PERST#
23	PERn0	24	3.3 Vaux
25	PERp0	26	GND
27	GND	28	1.5V
29	GND	30	SMB_CLK
31	PERn0	32	SMB_DATA
33	PERp0	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	3.3 Vaux	40	GND
41	3.3 Vaux	42	LED_WWAN#
43	GND	44	LED_WLAN#
45	RSVD	46	LED_WPAN#
47	RSVD	48	1.5 V
49	RSVD	50	GND
51	mSATA Detect	52	+3.3 Vaux
Shaded cells indicate unconnected signals.			

Additional Information

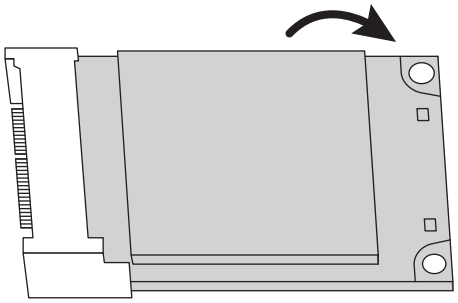
This connection is a Tyco 1775838-2 (or equivalent).

To install a MiniCard/mSATA into the MC2 socket:

1. Insert the MiniCard.



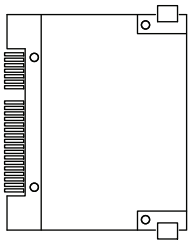
2. Push the free end of the card toward the circuit board, and then secure it with two 2 mm screws (WINSYSTEMS P/N: G527-0000-400).



7.12.26 CF1 - CFast SSD Connector

CFast is a small form factor SATA SSD standard that encompasses CFast data storage cards.

Layout and Pin Reference



Number	Segment	Name	Type	Description	Sequence
S1	SATA	SGND	Signal GND	Ground for signal integrity	1
S2	SATA	A+	SATA Differential	Signal Pair A	2
S3	SATA	A-	SATA Differential	Signal Pair A	2
S4	SATA	SGND	Signal GND	Ground for signal integrity	1
S5	SATA	B-	SATA Differential	Signal Pair B	2
S6	SATA	B+	SATA Differential	Signal Pair B	2
S7	SATA	SGND	Signal GND	Ground for signal integrity	1
KEY					
KEY					
PC1	PWR/CTL	CDI	Input	Card Detect IN	3
PC2	PWR/CTL	PGND	Device GND	Device Ground	1
PC3	PWR/CTL	DEVSLP	DEVSLP Card Input	DevSleep Power State Enable	2
PC4	PWR/CTL	Not applicable		Reserved	2
PC5	PWR/CTL	Not applicable		Reserved	2
PC6	PWR/CTL	Not applicable		Reserved	2
PC7	PWR/CTL	PGND	Device GND		1
PC8	PWR/CTL	LED1	LED Output	LED Output	2
PC9	PWR/CTL	LED2	LED Output	LED Output	2
PC10	PWR/CTL	Not applicable		Reserved	2
PC11	PWR/CTL	Not applicable		Reserved	2
PC12	PWR/CTL	IFDet	GND	Card output, connect to PGND on card	2
PC13	PWR/CTL	PWR	3.3 V	Device Power (3.3 V)	2
PC14	PWR/CTL	PWR	3.3 V	Device Power (3.3 V)	2
PC15	PWR/CTL	PGND	Device GND	Device Ground	1
PC16	PWR/CTL	PGND	Device GND	Device Ground	1
PC17	PWR/CTL	CDO	Output	Card Detect Out	3

Additional Information

This connection is a 3M N7G24-A0B2EB-10-3WF (or equivalent).

7.12.27 204-pin SODIMM Socket for System Memory

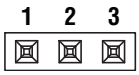
The EBC-C413 supports up to eight GB DDR3L SODIMM system memory through this one on-board socket.

7.13 Jumpers

Jumper PN SAMTEC 2SN-BK-G applies to all jumpers. These are available in a ten piece kit from WINSYSTEMS (PN KIT-JMP-G-200).

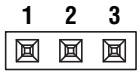
7.13.1 JP104P - PCI-104 Power Source Select

Purpose: Configures power source for the PC104-Plus (see “PC104P - PC104-Plus/PC104 Bus Connector” on page 36).

	Jumper	PC104-Plus Power Setting
	1-2	From Pin 5 of Power Connector (default)
	2-3	From onboard +3.3 V

7.13.2 JP5VSB - 5V Standby Power Select

Purpose: Shorts 5 V and 5V_SB. Connect pins 1-2 when using AT power supply; connect pins 2-3 or Open when using ATX power supply.

	Jumper	5 V Standby Power Setting
	1-2	Shorts +5 V IN to +5 V SB (default)
	2-3	+5 V IN to N.C. (no connection)

7.13.3 JPDIO1 - Power Enable (+5 VDC) to Pin 49 of DIO1

Purpose: When present, this jumper connect Pins 1-2 and applies power (+5 VDC, VCC1) to pin 49 of DIO1. With jumper removed, no voltage is applied to Pin 49.

	Jumper	5 V Standby Power Setting
	1-2	+5 VDC applied (default)
	NC	No voltage applied (pin 49 open)

7.13.4 JPDIO2 - Power Enable (+5 VDC) to Pin 49 of DIO2

Purpose: When present, this jumper connects Pins 1-2 and applies power (+5 VDC, VCC2) to pin 49 of DIO2. With jumper removed, no voltage is applied to Pin 49.

	Jumper	Voltage to pin 49 of DIO2
	1-2	+5 VDC applied (Default)
	NC	No voltage applied (pin 49 open)

7.13.5 JPSATA - Serial ATA Device Select

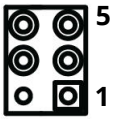
Purpose: Configures SATA channel for use with CFast (CF1) or SATA (SATA1) connector.

	Jumper	Serial ATA Device Selection
	Open	Forces SATA1 as active connector.
	1-2	Forces CFast to be active connector.
	2-3	Auto detects presence of CFast and claims channel for CFast connector.

7.13.6 JPATX - AT/ATX Power Supply Select

Purpose: Specifies the style of power supply connected. The presence of a jumper at JPATX specifies the style of supply connected to the single board computer (see “ATXAUX - ATX/Auxiliary Power Connector” on page 24). AT Power is a simple on/off power supply that has no interaction with the single board computer. Most embedded systems use this type of power supply (default setting).

Jumper Pin Reference

	Jumper	AT / ATX Mode Select
	4-6	ATX Mode (Default)
	2-4	AT Mode

7.13.7 JPMC1 - MC1 Wireless LAN Enable

Purpose: Enables wireless LAN (turns on) for MC1.

	Jumper	MC1 Wireless LAN Setting
	1-2	Disable wireless LAN (MC1)
	2-3	Enable wireless LAN (MC1)

7.13.8 JPMC2 - MC2 Wireless LAN Enable

Purpose: Enables wireless LAN (turns on) for MC2.

	Jumper	MC2 Wireless LAN Setting
	1-2	Disable wireless LAN (MC2)
	2-3	Enable wireless LAN (MC2)

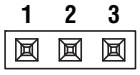
7.13.9 JPMSATA - MC2 mSATA/MiniCard Select

Purpose: Configures MC2 for use with mSATA or MiniCard.

	Jumper	MC2 mSATA Setting
	1-2	Configures MC2 for MiniCard
	2-3	Configures MC2 for mSATA

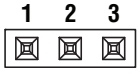
7.13.10 JPLCDP - LCD Panel Power Configuration

Purpose: JPLCDP controls the power voltage for LVDS panels.

	Jumper	LVDS setting
	1-2	+5 Volt panel
	2-3	+3.3 Volt panels
	Open	No power provided to panel

7.13.11 JPBAT - RTC Battery Enable

Purpose: Enable Real Time Clock (RTC) battery backup.

	Jumper	RTC Battery Enable Setting
	1-2	Normal operation
	2-3	Resets RTC time, date, and battery backed RAM

7.14 LED Indicators

The EBC-C413 contains four LEDs covered by the heat spreader.

SATA Activity (LED1)

LED1	Description
LED1	Indicates SATA activity

Power and Standby Status (LED2 and LED3)

LED2	LED3	Description
Off	Off	No Power
Off	Green	In Standby
Blue	Off	Normal Operation
Blue	Green	Abnormal Operation

7.14.1 LED4 User LED

The user light emitting diode (LED4) can be used for any application-specific purpose. In software applications, turn this LED on by writing a **1** to I/O port 29DH and turn it off by writing a **0** to 29DH.

8. BIOS

8.1 General Information

The EBC-C413 includes a BIOS from InsideH2O to ensure full compatibility with PC operating systems and software. The basic system configuration is stored in battery backed CMOS RAM within the clock/calendar. As an alternative, the CMOS configuration may be stored in EEPROM for operation without a battery. For more information of CMOS configuration, see the “BIOS” on page 54. Access to this setup information is through the Setup Utility in the BIOS.

8.2 Entering Setup

To enter setup, power up the computer and press **Del** (the delete key) when the splash screen is displayed. It may take a few seconds before the main setup menu screen is displayed.

8.3 Navigation of the Menus

Use the Up and Down arrow keys to move among the selections. To enter a sub-menu or to see a list of choices, press **Enter** when the selection is highlighted. See “BIOS Screens” on page 55 for available options.

8.4 BIOS Splash Screen

Custom BIOS splash screens can be made available for OEM customers. Contact one of our Application Engineers for details.

8.5 BIOS Screens

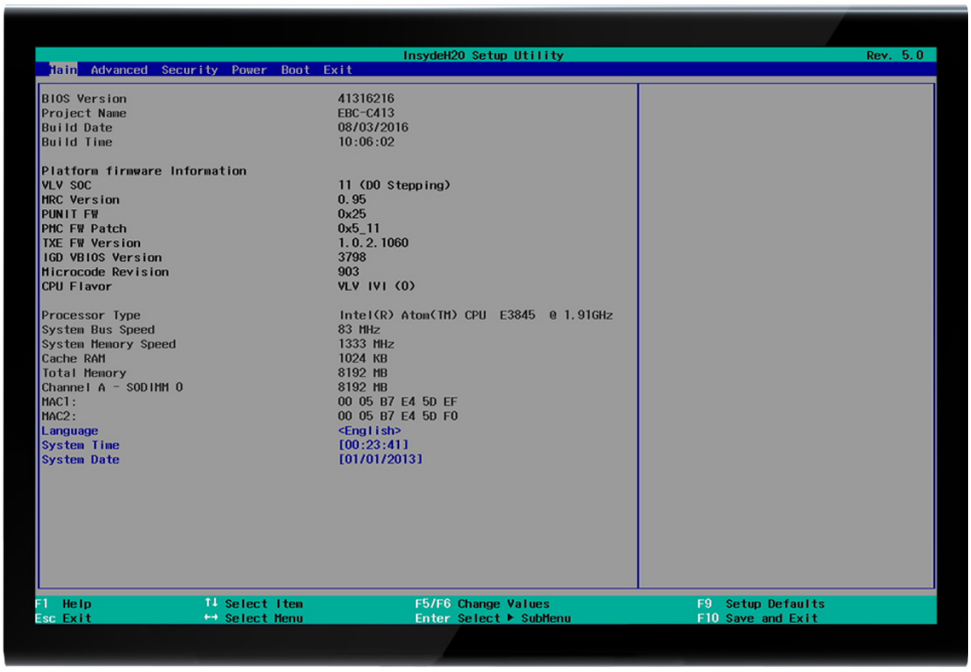
The following BIOS screens contain the options and sample settings for the EBC-C413. Your actual configuration may differ from the screens shown here.

NOTE Use care when modifying BIOS settings.

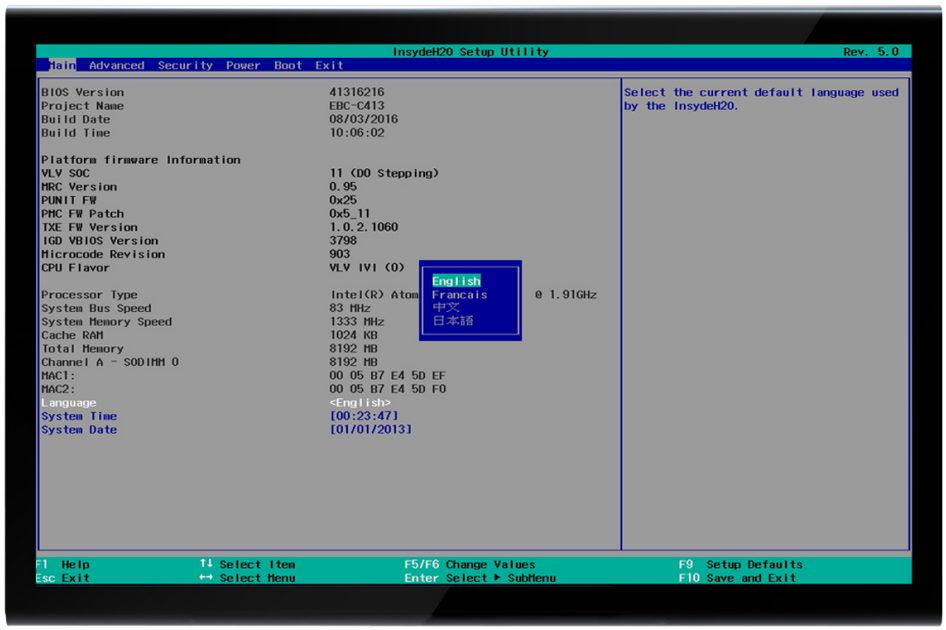
Main

Use this screen to view general configuration information about the system, and to configure the following components:

- Language
- System Time
- System Date

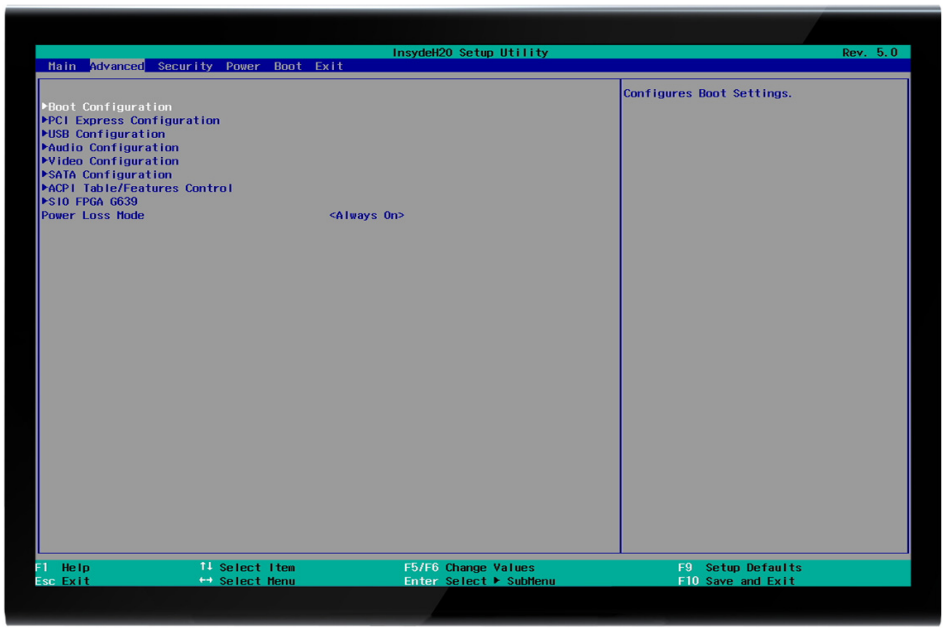


Language

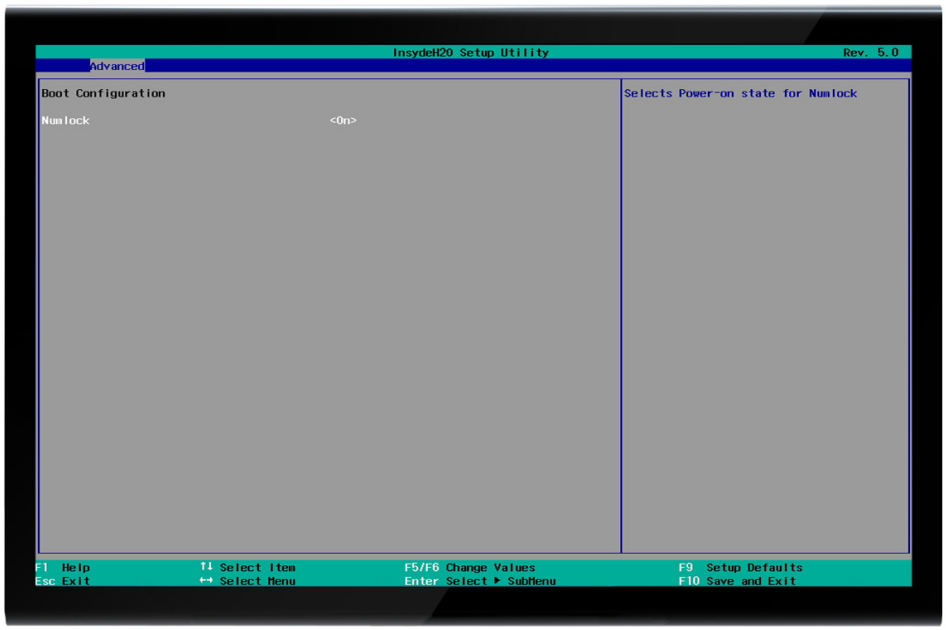


Advanced

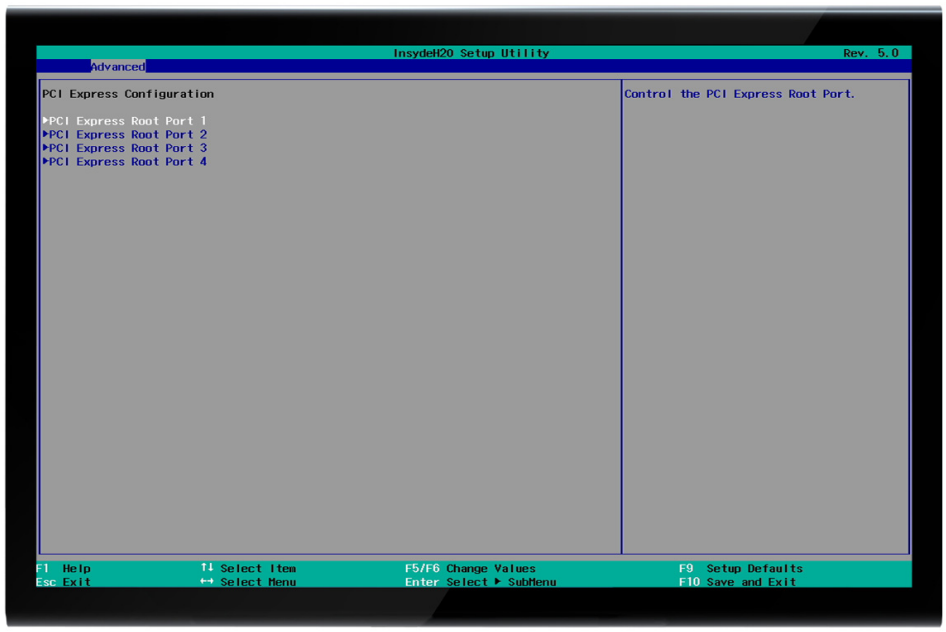
Access the configuration screens for Boot, PCI Express, USB, Audio, Video, SATA, ACPI, S10 FGPA G639, and Power Loss mode from the Advanced screen.



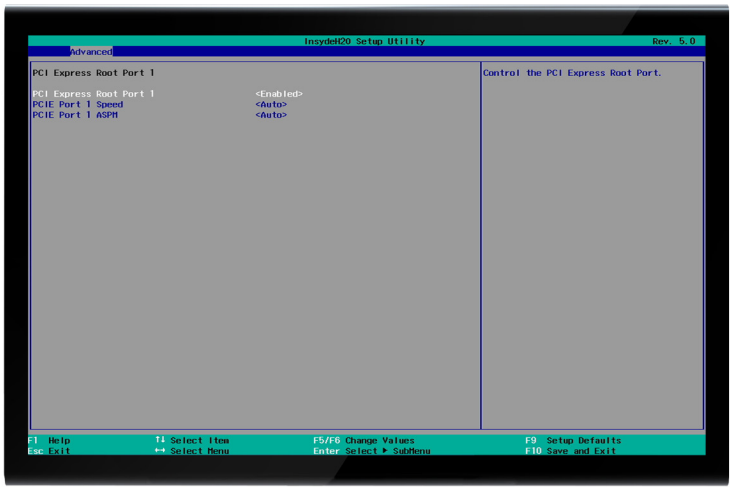
Boot Configuration



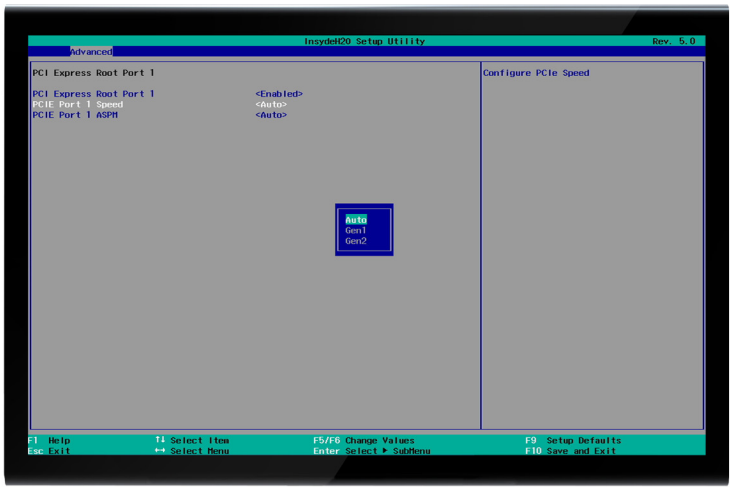
PCI Express Configuration



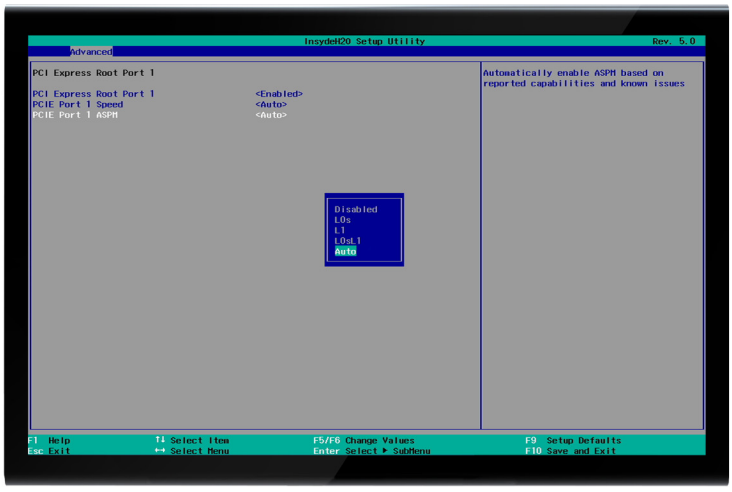
PCI Express Root Port Example (Port 1 shown)



PCI Port Speed Example (Port 1 shown)



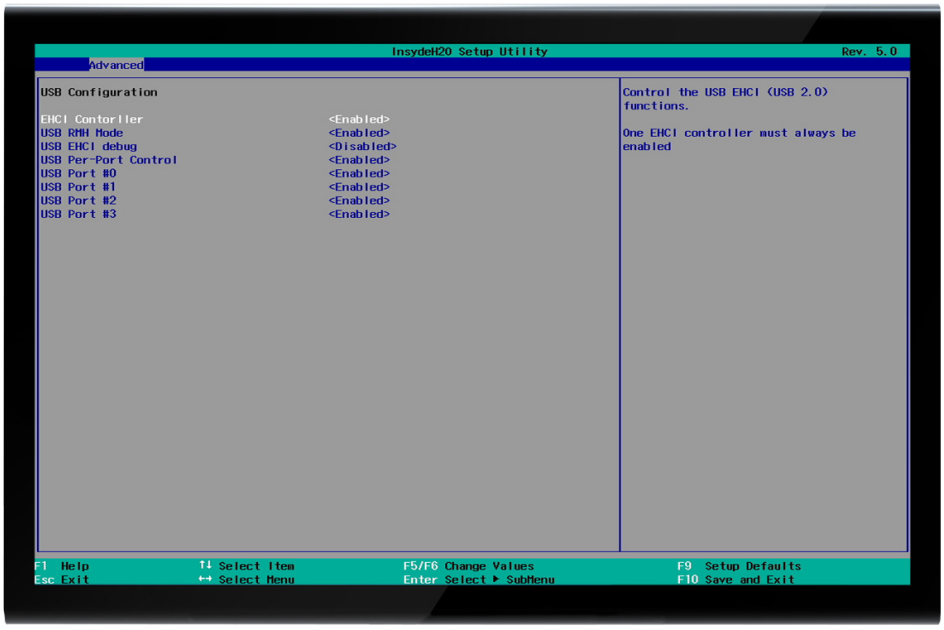
PCI Port ASPM Example (Port 1 shown)



USB Configuration

Use this screen to enable or disable the following components:

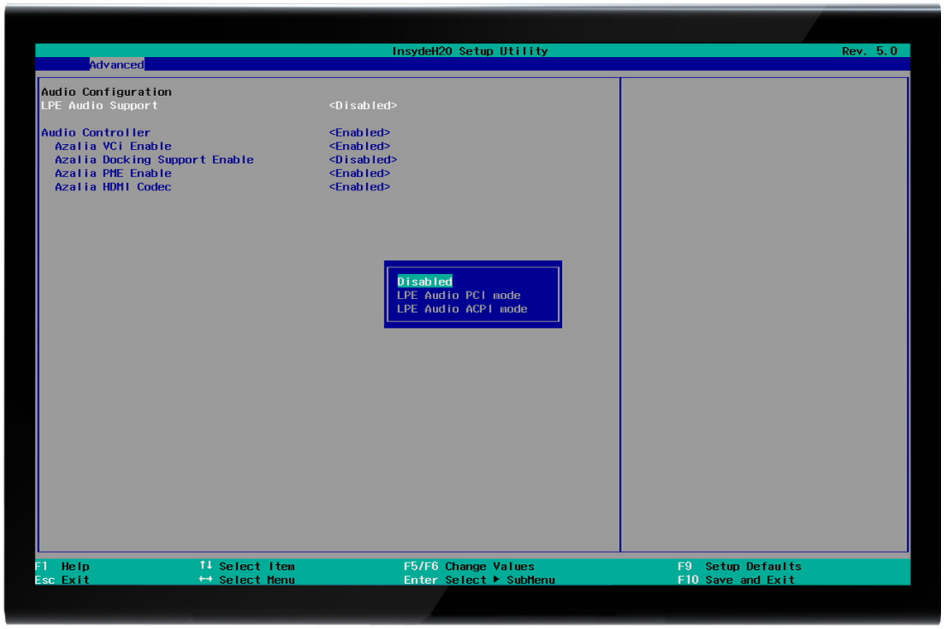
- EHCI Controller
- USB RMH Mode
- USB EHCI Debug
- USB Per-Port Control
- USB Port #0
- USB Port #1
- USB Port #2
- USB Port #3



Audio Configuration

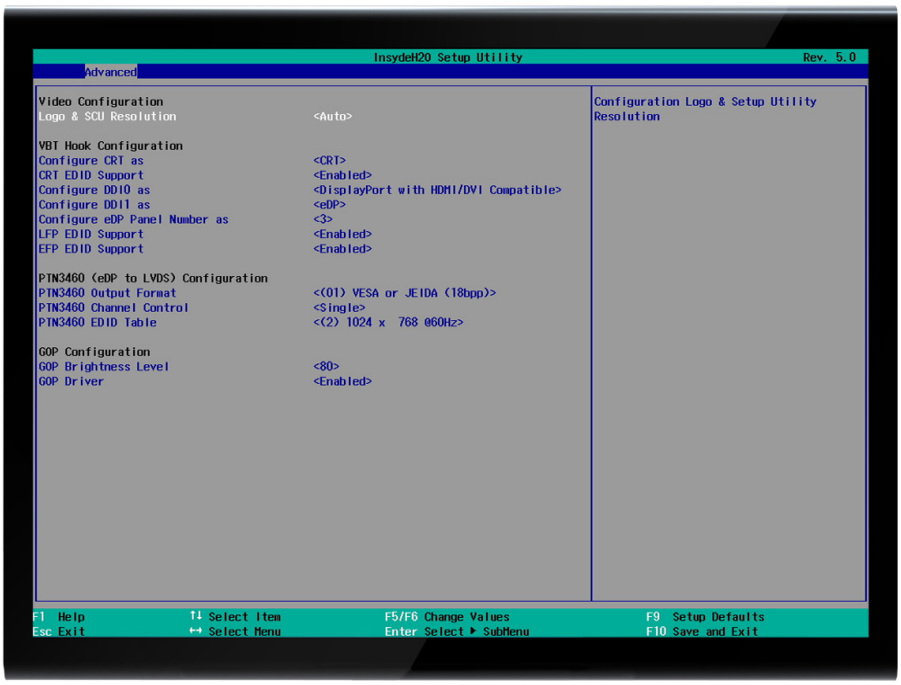
In addition to enabling and configuring LPE Audio Support, use this screen to enable or disable the following components:

- Audio Controller
- Azalia VCi Enable
- Azalia Docking Support Enable
- Azalia PME Enable
- Azalia HDMI Codec



Video Configuration

Use this screen to configure the video components listed below.



Video Configuration

- **Logo and SCU Resolution:** AUTO, 640 x 480, 800 x 600, 1024 x 768

VBT Hook Configuration

- **Configure CRT as:** Default, CRT, No Device
- **CRT EDID Support:** Enable, Disable
- **Configure DD10 as:** Default, eDP, DisplayPort, HDMI/DVI, DisplayPort with HDMI/DVI Compatible, No Device
- **Configure DD11 as:** Default, eDP, DisplayPort, HDMI/DVI, DisplayPort with HDMI/DVI Compatible, No Device
- **Configure eDP Panel Number as:** 1 through 16
- **LFP EDID Support:** Enable, Disable
- **EFP EDID Support:** Enable, Disable

PIN3460 (eDP to LVDS) Configuration

- **PIN3460 Output Format:** (00) VESA (24 bpp), (01) VESA or JEIDA (18 bpp), (10) JEIDA (24 bpp)
- **PIN3460 Channel Control:** Single, Dual
- **PIN3460 EDID Table**

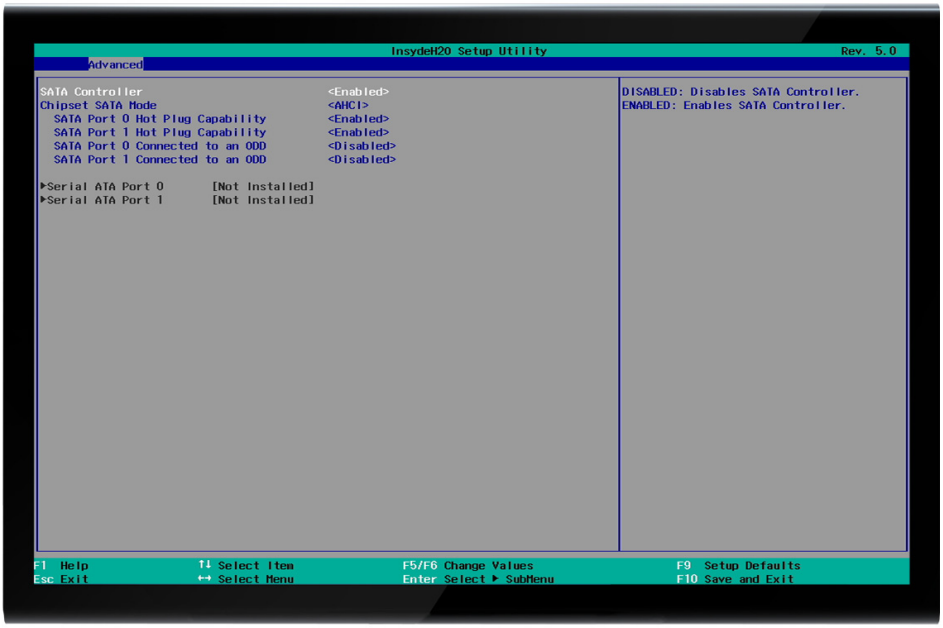
(0)	640 x 480	@ 60 Hz
(1)	800 x 600	@ 60 Hz
(2)	1024 x 768	@ 60 Hz
(3)	1366 x 768	@ 60 Hz
(4)	1280 x 1024	@ 60 Hz
(5)	1920 x 1080	@ 60 Hz
(6)	1920 x 1200	@ 60 Hz

GOP Configuration

- **GOP Brightness Level:** 20, 40, 60, 80, 100, 120, 140, 160, 180, 200, 220, 240, 255
- **GOP Driver:** Enable, Disable

SATA Configuration

Use this screen to configure the SATA components listed below.



SATA Controller: Enable, Disable

Chipset SATA Mode: IDE, AHCI

- **SATA PORT:** Enable, Disable
- **SATA PORT 0 Hot Plug Capability:** Enable, Disable
- **SATA PORT 1 Hot Plug Capability:** Enable, Disable
- **SATA PORT 0 Connected to an 0DD:** Enable, Disable
- **SATA PORT 1 Connected to an 0DD:** Enable, Disable

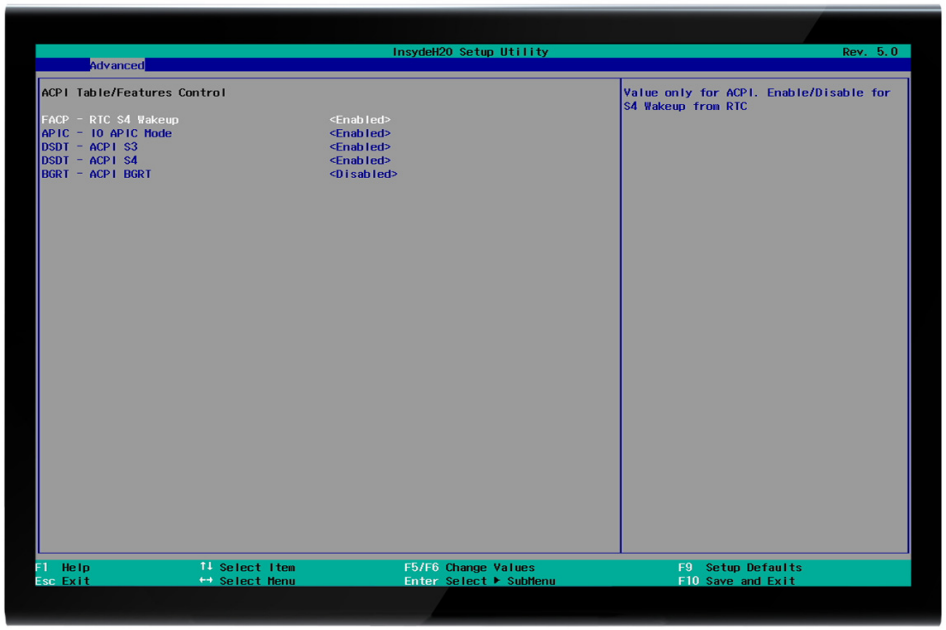
Serial ATA Port 0: Not Installed

Serial ATA Port 1: Not Installed

ACPI Table/Features Control

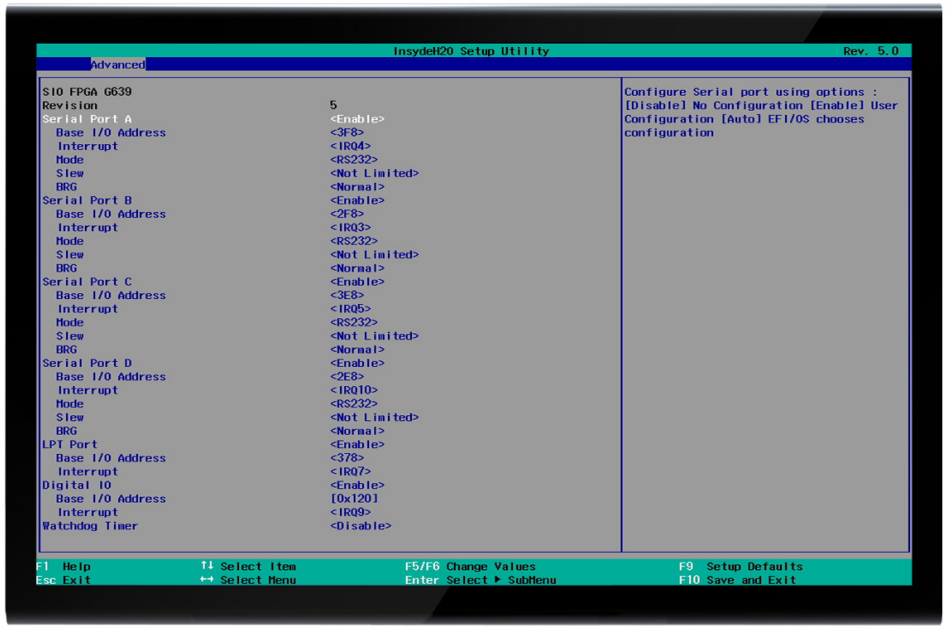
Use this screen to enable and disable the following components:

- FACP - RTC S4 Wakeup
- APIC - IO APIC Mode
- DSDT - ACPI S3
- DSDT - ACPI S4
- DSDT - ACPI BRGT



S10 FGPA G639

Use this screen to configure the S10 FGPA G639 components listed below.



Serial Port A through D: Enable, Disable

- **Base I/O Address:** 2E8, 2F8, 3E8, 3F8
- **Interrupt:** IRQ3 through IRQ11
- **Mode:** Loopback, RS232, RS485, RS422

- **Slew:** Not Limited, Limited
- **BRG:** Normal, High

LPT Port: Enable, Disable

- **Base I/O Interrupt:** 278, 378
- **Interrupt:** IRQ5 through IRQ7

Digital I/O: Enable, Disable

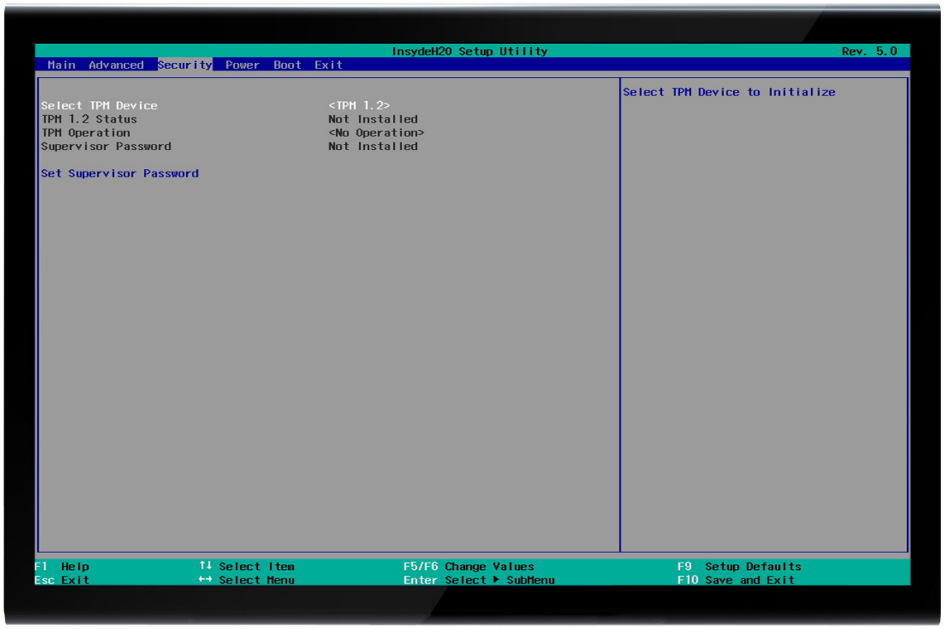
- **Base I/O Address:** [0x120]
- **Interrupt:** IRQ3 through IRQ11

Watchdog Timer: Enable, Disable

Security

Use this screen to configure, enable, and disable the following components:

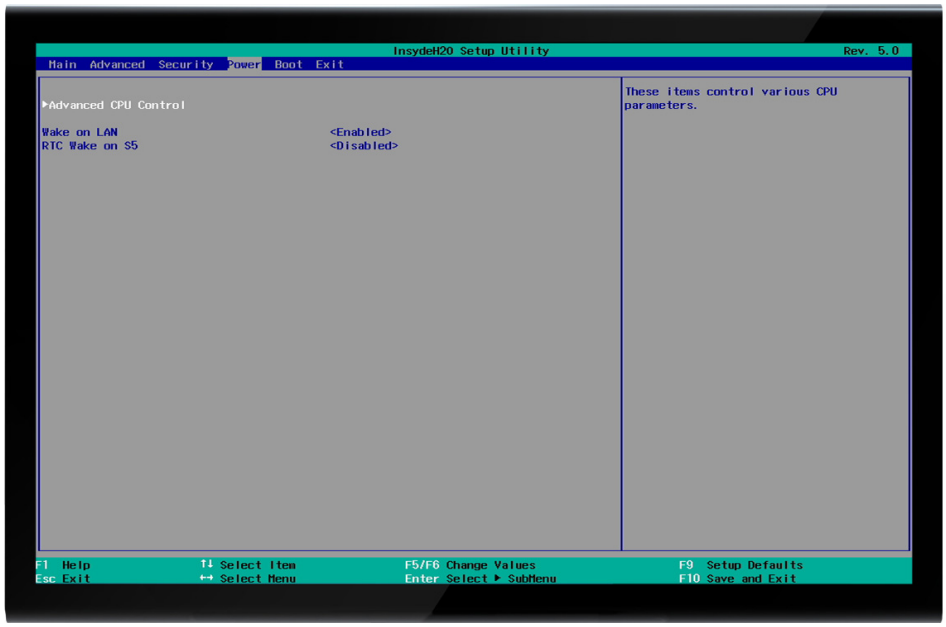
- **Select TPM Device:** TPM 1.2
- **Set Supervisor Password**



Power

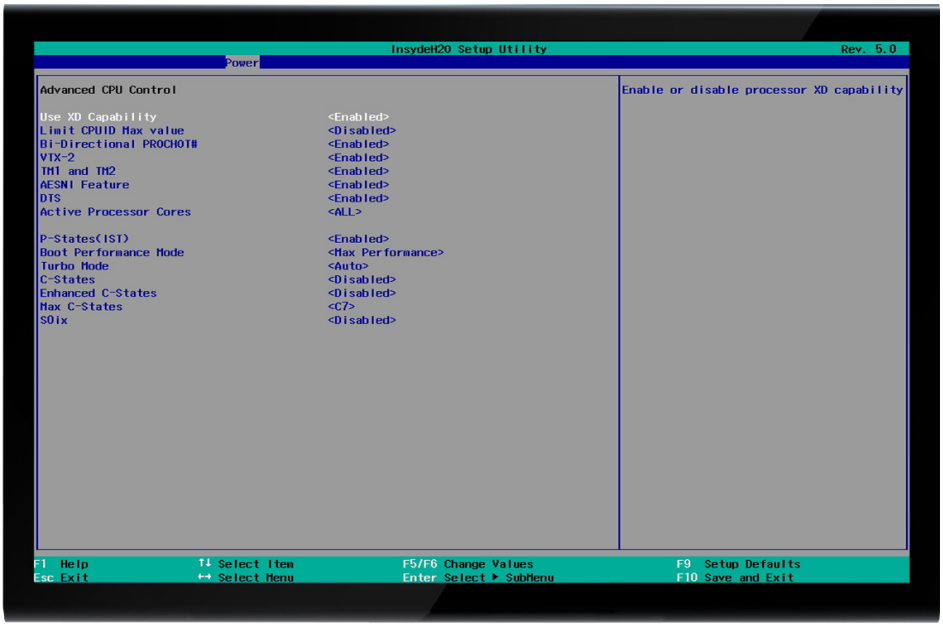
Use this screen to configure, enable, and disable the power components:

- **Advanced CPU Control:** Opens a new screen
- **Wake on LAN:** Enable, Disable
- **RTC Wake on S5:** Enable, Disable



Advanced CPU Control

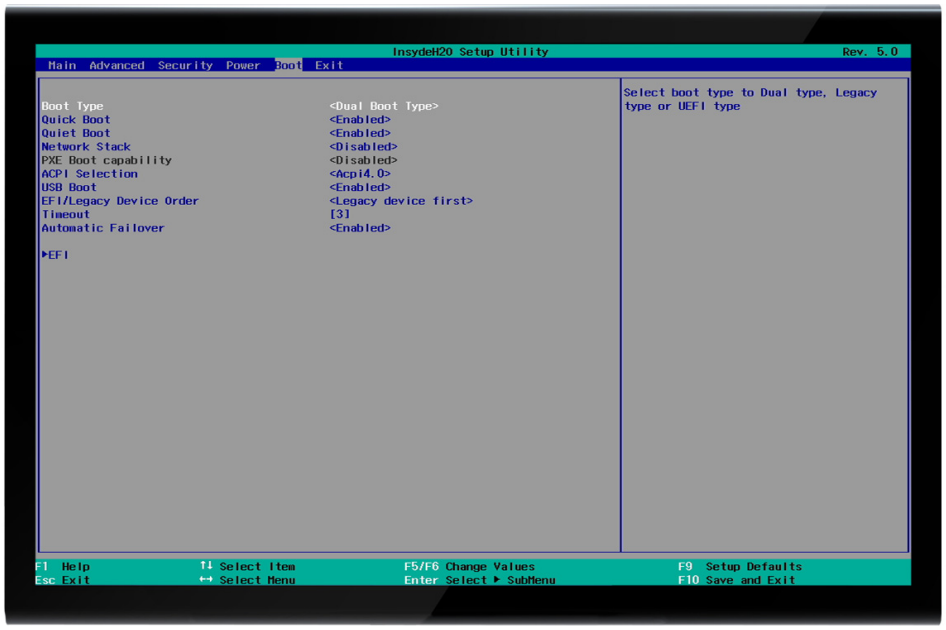
Use this screen to configure, enable, and disable the components listed below.



- **Use XD Capability:** Enable, Disable
- **Limit CPUID Max values:** Enable, Disable
- **Di-Directional PROCHOT#:** Enable, Disable
- **VTX-2:** Enable, Disable
- **TM1 AND TM2:** Enable, Disable
- **AESNI Feature:** Enable, Disable
- **DTS:** Enable, Disable
- **Active Processor Cores:** ALL, 1
- **P-Starts (IST):** Enable, Disable
- **Boot Performance Mode:** Max Performance, Max Battery
- **Turbo Mode:** Auto, Disabled, Enabled
- **C-States:** Enable, Disable
- **Enhanced C-States:** Enable, Disable
- **Max-C States:** C1, C6, C7
- **S0ix:** Enable, Disable

Boot

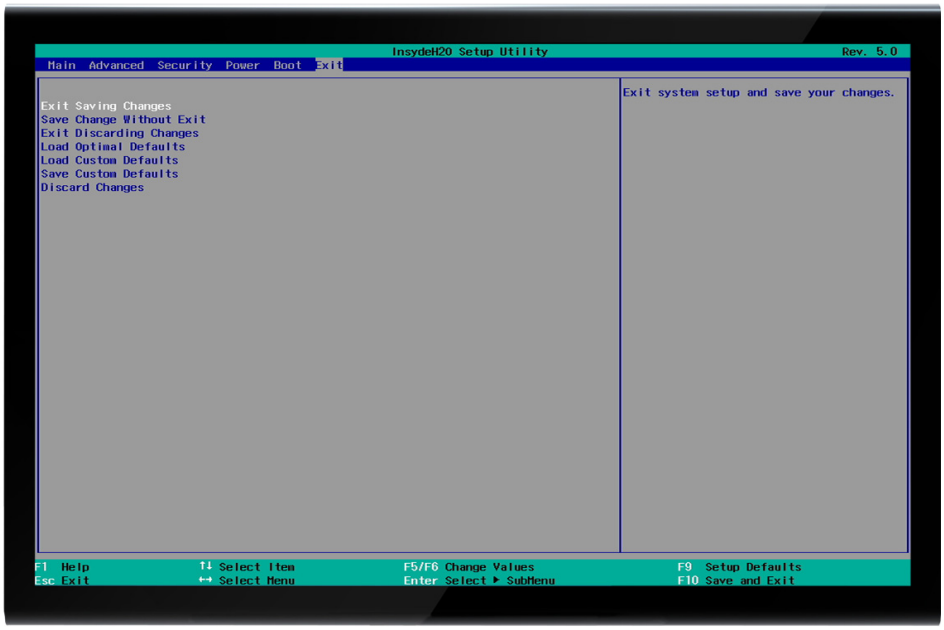
Use this screen to configure, enable, and disable the boot components listed below.



- **Boot Type:** Dual Boot Type, Legacy Boot Type, UEFI Boot Type
- **Quick Boot:** Enable, Disable
- **Quiet Boot:** Enable, Disable
- **Network Stack:** Enable, Disable
- **PXE Boot capability:** Enable, Disable
- **ACPI Selection:** Acpi1.0B, Acpi3.0, Acpi4.0, Acpi5.0
- **USB Boot:** Enable, Disable
- **EFI/Legacy Device Order:** EFI device first, Legacy device first, Smart Mode
- **Timeout:** Value
- **Automatic Failover:** Enable, Disable
- **EFI:** Internal EFI Shell

Exit

Use this screen to save or exit the BIOS configuration with specific treatment of any changes made.



9. Cables and Accessories

WINSYSTEMS cables and batteries simplify connection to the EBC-C413. The following table lists available items.

Item	Part Number	Connection	Description
Cables	CBL-236-G-2-1.5	See “PWR - Power Connector” on page 23	PWR power connection, DC harness EBC-TX. Unterminated, 18”
	CBL-173-G-1-1.0	See “COM3-4 - COM3 and COM4 Serial Ports” on page 25	COM3 and COM4, PCM-COM 4
	CBL-247-G-1-1.0	See “MIO - PS/2 Keyboard, Serial 1/2, and LPT” on page 26	Multi I/O: primary serial channels (COM1 and COM2), printer port, and keyboard
	CBL-RST-402-18	See “RST - Reset Connector” on page 28	Normally open monetary contact switch, 18”
	CBL-PWR-600-14	See “ATXAUX - ATX/Auxiliary Power Connector” on page 24	ATX signals for the power button, 5 V standby, and power good
	CBL-343-g-1-1-1.375	See “MOUSE - PS/2 Mouse Connector” on page 28	PS/2 mouse connection to 5 pin, 16.5”
	CBL-USB4-000-14	See “USB1 - USB Connector for Ports 0-3” on page 29. See “USB2 - USB Connector for Ports 4-7” on page 30	Pico-Clasp to unterminated
	CBL-USB4-001-12		Pico-Clasp to Pico-Clasp
	CBL-USB4-002-12		Pico-Clasp to 2 each, 2 x 4, 2 mm pitch housing
	CBL-129-4	See “DIO1 - Digital I/O Connector with Event Sense” on page 31 See “DIO2 - Digital I/O Connector” on page 33	Connect to 48 bidirectional TTL digital I/O lines (dual-port ram)
	CBL-SATA-701-20	See “SATA1 - Serial ATA Connector” on page 38	Latching signal, 0.5 m
	CBL-PWR-117-12	See “SATAPWR - Serial ATA Power Connector” on page 38	Power cable to SATA drive
	CBL-234-G-1-1-375	See “VGA - Analog VGA Display Connector” on page 41	2.0 mm to 15, D-sub (female)
	CBL-AUDIO7-102-12	Duo-Clasp. See “AUDIO - HD Audio Connector” on page 44	1.25 mm to 3 x 3.5 mm, 12”
	CBL-AUDIO7-100-14		1.25 mm, unterminated, 14"
	CBL-AUDIO5-102-12		1.25 mm to 6 x 3.5 mm, 12”
	CBL-AUDIO2-102-12		1.25 mm to 9 x 3.5 mm, 12”
Batteries	BAT-LTC-E-36-16-1	See “BAT - External Battery Connector” on page 43.	External 3.6 V, 1650 mAH battery with plug-in connector External
	BAT-LTC-E-36-27-1		External 3.6 V, 2700 mAH battery with plug-in connector
Screws	G527-0000-400	See “MC1 - MiniCard Connector with PCI-Express and USB” on page 46 See “MC2 - MiniCard/mSATA Connector with PCI-Express, USB, and SATA” on page 47	2 mm
Jumpers	KIT-JMP-G-200	See “Jumpers” on page 51	Jumper Kit (10 jumpers)

Item	Part Number	Connection	Description
Standoffs	KIT-PCM-STANDOFF-4	See “Mounting and Protecting the EBC-C413” on page 73	Four piece Nylon Hex PC104 Standoff Kit
	KIT-PCM-STANDOFF-B-4		Four piece Brass Hex PC104 Standoff Kit

10. Software Drivers

Go to www.winsystems.com for information on available software drivers.

Appendix A. Best Practices

This section outlines the best practices for operating the EBC-C413 in a safe, effective manner that does not damage the board. Read this section carefully.

Power Supply

Avoid Electrostatic Discharge (ESD)
Only handle the circuit board and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

Power Supply Budget

Evaluate your power supply budget. It is usually good practice to budget twice the typical power requirement for all of your devices.

Zero-Load Power Supply

Use a zero-load power supply whenever possible. A zero-load power supply does not require a minimum power load to regulate. If a zero-load power supply is not appropriate for your application, then verify that the single board computer's typical load is not lower than the power supply's mum load. If the single board computer does not draw enough power to meet the power supply's minimum load, then the power supply does not regulate properly and can cause damage to the EBC-C413.

Use Proper Power Connections (Voltage)—When verifying the voltage, measure it at the power connector on the EBC-C413. Measuring it at the power supply does not account for voltage drop through the wire and connectors.

The EBC-C413 requires +5 V (±5%) to operate. Verify the power connections. Incorrect voltages can cause catastrophic damage.

Populate all of the +5 V and ground connections. Most single board computers have multiple power and ground pins, and all of them should be populated. The more copper connecting the power supply to the EBC-C413 the better.

Adjusting Voltage

If you have a power supply that allows you to adjust the voltage, it is a good idea to set the voltage at the power connector of the EBC-C413 to 5.1 V. The EBC-C413 can tolerate up to 5.25 V, so setting your power supply to provide 5.1 V is safe and allows for a small amount of voltage drop that occurs over time as the power supply ages and the connector contacts oxidize.

Power Harness

Minimize the length of the power harness. This reduces the amount of voltage drop between the power supply and the EBC-C413.

Gauge Wire

Use the largest gauge wire that you can. Most connector manufacturers have a maximum gauge wire they recommend for their pins. Try going one size larger; it usually works and the extra copper helps your system perform properly over time.

Contact Points

WINSYSTEMS boards mostly use connectors with gold finish contacts. Gold finish contacts are used exclusively on high speed connections. Power and lower speed peripheral connectors may use a tin finish as an alternative contact surface. It is critical that the contact material in the mating connectors is matched properly (gold to gold and tin to tin). Contact areas made with dissimilar metals can cause oxidation/corrosion, resulting in unreliable connections.

Pin Contacts

Often the pin contacts used in cabling are not given enough attention. The ideal choice for a pin contact uses a design similar to Molex's or Trifurcon's design, which provides three distinct points to maximize the contact area and improve connection integrity in high shock and vibration applications.

Power Down

Make sure that power has been removed from the system before making or breaking any connections.

Power Supply OFF—The power supply should always be off before it is connected to the I/O Module. Do not hot-plug the EBC-C413 on a host platform that is already powered.

I/O Connections OFF—I/O connections should also be off before connecting them to the embedded computer modules or any I/O cards. Connecting hot signals can cause damage whether the embedded system is powered or not.

Mounting and Protecting the EBC-C413

The EBC-C413 must be mounted properly to avoid damage. The following standoff kits are available and recommended for use with the EBC-C413:

- KIT-PCM-STANDOFF-4: Four-piece nylon hex PC104 standoff kit
- KIT-PCM-STANDOFF-B-4: Four-piece brass hex PC104 standoff kit

The following table lists the items contained in each kit.

Kit	Component	Description	Qty
KIT-PCM-STANDOFF-4 4 pc. nylon hex PC104 standoff kit	Standoff	Nylon 0.25" hex, 0.600" long male/female 4-40	4
	Hex Nut	Hex nylon 4-40	4
	Screw	Phillips-pan head (PPH) 4-40 x 1/4" stainless steel	4
KIT-PCM-STANDOFF-B-4 4 pc. brass hex PC104 standoff kit	Standoff	Brass 5 mm hex, 0.600" long male/female 4-40	4
	Hex Nut	4-40 x 0.095 thick, nickel finish	4
	Screw	Phillips-pan head (PPH) 4-40 x 1/4" stainless steel	4

Placing the EBC-C413 on Mounting Standoffs—Be careful when placing the EBC-C413 on the mounting standoffs. Sliding the board around until the standoffs are visible from the top can cause component damage on the bottom of the board.

Do Not Bend or Flex the EBC-C413—Bending or flexing can cause irreparable damage. Embedded computer modules are especially sensitive to flexing or bending around Ball Grid Array (BGA) devices. BGA devices are extremely rigid by design and flexing or bending the embedded computer module can cause the BGA to tear away from the printed circuit board.

Mounting Holes—The mounting holes are plated on the top, bottom and through the barrel of the hole and are connected to the embedded computer module's ground plane. Traces are often routed in the inner layers right below, above or around the mounting holes.

- Never use a drill or any other tool in an attempt to make the holes larger.
- Never use screws with oversized heads. The head could come in contact with nearby components causing a short or physical damage.
- Never use self-tapping screws; they compromise the walls of the mounting hole.
- Never use oversized screws that cut into the walls of the mounting holes.

- Always use all of the mounting holes. By using all of the mounting holes, you provide the support that the embedded computer module needs to prevent bending or flexing.

Plug or Unplug Connectors Only on Fully Mounted Boards—Never plug or unplug connectors on a board that is not fully mounted. Many of the connectors fit tightly, and the force needed to plug or unplug them could cause the embedded computer module to flex.

Avoid Cutting the EBC-C413—Never use star washers or any fastening hardware that cuts into the EBC-C413.

Avoid Over-tightening of Mounting Hardware—Causing the area around the mounting holes to compress could damage interlayer traces around the mounting holes.

Use Appropriate Tools—Always use tools that are appropriate for working with small hardware. Large tools can damage components around the mounting holes.

Avoid Conductive Surfaces—Never allow the embedded computer module to be placed on a conductive surface. Many embedded systems use a battery to back up the clock-calendar and CMOS memory. A conductive surface such as a metal bench can short the battery causing premature failure.

Adding PC104 Boards to your Stack

Be careful when adding PC104 boards to your stack—Never allow the power to be turned on when a PC104 board has been improperly plugged onto the stack. It is possible to misalign the PC104 card and leave a row of pins on the end or down the long side hanging out of the connector. If power is applied with these pins misaligned, it causes the I/O board to be damaged beyond repair.

Conformal Coating

Conformal coating by any source other than WINSYSTEMS voids the product warranty and will not be accepted for repair by WINSYSTEMS. If such a product is sent to WINSYSTEMS for repair, it will be returned at customer expense and no service will be performed. A WINSYSTEMS product conformally coated by WINSYSTEMS will be subject to regular WINSYSTEMS warranty terms and conditions.

Operations/Product Manuals

Every single board computer has an Operations manual or Product manual.

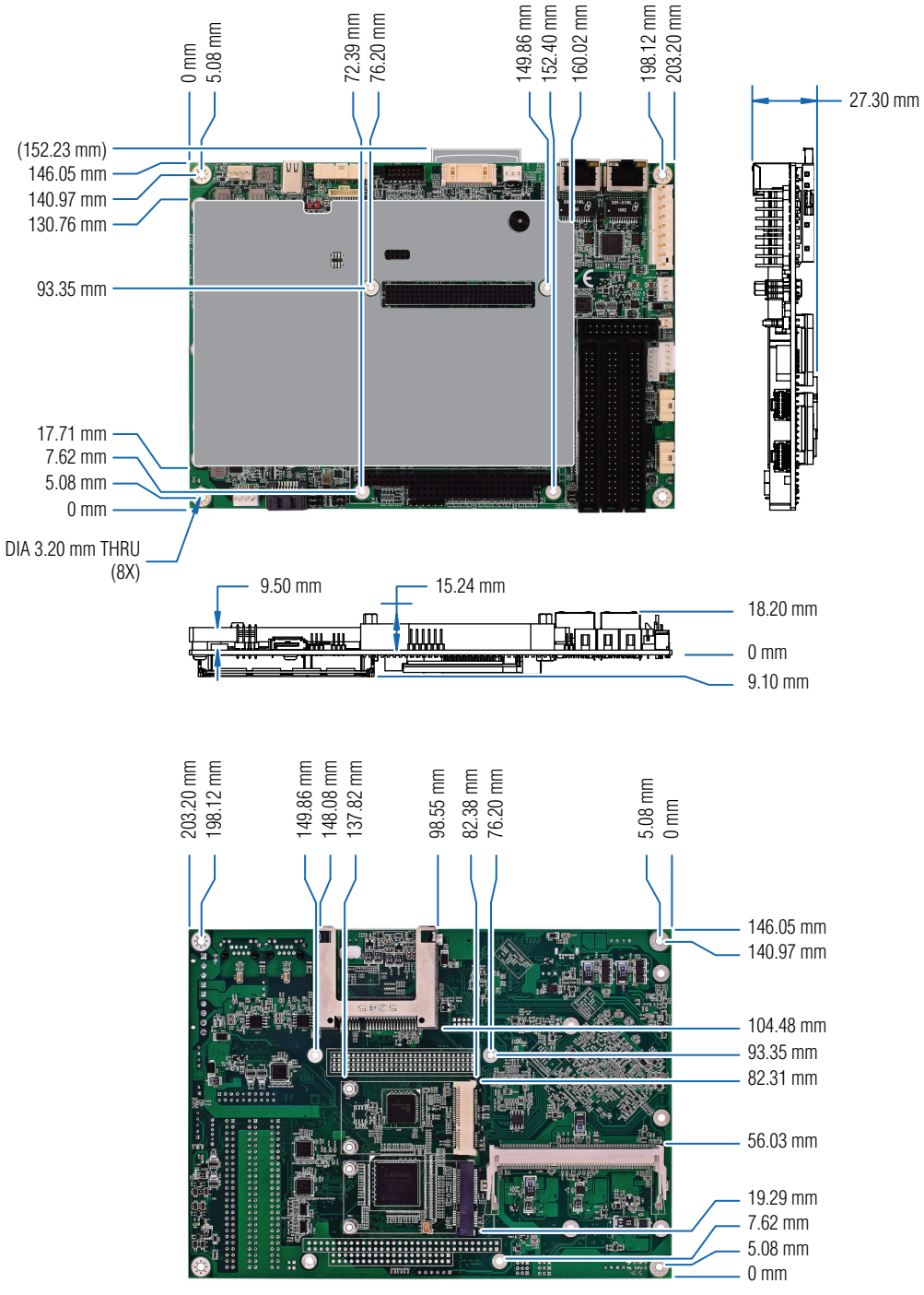
Periodic Updates—Operations/Product manuals are updated often. Periodically check the WINSYSTEMS website (https://www.winsystems.com) for revisions.

Check Pinouts—Always check the pinout and connector locations in the manual before plugging in a cable. Many I/O modules have identical headers for different functions and plugging a cable into the wrong header can have disastrous results.

Contact an Applications Engineer—If a diagram or chart in a manual does not seem to match your board, or if you have additional questions, contact a WINSYSTEMS Applications Engineer at: +1-817-274-7553.

Appendix B. Mechanical Drawings

EBC-C413 Dimensions



Appendix C. Power-on Self-Test (POST) Codes

If the system hangs before the BIOS can process the error, the value displayed at the I/O port address **80h** is the code of the last successful operation. In this case, the screen does not display an error code.

POST_CODE()

Use the `POST_CODE()` macro to output a number (Data) to the configured I/O port or status code.

Prototype

```
#include "InsydeModulePkg/Include/PostCode.h" POST_CODE(Data)
```

Parameters

Data: Unsigned integer that specifies the POST Code value. Must be between **0x00** and **0xff**.

POST Codes

POST codes are 8-bit unsigned integer values that are sent to a specific I/O port (where hardware can decode and display the value) or to the DDT debugger.

8-Bit POST Code Ranges

This table shows the overview of the 8-Bit POST code ranges used by InsydeH2O.

Phase	POST Code Value Ranges
SEC	0x01 - 0x0F
PEI	0x70 - 0x9F
DXE	0x40 - 0x6F
BDS	0x10 - 0x3F
SMM	0xA0 - 0xBF
S3	0xC0 - 0xCF
ASL	0x51 - 0x55 0xE1 - 0xE4
PostBDS	0xF9 - 0xFE
Insyde H2ODDT Reserved	0xD0 - 0xD7

Phase	POST Code Value Ranges
OEM Reserved	0xE8 - 0xEB
Reserved	0xD8 - 0xE0 0xE5 - 0xE7 0xEC - 0xF8

SEC Phase

The SEC phase 8-Bit POST code values are shown in the table below.

NOTE The shaded rows in the table indicate the related functions are not from InsydeH2O (platform dependent).

Value	Functionality Name	Description
01	SEC_SYSTEM_POWER_ON	CPU power on and switch to Protected mode
02	SEC_BEFORE_MICROCODE_PATCH	Patching CPU microcode
03	SEC_AFTER_MICROCODE_PATCH	Setup Cache as RAM
04	SEC_ACCESS_CSR	PCIE MMIO Base Address initial
05	SEC_GENERIC_MSRINIT	CPU Generic MSR initialization
06	SEC_CPU_SPEEDCFG	Setup CPU speed
07	SEC_SETUP_CAR_OK	Cache as RAM test
08	SEC_FORCE_MAX_RATIO	Tune CPU frequency ratio to maximum level
09	SEC_GO_TO_SECSTARTUP	Setup BIOS ROM cache
0A	SEC_GO_TO_PEICORE	Enter Boot Firmware Volume

PEI Phase

The PEI phase 8-Bit POST code values are shown in the table below.

NOTE The shaded rows in the table indicate the related functions are not from InsydeH2O (platform dependent).

Value	Functionality Name	Description
70	PEI_SIO_INIT	Super I/O initialization
71	PEI_CPU_REG_INIT	CPU Early Initialization
72	PEI_CPU_AP_INIT	Multi-processor Early initialization
73	PEI_CPU_HT_RESET	HyperTransport initialization
74	PEI_PCIE_MMIO_INIT	PCIE MMIO BAR Initialization
75	PEI_NB_REG_INIT	North Bridge Early Initialization
76	PEI_SB_REG_INIT	South Bridge Early Initialization
77	PEI_PCIE_TRAINING	PCIE Training
78	PEI_TPM_INIT	TPM Initialization
79	PEI_SMBUS_INIT	SMBUS Early Initialization
7A	PEI_PROGRAM_CLOCK_GEN	Clock Generator Initialization
7B	PEI_IGD_EARLY_INITIAL	Internal Graphic device early initialization
7C	PEI_HECI_INIT	HECI Initialization

Value	Functionality Name	Description
7D	PEI_WATCHDOG_INIT	Watchdog timer initialization
7E	PEI_MEMORY_INIT	Memory Initialization for Normal boot
7F	PEI_MEMORY_INIT_FOR_CRISIS	Memory Initialization for Crisis Recovery
80	PEI_MEMORY_INSTALL	Simple Memory test
81	PEI_TXTPEI	TXT function early initialization
82	PEI_SWITCH_STACK	Start to use Memory
83	PEI_MEMORY_CALLBACK	Set cache for physical memory
84	PEI_ENTER_RECOVERY_MODE	Recovery device initialization
85	PEI_RECOVERY_MEDIA_FOUND	Found Recovery image
86	PEI_RECOVERY_MEDIA_NOT_FOUND	Recovery image not found
87	PEI_RECOVERY_LOAD_FILE_DONE	Load Recovery Image complete
88	PEI_RECOVERY_START_FLASH	Start Flash BIOS with Recovery image
89	PEI_ENTER_DXEIPL	Loading BIOS image to RAM
8A	PEI_FINDING_DXE_CORE	Loading DXE core
8B	PEI_GO_TO_DXE_CORE	Enter DXE core
8C	PEI_IFFS_TRANSITION_START	iFFS Transition Start
8D	PEI_IFFS_TRANSITION_END	iFFS Transition End

DXE Phase

The DXE phase 8-Bit POST code values are shown in the table below.

NOTE The shaded rows in the table indicate the related functions are not from InsydeH2O (platform dependent).

Value	Functionality Name	Description
40	DXE_TCGDXE	TPM initialization in DXE
41	DXE_SB_SPI_INIT	South bridge SPI initialization
42	DXE_CF9_RESET	Setup Reset service
43	DXE_SB_SERIAL_GPIO_INIT	South bridge Serial GPIO initialization
44	DXE_SMMACCESS	Setup SMM ACCESS service
45	DXE_NB_INIT	North bridge Middle initialization
46	DXE_SIO_INIT	Super I/O DXE initialization
47	DXE_LEGACY_REGION	Set up Legacy Region service
48	DXE_SB_INIT	South Bridge Middle Initialization
49	DXE_IDENTIFY_FLASH_DEVICE	Identify Flash device
4A	DXE_FTW_INIT	Fault Tolerant Write verification
4B	DXE_VARIABLE_INIT	Variable Service Initialization
4C	DXE_VARIABLE_INIT_FAIL	Fail to initialize Variable services
4D	DXE_MTC_INIT	MTC Initialization
4E	DXE_CPU_INIT	CPU middle-phase initialization
4F	DXE_MP_CPU_INIT	Multi-processor middle-phase initialization
50	DXE_SMBUS_INIT	SMBUS Initialization
51	DXE_SMART_TIMER_INIT	8259 Initialization
52	DXE_PCRTC_INIT	RTC Initialization
53	DXE_SATA_INIT	SATA Controller early initialization
54	DXE_SMM_CONTROLER_INIT	Setup SMM Control service
55	DXE_LEGACY_INTERRUPT	Setup legacy interrupt services

Value	Functionality Name	Description
56	DXE_RELOCATE_SMBASE	Relocate SMM BASE
57	DXE_FIRST_SMI	SMI test
58	DXE_VTD_INIT	VTD Initialization
59	DXE_BEFORE_CSM16_INIT	Legacy BIOS initialization
5A	DXE_AFTER_CSM16_INIT	Legacy interrupt function initialization
5B	DXE_LOAD_ACPI_TABLE	ACPI Table Initialization
5C	DXE_SB_DISPATCH	Setup SB SMM Dispatcher service
5D	DXE_SB_IOTRAP_INIT	Setup SB IOTRAP service
5E	DXE_SUBCLASS_DRIVER	Build AMT Table
5F	DXE_PPM_INIT	PPM Initialization
60	DXE_HECIDRV_INIT	HECIDRV Initialization
61	DXE_VARIABLE_RECLAIM	Variable store garbage collection and reclaim operation
62	DXE_FLASH_PART_NONSUPPORT	Flash part not supported

BDS Phase

The BDS phase 8-Bit POST code values are shown in the table below.

NOTE The shaded rows in the table indicate the related functions are not from InsydeH2O (platform dependent).

Value	Functionality Name	Description
10	BDS_ENTER_BDS	Enter BDS entry
11	BDS_INSTALL_HOTKEY	Install Hotkey service
12	BDS_ASF_INIT	ASF Initialization
13	BDS_PCI_ENUMERATION_START	PCI enumeration
14	BDS_BEFORE_PCIIO_INSTALL	PCI resource assign complete
15	BDS_PCI_ENUMERATION_END	PCI enumeration complete
16	BDS_CONNECT_CONSOLE_IN	Keyboard controller, keyboard, and mouse initialization
17	BDS_CONNECT_CONSOLE_OUT	Video device initialization
18	BDS_CONNECT_STD_ERR	Error report device initialization
19	BDS_CONNECT_USB_HC	USB host controller initialization
1A	BDS_CONNECT_USB_BUS	USB BUS driver initialization
1B	BDS_CONNECT_USB_DEVICE	USB device driver initialization
1C	BDS_NO_CONSOLE_ACTION	Console device initialization fail
1D	BDS_DISPLAY_LOGO_SYSTEM_INFO	Display logo or system information
1E	BDS_START_IDE_CONTROLLER	IDE controller initialization
1F	BDS_START_SATA_CONTROLLER	SATA controller initialization
20	BDS_START_ISA_ACPI_CONTROLLER	SIO controller initialization
21	BDS_START_ISA_BUS	ISA BUS driver initialization
22	BDS_START_ISA_FDD	Floppy device initialization
23	BDS_START_ISA_SEIRAL	Serial device initialization
24	BDS_START_IDE_BUS	IDE device initialization
25	BDS_START_AHCI_BUS	AHCI device initialization
26	BDS_CONNECT_LEGACY_ROM	Dispatch option ROMs

Value	Functionality Name	Description
27	BDS_ENUMERATE_ALL_BOOT_OPTION	Get boot device information
28	BDS_END_OF_BOOT_SELECTION	End of boot selection
29	BDS_ENTER_SETUP	Enter Setup menu
2A	BDS_ENTER_BOOT_MANAGER	Enter Boot manager
2B	BDS_BOOT_DEVICE_SELECT	Try to boot system to OS
2C	BDS_EFI64_SHADOW_ALL_LEGACY_ROM	Shadow Misc Option ROM
2D	BDS_ACPI_S3SAVE	Save S3 resume required data in RAM
2E	BDS_READY_TO_BOOT_EVENT	Last chipset initialization before boot to OS
2F	BDS_GO_LEGACY_BOOT	Start to boot Legacy OS
30	BDS_GO_UEFI_BOOT	Start to boot UEFI OS
31	BDS_LEGACY16_PREPARE_TO_BOOT	Prepare to Boot to Legacy OS
32	BDS_EXIT_BOOT_SERVICES	Send END of POST Message to ME via HECI
33	BDS_LEGACY_BOOT_EVENT	Last chipset initialization before boot to Legacy OS
34	BDS_ENTER_LEGACY_16_BOOT	Ready to Boot Legacy OS
35	BDS_RECOVERY_START_FLASH	Fast recovery start flash
36	BDS_START_SDHC_BUS	SDHC device initialization
37	BDS_CONNECT_ATA_LEGACY	ATA legacy device initialization
38	BDS_CONNEC_SD_LEGACY	SD legacy device initialization

PostBDS Phase

The PostBDS phase 8-Bit POST code values are shown in the table below.

Value	Functionality Name	Description
F9	POST_BDS_NO_BOOT_DEVICE	No Boot Device
FB	POST_BDS_START_IMAGE	UEFI Boot Start Image
FD	POST_BDS_ENTER_INT19	Legacy 16 boot entry
FE	POST_BDS_JUMP_BOOT_SECTOR	Try to Boot with INT 19

S3

The S3 phase 8-Bit POST code values are shown in the table below.

Value	Functionality Name	Description
C0	S3_RESTORE_MEMORY_CONTROLLER	Memory initialization for S3 resume
C1	S3_INSTALL_S3_MEMORY	Get S3 resume required data from memory
C2	S3_SWITCH_STACK	Start to use memory during S3 resume
C3	S3_MEMORY_CALLBACK	Set cache for physical memory during S3 resume
C4	S3_ENTER_S3_RESUME_PEIM	Start to restore system configuration
C5	S3_BEFORE_ACPI_BOOT_SCRIPT	Restore system configuration stage 1
C6	S3_BEFORE_RUNTIME_BOOT_SCRIPT	Restore system configuration stage 2
C7	S3_BEFORE_RELOCATE_SMM_BASE	Relocate SMM BASE during S3 resume
C8	S3_BEFORE_MP_INIT	Multi-processor initialization during S3 resume
C9	S3_BEFORE_RESTORE_ACPI_CALLBACK	Start to restore system configuration in SMM
CA	S3_AFTER_RESTORE_ACPI_CALLBACK	Restore system configuration in SMM complete
CB	S3_GO_TO_FACS_WAKING_VECTOR	Back to OS

ACPI

The ACPI phase 8-Bit POST code values are shown in the table below.

Value	Functionality Name	Description
51	ASL_ENTER_S1	Prepare to enter S1
53	ASL_ENTER_S3	Prepare to enter S3
54	ASL_ENTER_S4	Prepare to enter S4
55	ASL_ENTER_S5	Prepare to enter S5
E1	ASL_WAKEUP_S1	System wakeup from S1
E3	ASL_WAKEUP_S3	System wakeup from S3
E4	ASL_WAKEUP_S4	System wakeup from S4
E5	ASL_WAKEUP_S5	System wakeup from S5

SMM

The SMM phase 8-Bit POST code values are shown in the table below.

Value	Functionality Name	Description
A0	SMM_IDENTIFY_FLASH_DEVICE	Identify flash device in SMM
A2	SMM_SMM_PLATFORM_INIT	SMM service initialization
A6	SMM_ACPI_ENABLE_START	OS call ACPI enable function
A7	SMM_ACPI_ENABLE_END	ACPI enable function complete
A1	SMM_S1_SLEEP_CALLBACK	Enter S1
A3	SMM_S3_SLEEP_CALLBACK	Enter S3
A4	SMM_S4_SLEEP_CALLBACK	Enter S4
A5	SMM_S5_SLEEP_CALLBACK	Enter S5
A8	SMM_ACPI_DISABLE_START	OS call ACPI disable function
A9	SMM_ACPI_DISABLE_END	ACPI disable function complete

InsydeH2O DDT Debugger

The InsydeH2O DDT Debugger 8-Bit POST code values are shown in the table below.

Value	Functionality Name	Description
0D	Used by Insyde debugger	Waiting for device connect
D0	Used by Insyde debugger	Waiting for device connect
D1	Used by Insyde debugger	InsydeH2O DDT ready
D2	Used by Insyde debugger	EHCI not found
D3	Used by Insyde debugger	Debug port connect low speed device
D4	Used by Insyde debugger	DDT cable became low speed device
D5	Used by Insyde debugger	DDT cable transmission error (Get descriptor fail)
D6	Used by Insyde debugger	DDT cable transmission error (Set debug mode fail)
D7	Used by Insyde debugger	DDT cable transmission error (Set address fail)

Appendix D. Warranty Information

Full warranty information can be found at https://winsystems.com/company-policies/warranty/.