WINSYSTEMS®

CFAST-B-XXG-SI

Industrial 64 GB CFast Card

Product Manual

WINSYSTEMS®

INDUSTRIAL GRADE

CFAST
32GB
-40°C to +85°C

Revision History

Document Version	Last Updated Date	Brief Description of Change
v1.0	8/20/2021	Initial release

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Table of Contents

1. Before You Begin

Review the warnings (in this section) and the best practice recommendations (see "Best Practices" on page 33) when using and handling the WINSYSTEMS CFAST-B-XXG-SI. Adherence to these recommendations provides an optimal user experience and prevents damage. Read through this document and become familiar with the CFAST-B-XXG-SI before proceeding.

FAILING TO COMPLY WITH THESE BEST PRACTICES MAY DAMAGE THE CFAST-B-XXG-SI AND VOID YOUR WARRANTY.

1.1 Warnings

Only qualified personnel should configure and install the CFAST-B-XXG-SI. While observing the best practices, pay particular attention to the following.

Avoid electrostatic discharge (ESD)
Only handle the circuit board and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

2. Introduction

This manual provides information for the CFAST-B-XXG-SI. If you still have questions, contact Technical Support at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

3. Features

Capacity/Flash Type

• 2 GB to 32 GB industrial temperature SLC

SATA Interface

• CFast 2.0 compliant
• SATA 3.3 compliant

Flash Interface

• Flash type: SLC

Performance

- Sequential read from 65 MB/s up to 255 MB/s
- Sequential write from 45 MB/s up to 90 MB/s

Power Consumption

- Active mode: up to 315 mA
- Idle mode: < 65 mA

General

- Static and dynamic wear leveling
- Bad block management
- SMART
- Firmware update capability
- Supports secure erase and sanitize via ATA passthrough commands

Environment

- -40 to +85°C operating temperature range
- -50 to +100°C storage temperature range
- RoHS compliant
- Relative humidity 10 to 95% under 55°C
- Shock specification: 12G Sawtooth pulse, 11 ms duration, 3 axes
- Vibration specification:
    - Sine vibration: 10 ~2000 Hz, 16.3 G peak to peak, 3 axes
    - Random vibration: 10 ~2000 Hz, 1.49 GRMS, 3 axes

Reliability

- MTBF: More than 2,000,000 hours at 0 to 25°C operation

ECC

- Flexible BCH and GCC engines, providing correction capability based on flash configuration
- Controller SRAM ECC

OS Compatibility

All SATA 3.3 compatible operating systems supported, including:

- Windows 7 (32 and 64 bit), Windows 8, Windows 10, Windows XP
- Linux Kernel 4.2.0-27 (Ubuntu 15.10)
- Mac OS X 10.8.4, 10.11.2

4.   Functionality

WINSYSTEMS CFAST-B-XXG-SI Industrial CFast 2.0 is designed as compact, removable storage media to be used as a boot device or for storing critical data. The industrial-grade card is fully compliant with CFast 2.0 specifications, and is built with industrial temp SLC NAND flash.

NOTE The CFAST-B-XXG-SI Industrial CFast is also available in a Security version, with locking, AES encryption and key management capabilities enabled through a custom firmware interface. Contact your WINSYSTEMS account manager for more information.

4.1   Flash Management

4.1.1   Error Correction Code (ECC)

Flash memory cells deteriorate with use, which might generate random bit errors in the stored data. Thus, the controller in WINSYSTEMS' Industrial CFast drive applies an advanced BCH ECC algorithm, which can detect and correct errors occur during read processes, ensuring data been read correctly, as well as protecting data from corruption. The WINSYSTEMS Industrial CFast also employs "near-miss" ECC, such that all blocks which reach a certain error threshold are automatically refreshed immediately upon detection. The threshold is determined by the specific flash and ECC configuration in the card.

4.1.2   Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some blocks are updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling techniques are applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

The controller in WINSYSTEMS newest Industrial CFast drive utilizes an advanced Wear Leveling algorithm, which optimizes life and performance, through a combination of static and global wear leveling. Static wear leveling is utilized until one flash reaches 90% of the rated P/E cycles, which is more efficient from a performance standpoint. Once a flash reaches 90%, wear leveling switches to a global scheme, and all flash blocks participate in wear leveling as one large pool, which enables the card to maximize lifetime.

4.1.3   Bad Block Management

Bad blocks are blocks that include one or more invalid bits and therefore, their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as "initial bad blocks." Blocks that develop invalid bits during the lifespan of the flash are named "later bad

blocks." The controller in the WINSYSTEMS CFAST-B-XXG-SI drive implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manage any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves data reliability.

4.1.4 SMART

Self-Monitoring, Analysis, and Reporting Technology (SMART) is a special function that allows a memory device to automatically monitor its health. Refer to "ATA SMART Functionality" for the command details and the information that can be extracted from the card.

4.1.5 Read Disturb Management

WINSYSTEMS Industrial CFast drives have advanced Read Disturb Management to prevent uncorrectable errors in heavy read applications. As flash geometries shrink, the likelihood of disturbances when adjacent pages are frequently read is increased, and typically wear leveling is triggered by writing and erasing. However, the advanced read disturb management system actually counts all reads on a block level, and compares them to a configurable threshold. When the threshold has been reached, a read wear level is triggered and the block is refreshed, sending it to the back of the line. This ensures that errors do not accumulate to the point that they are uncorrectable.

4.1.6 Firmware Redundancy

Since flash storage is often used in applications with unstable sources of power, protecting the firmware is critical. WINSYSTEMS Industrial CFast drives maintain two copies of firmware within the flash, so that if the primary copy of the firmware is damaged, the back-up copy can be used. If the back-up copy is used, then the original copy is repaired.

4.1.7 Dynamic Data Refresh

Typically, when a drive is new and less than 10% of the program/erase cycles have been consumed, the data retention time of the flash is 5 or 10 years, depending on the type of flash. At end of life, however, when 100% of the program/erase cycles have been consumed, typically, the retention time is 1 year. To extend long term data retention over the life of a card, WINSYSTEMS CFAST-B-XXG-SI automatically refreshes data that is not accessed for a long time, which can be triggered based on a configurable power-on count threshold and operate in the background.

4.1.8 Power Fail Robustness

With the goal of preventing data corruption and card failure, the WINSYSTEMS Industrial CFast drives have been developed to survive unscheduled power interruptions with minimal effect. In the event of a power loss, the controller resets and flash is immediately write-protected.

A log is kept of recent flash transactions, and if the last data in the log is corrupt, then the controller recovers the latest valid entry. If a write operation was in process at the time of the power loss, but not committed to flash, or the tables had not yet been updated, then this data might be lost. The original data is always kept in a "twin" of the active block, so we can always revert back to the last known valid state of the card.

4.1.9   Page-based Mapping

CFAST-B-XXG-SI uses page-based mapping, which has the advantages of improved random performance and reduced write amplification, which improves device overall life.

5.   Endurance and Data Retention

Attribute	Value
Raw flash program/ erase rating	50,000 cycles for 2 and 4 GB capacities
	100,000 cycles for 8 GB and higher capacities
TBW	Contact WINSYSTEMS for TBW and life estimate based on your specific application/workload
Data retention	10 years when P/E cycles <10% of rated cycling
	1 year when P/E cycles at 100% of rated cycling

6.   Sequential and Random Performance

Performance is measured with CrystalDiskMark 3.0.3 64 bit, random performance for 4K blocks. Performance by capacity and firmware type is shown in the table.

Capacity	Sequential		Random	
	Read (MB/s)	Write (MB/s)	Read (MB/s)	Write (MB/s)
2 GB SLC	65	45	10	5
4 GB SLC	65	47	10	5
8 GB SLC	255	50	14	5
16 GB SLC	255	70	14	5
32 GB SLC	255	90	14	5
64 GB SLC	260	115	14	5

7. CF Card Interface

7.1 CF Card Interface

CFast Mechanical Form Factor Attributes

Dimension	Measurement
Height	3.6 mm
Width	42.8 mm
Length	36.4 mm
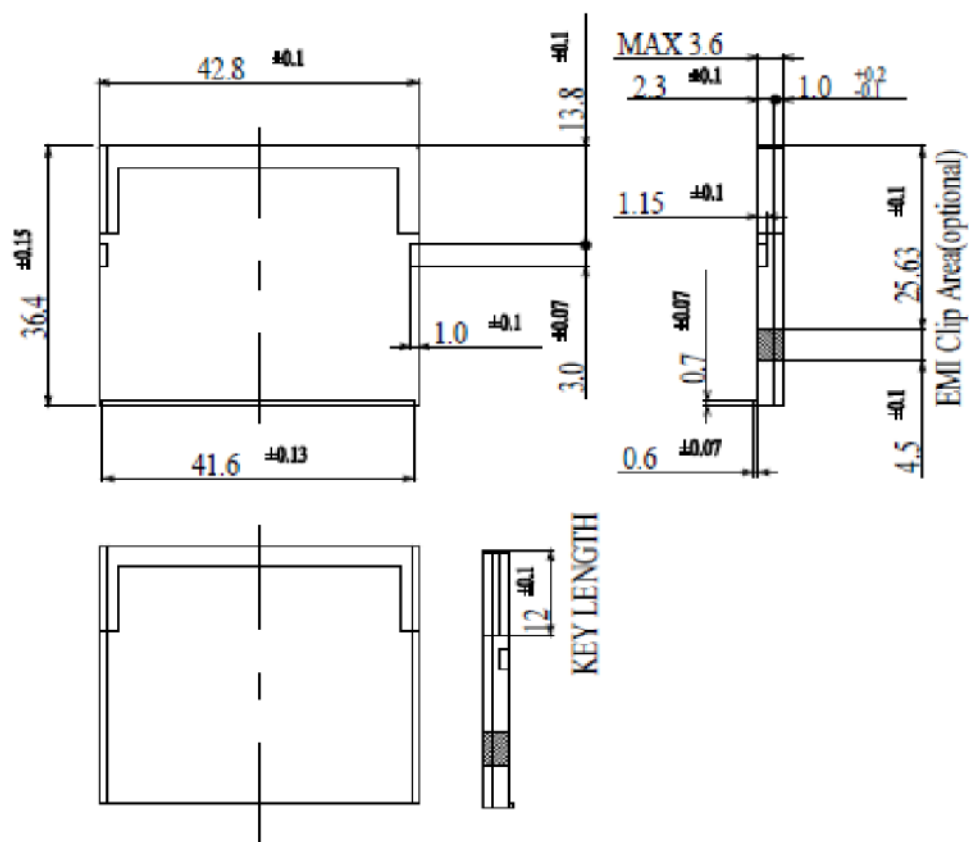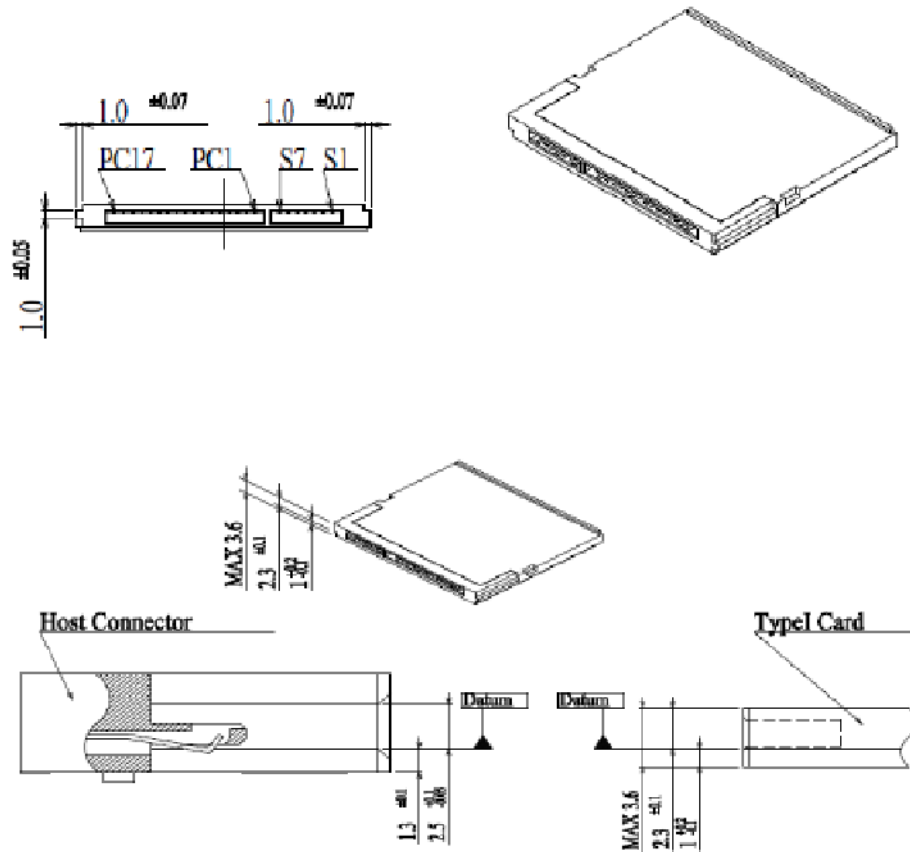
7.1.1 Pin Assignments

Pin #	CFAST	Description
S1	SGND	Signal ground
S2	A+	SATA pair A
S3	A-	
S4	SGND	Digital GND
S5	B-	SATA pair B
S6	B+	
S7	SGND	Signal ground
Key		
Key		
PC1	CDI	Card detect in
PC2	GND	Ground
PC3	NC	No connect
PC4	NC	No connect

Pin #	CFAST	Description
PC5	NC	No connect
PC6	NC	No connect
PC7	GND	Ground
PC8	LED1	LED output
PC9	LED2	LED output
PC10	IO1	Reserved
PC11	IO2	Reserved
PC12	IO3	Reserved
PC13	3.3V	Power
PC14	3.3V	Power
PC15	GND	Ground
PC16	GND	Ground
PC17	CDO	Card detect out

7.2 Electrical Interface

7.2.1 Supply Voltage

Parameter	Rating
Operating voltage	3.3V ± 5%

7.2.2 Power Consumption

Unit: mA

Capacity	Read (max)	Write (max)	Idle (max)
2 GB	125	145	65
4 GB	130	145	65
8 GB	315	190	65
16 GB	315	210	65
32 GB	315	230	65
64 GB	315	255	65

Notes:

- The measured input power voltage is 3.3 V.
- Power consumption might vary according to flash configuration, host platform, and other factors.

8. Identify Device and SMART Functionality

8.1 ATA Identify Device Information

The following table lists the information returned by the identify device ATA passthrough command.

Word Address	Default Value	Total Bytes	Data Field Type Information
0	0000h	2	General configuration bit significant information
1	XXXXh	2	Default number of cylinders
2	C837h	2	Specific configuration
3	00XXh	2	Default number of heads
4 – 5	0000h	4	Reserved
6	XXXXh	2	Default number of sectors per track
7 – 8	XXXXh	4	Number of sectors per card
9	0000h	2	Reserved
10-19	XXXXh	20	Serial number (20 ASCII characters)

Word Address	Default Value	Total Bytes	Data Field Type Information
20 – 21	0000h	4	Reserved
22	0000h	2	Number of ECC bytes passed on read/write long commands
23 – 26	XXXXh	8	Firmware revision (8 ASCII characters)
27 – 46	XXXXh	40	Model number (40 ASCII characters)
47	8001h	2	Maximum 1 sector on read/write multiple command
48	0000h	2	Double word not supported
49	0F00h	2	Capabilities: DMA, LBA, IORDY supported
50	4001h	2	Capabilities: device specific standby timer
51	0200h	2	PIO data transfer cycle timing mode 2
52	0000h	2	DMA data transfer cycle timing mode not
53	0007h	2	Data fields 54 to 58, 64 to 70, and 88 are valid
54	XXXXh	2	Number of current logical cylinders
55	XXXXh	2	Number of current logical heads
56	XXXXh	2	Number of current logical sectors per track
57 – 58	XXXXh	4	Current capacity in sectors
59	010Xh	2	Multiple sector setting is valid
60-61	XXXXh	4	Total number of sectors addressable in LBA
62	0000h	2	Single Word DMA transfer not implemented
63	0X0Xh	2	Multiword DMA transfer mode
64	0003h	2	Advanced PIO modes: modes 3 and 4 supported
65	0078h	2	Minimum multiword DMA cycle time, 0 if no MDMA
66	0078h	2	Recommended multiword DMA cycle time, 0 if no MDMA
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer cycle time with flow control
69	C100h	2	CFast, deterministic read after DSM trim, download microcode DMA supported
70 – 74	0000h	10	Reserved
75	001Fh	2	Queue depth
76	E20Eh	2	Serial ATA capabilities: READ LOG DMA EXT, device automatic partial to slumber transitions, SATA Gen 1-3 supported, host automatic partial to slumber transitions, Receipt of host-initiated interface power management requests
77	00CXh	2	Serial ATA additional capabilities: DevSleep to reduced power state, RECEIVE FPDMA QUEUED, SEND FPDMA QUEUED supported

Word Address	Default Value	Total Bytes	Data Field Type Information
78	015Eh	2	Serial ATA features supported: Device sleep, software settings preservation, in-order data delivery, device initiated interface power management, DMA setup auto-activate, non-zero buffer offsets supported
79	0XXXh	2	Serial ATA features enabled
80	0FE0h	2	Major version number, ATA-5 to ATA-8, ACS-1, to ACS-4 support
81	0000h	2	Minor version number, not reported
82	746Bh	2	Command set: NOP, READ BUFFER, WRITE BUFFER, Host Protected Area, look-ahead, volatile write cache, power management feature set, Security Mode feature set, SMART feature set
83	7509h	2	Command set: FLUSH CACHE, FLUSH CACHE EXT, LBA48, Set Max Security Extension, Advanced Power Management, DOWNLOAD MICROCODE
84	4161h	2	Command set/feature supported extension: World Wide Name, Write FUA Ext, General Purpose Logging, SMART self-test, SMART error logging
85	74XXh	2	Command set enabled: NOP, READ BUFFER, WRITE BUFFER, Host Protected Area, look ahead enabled/disabled, volatile write cache enabled/disabled, power management feature set, Security Mode feature set enabled/disabled, SMART feature set enabled/disabled
86	F409h	2	Command set enabled: FLUSH CACHE, FLUSH CACHE EXT, LBA48, DOWNLOAD MICROCODE, words 119 and 120 supported
87	4161h	2	Command set/feature default
88	XXXXh	2	UDMA transfer mode enabled and supported
89	00XXh	2	Time for security erase unit
90	00XXh	2	Time for enhanced security erase unit
91	00XXh	2	Advanced power management level
92	XXXXh	2	Master password revision code
93	XXXXh	2	Hardware reset result
94 – 99	0000h	12	Reserved
100 – 103	XXXXh	8	Total number of sectors addressable in LBA48 mode
104	0000h	2	Reserved
105	0001h	2	Number of sectors per data set management command
106	4000h	2	Physical sector size/Logical sector size

Word Address	Default Value	Total Bytes	Data Field Type Information
107	0000h	2	Reserved
108 – 111	XXXXh	8	World wide name
112 – 118	0000h	14	Reserved
119	4008h	2	Commands and feature sets supported
120	4008h	2	Commands and feature sets supported or enabled
121-127	0000h	14	Reserved
128	0XXXh	2	Security status
129	XX00h	2	Write protect status • Bit 9 = permanent write protect from vendor command • Bit 8 = temporary write protect from vendor command
130-133	XXXXh	8	Firmware date string
134-135	0000h	4	Reserved
136-141	XXXXh	12	Firmware file name
142-147	XXXXh	12	Preformat file name
148-153	XXXXh	12	Anchor program file name
154	0000h	2	Firmware major revision
155	0000h	2	Firmware minor revision
156-160	0000h	10	Reserved
161	8202h	2	CFast specification major version 2, ACTPM supported
162 – 164	0000h	6	Reserved
165	80XXh	2	CFast card operating temperature range
166 – 168	0000h	6	Reserved
169	0001h	2	Trim bit in data set management supported
170 to 208	0000h	78	Reserved
209	4000h	2	Alignment of logical blocks within a larger physical block
210 – 216	0000h	14	Reserved
217	0001H	2	Solid state device (non-rotating media)
218 – 221	0000h	8	Reserved
222	11FFh	2	Transport major revision number: ATA8-AST, SATA 1.0 – SATA 3.3
223	0000h	2	Transport minor revision number
224-254	0000h	62	Reserved
255	XXA5h	2	Integrity word

8.2   ATA SMART Functionality

The F300 CFast firmware supports the following SMART commands, determined by the **features** register value.

Value	Command
D0h	Read data
D1h	Read attribute thresholds
D2h	SMART enable/disable attribute autosave
D5h	SMART read log
D6h	SMART write log
D8h	Enable SMART operations
D9h	Disable SMART operations
DAh	SMART return status
E0h	SMART read remap data
E1h	SMART read wear level data

SMART commands with **features** register values not mentioned in the above table are not supported and are aborted.

8.2.1   SMART Enable Operations

COMMAND CODE: B0h with a features register value of D8h

PROTOCOL: Non-data command

INPUTS:

Register	7	6	5	4	3	2	1	0
Features	D8h							
Sector count								
Sector number								
Cylinder low	4Fh							
Cylinder high	C2h							
Device/head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if the signature in the cylinder registers is invalid.

DESCRIPTION: This command enables access to the SMART capabilities of the CFast controller firmware. The state of SMART (enabled or disabled) is preserved across power cycles.

8.2.2 SMART Disable Operations

COMMAND CODE: B0h with a features register value of D9h

PROTOCOL: 5Ah

INPUTS:

Register	7	6	5	4	3	2	1	0
Features				D9h				
Sector count								
Sector number								
Cylinder low				4Fh				
Cylinder high				C2h				
Device/head	1	1	1	D				
Command				B0h				

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if either the signature in the cylinder registers is invalid or if SMART is not enabled.

DESCRIPTION: This command disables access to the SMART capabilities of the CFast controller firmware. The state of SMART (enabled or disabled) is preserved across power cycles.

8.2.3 SMART Enable/Disable Attribute Autosave

COMMAND CODE: B0h with a features register value of D2h

PROTOCOL: 5Ah

INPUTS:

Register	7	6	5	4	3	2	1	0
Features				D2h				
Sector count				00h or F1h				
Sector number								
Cylinder low				4Fh				
Cylinder high				C2h				
Device/head	1	1	1	D				
Command				B0h				

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if either the signature in the cylinder registers is invalid or if SMART is not enabled.

DESCRIPTION: This command is effectively a no-operation, as the data for the SMART function is always available and kept current in the firmware.

8.2.4 SMART Read Data

COMMAND CODE: B0h with a features register value of D0h

PROTOCOL: PIO data in

INPUTS:

Register	7	6	5	4	3	2	1	0
Features	D0h							
Sector count								
Sector number								
Cylinder low	4Fh							
Cylinder high	C2h							
Device/head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if the signature in the cylinder registers is invalid or if SMART is not enabled.

DESCRIPTION: This command returns one sector of SMART data. The data structure returned is shown in the "SMART Data Structure" section.

8.2.5 SMART Data Structure

The following 512 bytes make up the device SMART data structure. Users can obtain the data using the SMART read data command (D0h).

Byte	F/V	Description
0 – 1	0010h	SMART structure version
2 – 361		Attribute entries 1 to 30 (12 bytes each)
362	00h	Off-line data collection status (no off-line data collection)
363	00h	Self-test execution status byte (self-test completed)
364 – 365	0000h	Total time to complete off-line data collection activity
366	00h	—
367	00h	Off-line data collection capability (no off-line data collection)
368 – 369	0003h	SMART capability
370	00h	Error logging capability (no error logging)
371	00h	—
372	00h	Short self-test routine recommended polling time

Byte	F/V	Description
373	00h	Extended self-test routine recommended polling time
374 – 385	00h	Reserved
386 – 387	0004h	SMART structure version
388 – 391		Firmware "commit" counter
392 - 395		Firmware wear level threshold
396	01h	Global wear leveling active
397	01h	Global bad block management active
398 – 401		Average flash block erase count in native mode block pool
402 – 405		Number of flash blocks involved in wear leveling in all block pools
406 – 409		Number of total ECC errors in all block pools during firmware initialization
410 – 413		Number of correctable ECC errors in all block pools during firmware initialization
414 – 417		Number of flash blocks involved in wear leveling in native mode block pool
418 – 421		Number of total ECC errors in native mode block pool during firmware initialization
422 – 425		Number of correctable ECC errors in native block mode pool during firmware initialization
426 – 429		Average flash block erase count in SLC mode block pool
430 – 433		Number of flash blocks involved in wear leveling in SLC mode block pool
434 – 437		Number of total ECC errors in SLC mode block pool during firmware initialization
438 – 441		Number of correctable ECC errors in SLC mode block pool during firmware initialization
442 – 510	00h	—
511		Data structure checksum

- The attributes that are defined for the CFast firmware return their data in the attribute section of the SMART data, using a 12 byte data field.
- The field at offset 386 gives a version number for the contents of the SMART data structure. For the controller in the WINSYSTEMS CFast, only version 4 is defined.
- The byte at offset 396 is fixed to 1 for page-based firmware. All chips within an interleaved channel are used for wear leveling.
- The byte at offset 397 is fixed to 1 for page-based firmware. Bad block management is always done within all chips of an interleaved channel.
- The data at offsets 414 – 441 are available only for TLC flash types with separate block pools for native and SLC mode blocks.

Spare Block Count Attribute

This attribute gives information about the amount of available spare blocks.

Offset	Value	Description
0	196	Attribute ID – Reallocation count
1 – 2	0013h	Flags – Pre-fail type, attribute value is updated during normal operation, attribute is an event count
3		Attribute value The value returned here is the percentage of remaining spare blocks summed over all flash chips, that is, (100 x current spare blocks/initial spare blocks)
4		Attribute value (worst value)
5 – 7		Sum of the initial number of spare blocks for all flash chips
8 – 10		Sum of the current number of spare blocks for all flash chips
11	00h	Reserved

This attribute is used for the SMART return status command. If the attribute value field is less than the spare block threshold (currently fixed at 10), the SMART return status command indicates a threshold exceeded condition.

Spare Block Count Worst Chip Attribute Threshold

This attribute gives information about the amount of available spare blocks on the interleave channel that has the lowest current number of spare blocks.

Offset	Value	Description
0	213	Attribute ID – Spare block count worst chip (vendor specific)
1 – 2	0013h	Flags – Pre-fail type, attribute value is updated during normal operation, attribute is an event count
3		Attribute value The value returned here is from all interleaved channels the worst percentage of remaining spare blocks, that is, (100 * current spare blocks/initial spare blocks)
4		Attribute value (worst value)
5 – 7		Initial number of spare blocks of the interleave channel with the lowest current number of spare blocks
8 – 10		Current number of spare blocks of the interleave channel with the lowest current number of spare blocks
11	00h	Reserved

Erase Count Attribute

The erase count usage attribute gives information about the amount of flash block erases that have been performed.

Offset	Value	Description
0	229	Attribute ID – Erase count usage (vendor specific)
1 – 2	001Xh	Flags – Pre-fail or advisory type, attribute value is updated during normal operation, attribute is an event count
3		Attribute value The value returned here is an estimation of the remaining card life, in percent, based on the number of flash block erases compared to the target number of erase cycles per block
4		Attribute value (worst value)
5 – 10		Estimated total number of block erases
11	00h	Reserved

This attribute is used for the SMART return status command. If the attribute value field is less than the erase count threshold (currently fixed at 10), the SMART return status command indicates a threshold exceeded condition.

The target number of erase cycles per flash block is taken from the **MaxBlockEraseCount** column in the Device Description file.

Total ECC Errors Attribute

The number of ECC errors attribute gives information about the total number of ECC errors that have occurred on flash read commands during firmware runtime. This attribute is not used for the SMART return status command.

Offset	Value	Description
0	203	Attribute ID – Number of ECC errors
1 – 2	001Ah	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count, attribute is an error rate
3	64h	Attribute value; this value is fixed at 100
4	64h	Attribute value (worst value)
5 – 8		Total number of ECC errors (correctable and uncorrectable)
9 – 10		—
11	00h	Reserved

Correctable ECC Errors Attribute

The number of corrected ECC errors attribute gives information about the total number of correctable ECC errors that have occurred on flash read commands during firmware runtime. This attribute is not used for the SMART return status command.

Offset	Value	Description
0	204	Attribute ID – Number of corrected ECC errors
1 – 2	001Ah	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count, attribute is an error rate
3	64h	Attribute value; this value is fixed at 100
4	64h	Attribute value (worst value)
5 – 8		Total number of correctable ECC errors
9 – 10		—
11	00h	Reserved

UDMA CRC Errors Attribute

The UDMA CRC error rate attribute gives information about the total number of SATA CRC errors.

Offset	Value	Description
0	199	Attribute ID –UDMA CRC error rate
1 – 2	001Ah	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count, attribute is an error rate
3	64h	Attribute value; this value is fixed at 100
4	64h	Attribute value (worst value)
5 – 8		Total number of SATA CRC errors
9 – 10		—
11	00h	Reserved

Total Number of Reads Attribute

The number of reads attribute gives information about the total number of sectors read from flash, which can be useful for the interpretation of the number of correctable or total ECC errors. This attribute is not used for the SMART return status command.

Offset	Value	Description
0	232	Attribute ID – Number of reads (vendor specific)
1 – 2	0012h	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count
3	64h	Attribute value; this value is fixed at 100

Offset	Value	Description
4	64h	Attribute value (worst value)
5 - 10		Total number of flash read commands
11	00h	Reserved

Power On Count Attribute

Offset	Value	Description
0	12	Attribute ID – Power on count (vendor specific)
1 – 2	0012h	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count
3	64h	Attribute value; this value is fixed at 100
4	64h	Attribute value (worst value)
5 - 8		Number of power On cycles
9 – 10		—
11	00h	Reserved

Total LBAs Written Attribute

The total LBAs written attribute gives the total amount of data written to the disk, in units of 32 MB (65536 sectors.) This number can be converted to terabytes written (TBW) by dividing the raw attribute value by 2^{15}.

Offset	Value	Description
0	241	Attribute ID – Total LBAs written (vendor specific)
1 – 2	0012h	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count
3	64h	Attribute value; this value is fixed at 100
4	64h	Attribute value (worst value)
5 - 10		Total number of LBAs written to the disk, divided by 65536
11	00h	Reserved

Total LBAs Read Attribute

The total LBAs read attribute gives the total amount of data read from the disk, in units of 32 MB (65536 sectors.) This number can be converted to terabytes read by dividing the raw attribute value by 2^{15}.

Offset	Value	Description
0	241	Attribute ID – Total LBAs read (vendor specific)
1 – 2	0012h	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count
3	64h	Attribute value; this value is fixed at 100
4	64h	Attribute value (worst value)

Offset	Value	Description
5 - 10		Total number of LBAs read from the disk, divided by 65536
11	00h	Reserved

Anchor Block Status Attribute

The anchor block status attribute reports how many times the anchor block of the card has been re-written, either by the anchor block repair routine, or by a firmware update.

Offset	Value	Description
0	214	Attribute ID – Anchor block status (vendor specific)
1 – 2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value; this value is fixed at 100
4	64h	Attribute value (worst value)
5 – 8		Anchor block write count
9 – 10		—
11	00h	Reserved

Trim Status Attribute

The trim status attribute gives percent ratio for the disk space that is currently in the trimmed state (as a percentage).

Offset	Value	Description
0	215	Attribute ID – Trim status (vendor specific)
1 – 2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3		Attribute value
4		Attribute value (worst value)
5 - 10		—
11	00h	Reserved

Temperature Status Attribute

The temperature status attribute reports the current, min, and max temperature of the internal temp sensors. The attribute value is set to the current temperature and the worst value is set to the maximum temperature. Temperature is read every 4 seconds.

Offset	Value	Description
0	194	Attribute ID – Temperature status (vendor specific)
1 – 2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3		Attribute value
4		Attribute value (worst value)
5 - 10		—
11	00h	Reserved

8.2.6 SMART Read Attribute Thresholds

COMMAND CODE: B0h with a features register value of D1h

PROTOCOL: PIO data in

INPUTS:

Register	7	6	5	4	3	2	1	0
Features	D1h							
Sector count								
Sector number								
Cylinder low	4Fh							
Cylinder high	C2h							
Device/head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if either the signature in the cylinder registers is invalid or if SMART is not enabled.

DESCRIPTION: This command returns one sector of SMART attribute thresholds. The data structure returned is shown in the table below.

Offset	Value	Description
0 - 1	001h	SMART structure version
2 – 361		Attribute threshold entries 1 to 30 (12 bytes each)
362 – 379	00h	Reserved
380 – 510	00h	—
511		Data structure checksum

Spare Block Count Attribute Threshold

Offset	Value	Description
0	196	Attribute ID – Reallocation count

Offset	Value	Description
1		Spare block count threshold
2 - 11	00h	Reserved

Spare Block Count Worst Channel Attribute Threshold

Offset	Value	Description
0	213	Attribute ID – Spare block count worst channel (vendor specific)
1		Spare block count worst channel threshold
2 - 11	00h	Reserved

Erase Count Attribute Threshold

Offset	Value	Description
0	229	Attribute ID – Erase count usage (vendor specific)
1		Erase count threshold
2 - 11	00h	Reserved

Total ECC Errors Attribute Threshold

Offset	Value	Description
0	203	Attribute ID – Number of ECC errors
1	00h	No threshold for the total ECC errors attribute
2 - 11	00h	Reserved

Correctable ECC Errors Attribute Threshold

Offset	Value	Description
0	204	Attribute ID – Number of corrected ECC errors
1	00h	No threshold for the correctable ECC errors attribute
2 - 11	00h	Reserved

UDMA CRC Errors Attribute Threshold

Offset	Value	Description
0	199	Attribute ID – UDMA CRC error rate
1	00h	No threshold for the UDMA CRC errors attribute
2 - 11	00h	Reserved

Total Number of Reads Attribute Threshold

Offset	Value	Description
0	232	Attribute ID – Number of reads (vendor specific)
1	00h	No threshold for the total number of reads attribute
2 - 11	00h	Reserved

Power On Count Attribute Threshold

Offset	Value	Description
0	12	Attribute ID – Power on count
1	00h	No threshold for the power on count attribute
2 - 11	00h	Reserved

Total LBAs Written Attribute Threshold

Offset	Value	Description
0	241	Attribute ID –Total LBAs written (vendor specific)
1	00h	No threshold for the total LBAs written attribute
2 - 11	00h	Reserved

Total LBAs Read Attribute Threshold

Offset	Value	Description
0	242	Attribute ID – Total LBAs read (vendor specific)
1	00h	No threshold for the total LBAs read attribute
2 - 11	00h	Reserved

Anchor Block Status Attribute Threshold

Offset	Value	Description
0	214	Attribute ID – Anchor block status (vendor specific)
1	00h	No threshold for the anchor block status attribute
2 - 11	00h	Reserved

Trim Status Attribute Threshold

Offset	Value	Description
0	215	Attribute ID – Trim status (vendor specific)
1	00h	No threshold for the trim status attribute
2 - 11	00h	Reserved

Temperature Status Attribute Threshold

Offset	Value	Description
0	194	Attribute ID – Trim status (vendor specific)
1	00h	No threshold for the trim status attribute
2 - 11	00h	Reserved

8.2.7 SMART Return Status

COMMAND CODE: B0h with a features register value of DAh

PROTOCOL: 5Ah

INPUTS:

Register	7	6	5	4	3	2	1	0
Features	DAh							
Sector count								
Sector number								
Cylinder low	4Fh							
Cylinder high	C2h							
Device/head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS: Returns a status indication as described below.

ERROR OUTPUTS: Aborted if the signature in the cylinder registers is invalid or if SMART is not enabled.

DESCRIPTION: This command checks the device reliability status. If a threshold exceeded condition exists for either the spare block count worst channel attribute or the erase count attribute, the device sets the cylinder low register to F4h and the cylinder high register to 2Ch. If no threshold exceeded condition exists, the device sets the cylinder low register to 4Fh and the cylinder high register to C2h.

8.2.8 SMART Read Log

COMMAND CODE: B0h with a features register value of D5h

PROTOCOL: PIO data in

INPUTS:

Register	7	6	5	4	3	2	1	0
Features	D5h							
Sector count	Number of sectors to be read							
Sector number	Log address							
Cylinder low	4Fh							
Cylinder high	C2h							
Device/head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if the signature in the cylinder registers is invalid or if SMART is not enabled.

DESCRIPTION: This command returns data of the SMART log. The following log addresses are defined.

Address	Description
0x00	Log directory
0x80 – 0x9F	Host vendor-specific logs
0xA0	SMART wear level data
0xA1	SMART remap data
0xA2	Reserved

The log directory (at log address 0) returns one sector that shows the number of sectors for log addresses 1 to 255.

Offset	Value	Description
0 – 1	1	SMART logging version
2 – 3	1	Number of sectors in the SMART error log
4 – 5	51	Number of sectors in the comprehensive SMART error log
6 – 7	16383	Number of sectors in the extended comprehensive SMART error log
96 – 97	9	Identify device data
256 – 319	16	Number of sectors in the logs at addresses 0x80 – 0x9F
320 – 321	4	Number of sectors in the log at address 0xA0
322 – 323	1	Number of sectors in the log at address 0xA1
324 – 325	1	Number of sectors in the log at address 0xA2

All other bytes in the log directory are zero.

The SMART error logs contain entries for internal flash errors or host transfer errors, based on the same data that is returned by the read error log command. If the corresponding host command for a flash error could not be determined, the command code field in the error entry is set to

0xF0. For flash errors that do not correspond to a processed host command, the command code field is set to 0xFF.

The host vendor-specific logs can be used by the host to store and retrieve arbitrary data.

8.2.9 SMART Write Log

COMMAND CODE: B0h with a features register value of D6h

PROTOCOL: PIO data out

INPUTS:

Register	7	6	5	4	3	2	1	0
Features	D6h							
Sector count	Number of sectors to be written							
Sector number	Log address							
Cylinder low	4Fh							
Cylinder high	C2h							
Device/head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if the signature in the cylinder registers is invalid, the log address or the number of sectors is invalid, or if SMART is not enabled.

DESCRIPTION: This command can be used to write data into the SMART log. Writes are allowed only to the host vendor-specific logs. All other log addresses can only be read.

8.2.10 SMART Read Remap Data

COMMAND CODE: B0h with a features register value of E0h

PROTOCOL: PIO data in

INPUTS:

Register	7	6	5	4	3	2	1	0
Features	E0h							
Sector count	01h							
Sector number								
Cylinder low	4Fh							
Cylinder high	C2h							
Device/head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if the signature in the cylinder registers is invalid, if the sector count is not 1, or if SMART is not enabled.

DESCRIPTION: This command returns status information for the internal bad block mapping algorithm. The returned data gives the initial number of flash memory blocks available for remapping bad blocks and the current number of blocks available for remapping bad blocks. All numbers are reported per interleave factor.

The data layout is shown in the table.

Offset	Description
0 – 31	Initial number of spare blocks for interleave units 1 to 16
32 – 63	Current number of spare blocks for interleave units 1 to 16

8.2.11 SMART Read Wear Level Data

COMMAND CODE: B0h with a features register value of E1h

PROTOCOL: PIO data in

INPUTS:

Register	7	6	5	4	3	2	1	0
Features				E1h				
Sector count				04h				
Sector number								
Cylinder low				4Fh				
Cylinder high				C2h				
Device/head	1	1	1	D				
Command				B0h				

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if the signature in the cylinder registers is invalid, if the sector count is greater than 4, or if SMART is not enabled.

DESCRIPTION: This command returns information regarding the status of the wear leveling. The information returned is the distribution of the blocks into the 1024 possible wear level classes. For each of the non-empty wear level classes, the number of blocks that have this class is returned in the return data.

Offset	Description
0 – 3	Marker bytes, fixed value of 0xFFFFFFFF
4 – 5	Lowest wear level class
6 – 7	Highest wear level class
8 – 15	Wear level class entry 1
16 – 23	Wear level class entry 2
....	....
2040 – 2047	Wear level class entry 255

Each wear level class entry consists of this data.

Unused wear level class entries are zero.

Offset	Description
0 – 3	Wear level class index
4 – 7	Number of blocks in this wear level class

This product may contain chemicals known to the State of California to cause cancer, birth defects, or other reproductive harm. For more information go to www.p65warnings.ca.gov.

Appendix A. Best Practices

This section outlines the best practices for operating the CFAST-B-XXG-SI in a safe and effective manner that does not damage the board. Read this section carefully.

Avoid electrostatic discharge (ESD)
Only handle the circuit board and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

Power Down

Make sure that power has been removed from the system before inserting or removing the CFAST-B-XXG-SI from your host system.

Power Supply OFF
The power supply should always be off before installing the CFAST-B-XXG-SI. Do not hot-plug the CFAST-B-XXG-SI on a host platform that is already powered.

I/O Connections OFF—I/O Connections should also be off before connecting them to the embedded computer modules or any I/O cards. Connecting hot signals can cause damage whether the embedded system is powered or not.

Operations/Product Manuals

Every WINSYSTEMS product has an Operations manual or Product manual.

Periodic Updates—Operations/Product manuals are updated often. Periodically check the WINSYSTEMS website (http://www.winsystems.com) for revisions.

Check Pinouts—Always check the pinout and connector locations in the manual before plugging in a cable. Many I/O modules have identical headers for different functions and plugging a cable into the wrong header can have disastrous results.

Contact an Applications Engineer—If a diagram or chart in a manual does not seem to match your board, or if you have additional questions, contact a WINSYSTEMS Applications Engineer at: +1-817-274-7553.

Appendix B. Warranty Information

WINSYSTEMS warrants that for a period of two (2) years from the date of shipment, any Products and Software purchased or licensed hereunder which have been developed or manufactured by WINSYSTEMS shall be free of any defects and shall perform substantially in accordance with WINSYSTEMS' specifications therefor. With respect to any Products or Software purchased or licensed hereunder which have been developed or manufactured by others, WINSYSTEMS shall transfer and assign to Customer any warranty of such manufacturer or developer held by WINSYSTEMS, provided that the warranty, if any, may be assigned. The sole obligation of WINSYSTEMS for any breach of warranty contained herein shall be, at its option, either (i) to repair or replace at its expense any materially defective Products or Software, or (ii) to take back such Products and Software and refund the Customer the purchase price and any license fees paid for the same. Customer shall pay all freight, duty, broker's fees, insurance, charges and other fees and charges for the return of any Products or Software to WINSYSTEMS under this warranty. WINSYSTEMS shall pay freight and insurance charges for any repaired or replaced Products or Software thereafter delivered to Customer within the United States. All fees and costs for shipment outside of the United States shall be paid by Customer. The foregoing warranty shall not apply to any Products or Software which have been subject to abuse, misuse, vandalism, accident, alteration, neglect, unauthorized repair or improper installation.

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Until title to the Products pass in accordance with the provision set out above, except with the prior written approval of WINSYSTEMS, no Products shall be modified, altered, moved or in any way assigned, sublet, mortgaged or charged nor may Customer part with possession of all or part of the same.

There are no understandings, agreements or representations, express or implied, other than those set forth herein. This Order embodies the entire agreement between the parties and may be waived, amended or supplemented only by a written instrument executed jointly by WINSYSTEMS and Customer as evidenced only by the signature of duly authorized officers of each party. The foregoing terms and conditions of any order which may be issued by Customer for the purchase of Products or licensing of Software hereunder.

In the event this Order is placed in the hands of an attorney or collection agency by WINSYSTEMS to collect any sums due hereunder to WINSYSTEMS, Customer shall pay all reasonable attorney's fees, expenses, collection and court costs incurred by WINSYSTEMS.

THIS AGREEMENT SHALL BE GOVERNED AND CONSTRUED UNDER THE TEXAS UNIFORM COMMERCIAL CODE AND THE APPLICABLE LAWS OF THE STATE OF TEXAS. THE PARTIES ACKNOWLEDGE THAT ANY ACTION BROUGHT HEREUNDER SHALL ONLY BE BROUGHT IN A COURT OF COMPETENT JURISDICTION IN TARRANT COUNTY, TEXAS.

Warranty Service

1. To obtain service under this warranty, obtain a return authorization number. In the United States, contact the WINSYSTEMS Service Center for a return authorization number. Outside the United States, contact your local sales agent for a return authorization number.
2. You must send the product postage prepaid and insured. You must enclose the products in an anti-static bag to protect from damage by static electricity. WINSYSTEMS is not responsible for damage to the product due to static electricity.