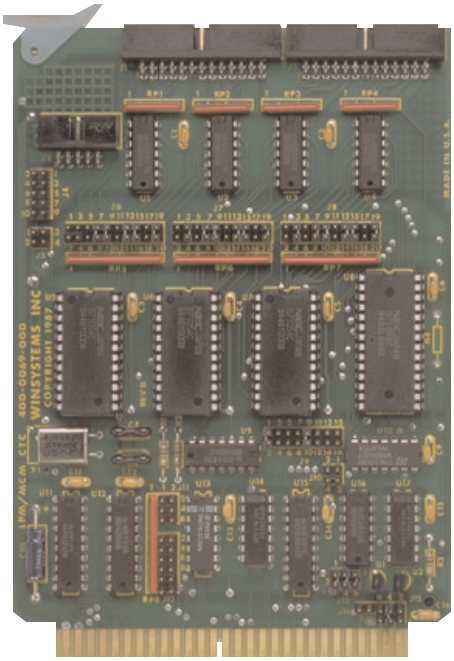
WinSystems®

STD BUS, CMOS STD BUS

LPM-CTC
MCM-CTC
9-Channel Counter/Timer

FEATURES

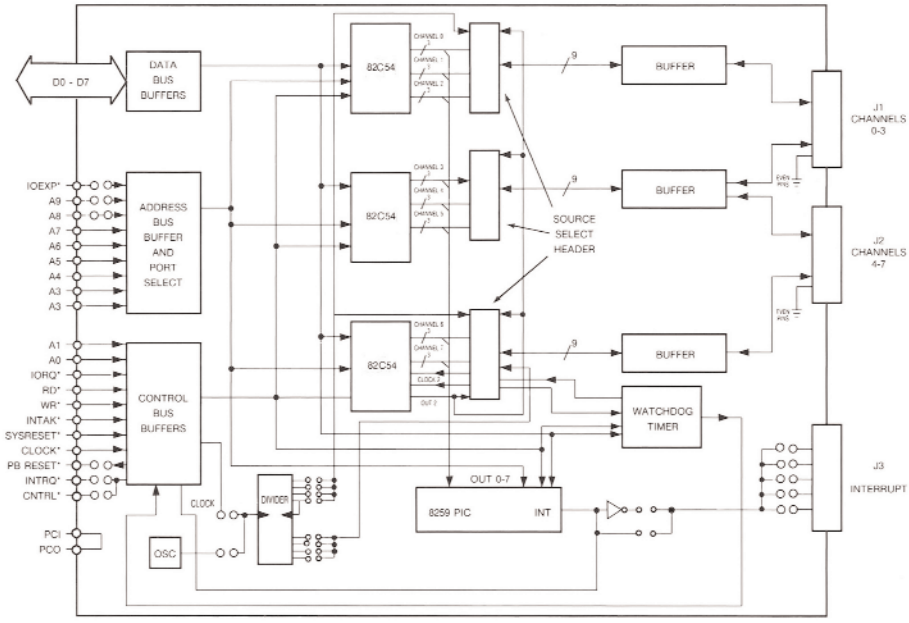
- Nine independent 16-bit Counter/Timers
- Uses 3 standard 82C54 Programmable Interval Timers
- Six programmable counter modes per channel
- Handles inputs from DC to 8 MHz
- Binary or BCD counting
- Clock, Gate, and Out signals from 8 channels buffered and accessed via 2 connectors
- Channel 9 configurable as clock source for other channels
- Optional 82C59A Interrupt Controller
- Configurable Watchdog Timer
- Single +5 volt supply
- Available for CMOS STD Bus: LPM-CTC



The LPM/MCM-CTC card is designed to solve the common timing problems in industrial systems design. Nine independent 16-bit channels are capable of frequency/event counting from DC to 8 MHz, pulse marker or square wave generation, time interval measurements, and one-shot simulation. Eight channels have a buffered Clock, Gate, and Output available at the top of the card. Jumper headers provide source selection and cascading to yield maximum configuration flexibility.

FUNCTIONAL CAPABILITY

STD Bus Interface - The LPM-CTC is the CMOS STD Bus versions and the MCM-CTC is the STD Bus versions of these cards. The LPM/MCM prefix



indicates the card has the same features and functionality. The differences between the two products are the various power requirements, bus interface levels, and operation temperature ranges.

Addressing - The LPM/MCM-CTC is I/O mapped for either 8 or 10-bit I/O addressing and is jumper configurable to start on any even 16 byte boundary.

Counter/Timers - The LPM/MCM-CTC utilizes three 82C54 programmable interval timers that can be individually configured to be real time clocks, event counters, digital one-shots, square wave generators, or programmable rate generators. Each 82C54 contains three independent software programmable counter/timers yielding a total of nine 16-bit channels. The individual channels can be cascaded for longer count sequences.

The three internal 82C54 counters are identical in operation. Each consists of a single, 16-bit, presettable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of modes stored in the Control Word Register. The status of the contents of each counter is available to the computer with a simple READ operation for event counting applications. Special logic is included so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

Watchdog Timer - The nineth channel can alternatively be used as a watchdog timer. This channel, programmed in the retriggerable one-shot mode, can have its output jumpered to the PBRESET* line of the STD Bus and CMOS STD Bus which will force a system reset in case of a software malfunction.

Time Base Clock - The nineth channel can also serve as a jumper selectable clock input to any of the other 8 channels for use in interval measurements. Either the System Clock or a onboard 2.4576 MHz crystal oscillator drives a dual divide by 2, 4, 8, or 16 prescaler that is input to Channel 9 and available to the other counters via the configuration header. The output of Channel 9's counter can be used to further scale the clock and its corresponding output is available to the other 8 channels.

Configuration Headers - Access to the Clock, Gate, Out and the boards Time Base Clock is provided for all channels. A select header is provided to permit jumpering clock inputs from the I/O Connectors, Channel 9, or the System Clock.

Connector Configuration - The LPM/MCM-CTC has two, 26-pin connectors that permit access to the Clock, Gate and Out signals for each channel. The connectors are grouped with 4 channels per connector. All the signals are fully buffered on and off the board. Each signal line is paired with a ground line to prevent adjacent noise and crosstalk. All input lines have Schmitt trigger circuits to prevent oscillation from signals with slow rise and fall times.

Interrupts - The LPM/MCM-CTC will generate STD-8088 compatible interrupts when an optional 82C59A PIC is installed (LPM/MCM-CTC-1). The PIC generates a unique, vectored interrupt for each of the 8 CTC channels.

SPECIFICATIONS

Electrical

System Clock: Up to 8 MHz

Interface: Inputs - All inputs are 74HC/TTL levels
Outputs - All outputs are 74HC/TTL levels

Power Requirements:
LPM-CTC: +5V ± 10% at 20mA typ.
MCM-CTC: +5V ± 10% at 215mA typ.

Mechanical

Meets STD Bus mechanical specifications

Connectors

Channel: Two, 26-pin dual on 0.100 grid
Interrupt: 10-pin dual on 0.100 inch grid
Jumpers: 0.025 inch square posts

Environmental

Operating Temperature:
LPM-CTC -40°C to +85°C
MCM-CTC 0°C to +65°C
Non-condensing relative humidity: 5% to 95%

ORDERING INFORMATION

LPM-CTC-0	CMOS STD Bus Nine channel 16-bit counter/timer card
LPM-CTC-1	CMOS STD Bus Nine channel 16-bit counter/timer card with 82C59 PIC
MCM-CTC-0	STD Bus Nine channel 16-bit counter/timer card
MCM-CTC-1	STD Bus Nine channel 16-bit counter/timer card with 82C59 PIC

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